# 8-port Smart Gigabit Ethernet Switch Controller w/ memory

## Features

- 8 Ethernet 10/100/1000Mbps ports
- MII/GMII interface for all ports
- Two trunk groups with two ports at each group
- Four Classes of Service (CoS) selectable per port basis and/or checked via IP Header and 802.1Q VLAN Tag
- 8 Port-based VLANs group support
- Maximum throughput, non head-of-line blocking architecture
- Embedded 2 Mbit SSRAM packet buffer
- 8K MAC address table
- Configurable to 10Mbps, 100M full/half duplex and 1000M full duplex for each port
- IEEE 802.3x Flow Control
- Broadcast throttling
- Port Mirroring
- Serial EEPROM Interface
- 25Mhz oscillator input only
- MDIO master for PHY configuration / polling
- Low power 1.8V/3.3V dual voltage power supply
- 0.18um CMOS technology
- 292-pin PBGA

## Functional Description

TC9208M is a fully integrated 8-port 10/100/1000Mbps smart Ethernet switch controller designed for low cost and high performance solutions. The chip embeds all necessary SSRAM for packet buffer and MAC address table. It provides MII / GMII interface for all ports. A store-and-forward switching method using a non-blocking architecture is implemented within TC9208M to improve the availability and bandwidth.

**Classes of Service**

TC9208M provides evolved CoS with four levels of priority. The priority can be checked via layer 2 (802.1Q VLAN Tagging) and/or layer 3 (IP Header TOS bits). Port based priority is also provided to ensure transmission with precedence for all packets incoming from selected port(s). This feature allows improved support for multimedia applications.

**Flow Control**

The chip embeds IEEE 802.3 MAC functions for 8 ports supporting full and half duplex modes for both 10 and 100 Mbits/s data rates and full duplex for 1000 Mbit/s. Each port includes dedicated receive and transmit FIFOs with necessary logic to implement flow control for both duplex modes. TC9208M uses IEEE 802.3x frame based flow control for full duplex and backpressure for half duplex.

**Port Mirroring**

TC9208M has the ability to set a pair of mirroring ports. The mirror source port will be simultaneously forwarded towards its regular destination and to the monitoring port. And the bad CRC / undersized frames will be filtered out.

**Broadcast Throttling**

In case of excessive broadcast, TC9208M will throttle the broadcast traffic based on buffer memory loading. Both global buffer pool loading and source port loading are considered. The number of frame buffers that can be consumed by broadcast packets received from an individual source port is permanently limited to a EEPROM configurable value.

**Trunk Configuration**

Increased interconnection bandwidth can be achieved using TC9208M's trunking capabilities. Two trunk groups of up to two ports each can be setup with TC9208M. Several load-balancing schemes are provided through pin and EEPROM configuration. A port mirror feature, optionally including bad frames, can be used for debugging network problems.

**EEPROM interface**

The pin configuration interface comprises 40 configurations, which are shared with GMII output pins by latching the configuration data during reset. An external EEPROM device can also be used to configure the TC9208M at power-up. With reference to pin configuration interface, the EEPROM extends the chip's configuration capability with new features and enables a jumper-less configuration mode using a parallel interface for reprogramming. A virtual internal EEPROM mode is also provided to enable use of the programming interface in the absence of external EEPROM. TC9208M can make effective use of most of its features using only the pin configuration interface.

**Physical layer configuration/polling**

TC9208M includes a physical layer configuration / polling entity used to configure the PHY and monitor the physical layer transceiver's speed and duplex mode, link status and full duplex flow control ability for each port. The chip provides four modes of PHY configuration including an auto-negotiation disable procedure for 10/100Mbps speed modes. The PHY configuration information is provided through EEPROM settings.