ADVANCED INFORMATION

LOW-COST FLEXIBLE PWM CONTROLLER

FEATURES

- **Can Be Used For Power Factor Correction/Line Harmonics Reduction to Meet IEC1000-3-2 Requirements**
- **Maximum Duty Ratio 89% (typ.)**
- **Low Standby Current for Current-Fed Start-Up**
- **Current-Mode or Voltage-Mode Control**
- **Internal User-Adjustable Slope Compensation**
- **Pulse-by-Pulse Current Limiting**

APPLICATIONS

- **Power Factor Correction Converters**
- **Off-Line Power Supplies**
- **Industrial Power Supplies**
- **Off-Line Battery Charger**

DESCRIPTION

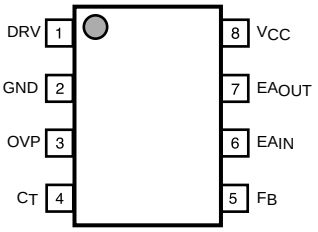
The TK75005 is an 8-pin PWM controller suitable for both voltage-mode and current-mode control. It also has advanced features not available in controllers with a higher pin count. One such feature is a sawtooth current flowing out of the feedback pin (FB), which provides a slope compensation ramp (in current mode applications) in proportion to the resistance terminating that FB pin.

The TK75005 offers the same features as the TK75003 with the addition of the Error Amplifier and the Overvoltage Protection (OVP) functions, and the deletion of the Overcurrent Frequency Reduction feature.

This PWM has features similar to the UC3842 (please refer to UC3842 Comparison Section).

TK75005

SOP-8



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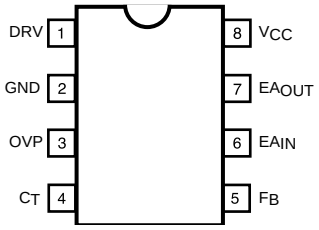
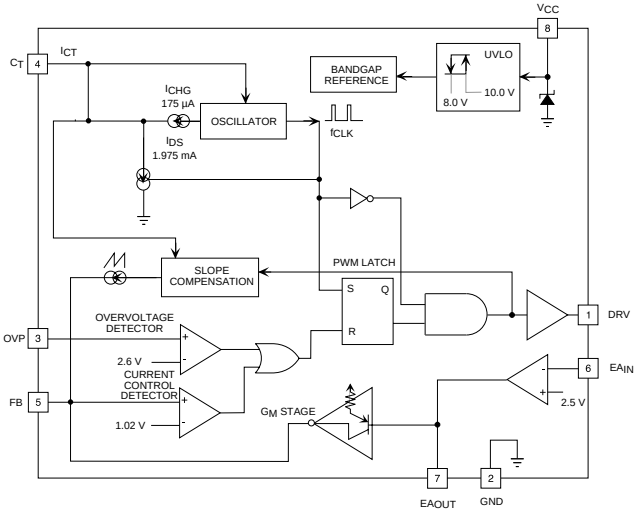


BLOCK DIAGRAM



ORDERING INFORMATION

TK75005 □□□□

- Package Code
- Tape/Reel Code
- Temp. Range

PACKAGE CODE	TEMPERATURE RANGE	TAPE/REEL CODE
D: DIP-8	C: -40 TO 80 °C	TL: Tape Left
M: SOP-8		MG: Magazine

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Low Impedance) ..... 18 V
Supply Voltage (I_{CC} < 30 mA) ..... Self Limiting
Power Dissipation (Note 1) ..... 800 mW
Output Energy ..... 5 µJ
C_T and FB Pins ..... 10 V
Junction Temperature ..... 150 °C
Storage Temperature Range ..... -55 to +150 °C
Operating Temperature Range ..... -20 to +80 °C
Extended Temperature Range ..... -40 to +85 °C
Lead Soldering Temperature (10 s) ..... 235 °C

TK75005 ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = 13 V, C_{CC} = 4.7 µF, C_T = 680 pF, C_{DRV} = 1000 pF, $T_A = T_j$ = Full Operating Temperature Range, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{CC(START)}$	Start-up Supply Current	Current Source to V_{IN} Pin		0.25	0.9	mA
$I_{CC(ON)}$	Operating Supply Current	EA_{IN} = 2 V		12	17	mA
		EA_{IN} = 3 V		14.5	19.0	mA
$V_{CC(ON)}$	UVLO Voltage ON	V_{CC} Sweeps Upward	9	10	11	V
$V_{CC(OFF)}$	UVLO Voltage OFF	V_{CC} Sweeps Downward	7	8	9	V
V_{HYST}	UVLO Hysteresis		1	2.0		V
OSCILLATOR SECTION (C_T PIN)						
f_{DRV}	Frequency at DRV Pin (Note 3)	$T_A = T_j$ = 25 ° C	90	100	110	kHz
		$T_A = T_j$ = Full Range	85		115	kHz
$V_{CT(PK)}$	Peak Voltage		2.5	3.2	3.9	V
$V_{CT(VL)}$	Valley Voltage			1.1		V
$I_{CT(DIS)}$	Discharge Current	$V_{CT} = V_{CT(PK)}$	1.0	1.8	3.0	mA
$C_{T(MAX)}$	Maximum Timing Capacitance		4.7			nF
CURRENT DETECTOR, OVERVOLTAGE PROTECTION (OVP PIN) AND SLOPE COMPENSATION SECTIONS						
V_{CCD}	Current Control Detector Reference Voltage	$T_A = T_j$ = 25 ° C	0.99	1.02	1.05	V
		$T_A = T_j$ = Full Range	0.966		1.077	V
t_{CCD}	Propogation Delay to DRV Pin	V_{FB} steps from 0 to 2 V		80	180	ns
V_{OVD}	Overvoltage Protection Detector Reference Voltage	$T_A = T_j$ = 25 ° C	2.51	2.60	2.69	V
		$T_A = T_j$ = Full Range	2.46		2.74	V
t_{OVP}	Propogation Delay to DRV Pin	V_{OVP} steps from 2 to 3 V		80	180	ns
$i_{SC(PK)}$	Slope Compensation Peak Current	C_T Pin = $V_{CT(PK)}$, $T_A = T_j$ = 25 ° C, $EA_{OUT(HIGH)}$,(Note 2)	-250	-205	-160	µA
$i_{SC(VL)}$	Slope Compensation Valley Current	C_T Pin = $V_{CT(VL)}$, $T_A = T_j$ = 25 ° C, $EA_{OUT(HIGH)}$,(Note 2)	-55	-30	-5	µA
$i_{SC(PK-VL)}$	Slope Compensation Peak to Valley	C_T Pin = $V_{CT(PK)}$, $T_A = T_j$ = 25 ° C, $EA_{OUT(HIGH)}$,(Note 2)	-215	-175	-135	µA

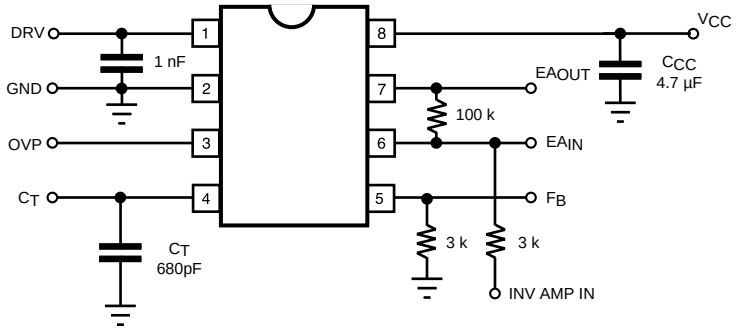
TK75005 ELECTRICAL CHARACTERISTICS (CONT.)

Test Conditions: V_{CC} = 13 V, C_{CC} = 4.7 µF, C_T = 680 pF, C_{DRV} = 1000 pF, $T_A = T_j$ = Full Operating Temperature Range, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ERROR AMPLIFIER AND GM STAGE SECTIONS (EA_{IN} AND EA_{OUT} PINS)						
V_{ref}	Reference Voltage	$T_A = T_j$ = 25 ° C	2.43	2.50	2.57	V
		$T_A = T_j$ = Full Range	2.37		2.64	V
I_{IB}	Input Bias Current			1.0		µA
A_{VD}	Open Loop Gain		65	75		dB
	Unity Gain Bandwidth	(Note 3)		2		MHz
PSRR	Power Supply Rejection Ratio	(Note 3)	60	70		dB
$I_{OUT(SINK)}$	Output Sink Current	EA_{OUT} = 1.2 V	2	6.8		mA
$I_{OUT(SOURCE)}$	Output Source Current	EA_{OUT} = 3.5 V		-1.1	-0.5	mA
$V_{OUT(HIGH)}$	$V_{OUT(HIGH)}$ at EA_{OUT} Pin	EA_{IN} @ 2 V	3.5	4.1		V
$V_{OUT(LOW)}$	$V_{OUT(LOW)}$ at EA_{OUT} Pin	EA_{IN} @ 3 V		0.4	0.7	V
$I_{GM(MAX)}$	$I_{OUT(MAX)}$ at FB Pin from GM Stage	$EA_{OUT(LOW)}$, FB @ 2 V	-1.95	-1.50	-1.05	mA
$I_{GM(MIN)}$	$I_{OUT(MIN)}$ at FB Pin from GM Stage	$EA_{OUT(HIGH)}$, FB @ 2 V		-1.0		µA
OUTPUT SECTION (DRV PIN)						
$D_{DRV(MAX)}$	Maximim Duty ratio		86	89	92	%
$t_{DRV(RISE)}$	Rise Time	1000 pF load		25	75	ns
$t_{DRV(FALL)}$	Fall Time	1000 pF load		25	75	ns
$V_{DRV(HIGH)}$	Output Voltage HIGH	I_{DRV} = -40 mA	10.1	11.0		V
		I_{DRV} = 100 mA	10.0	10.8		V
$V_{DRV(LOW)}$	Output Voltage LOW	I_{DRV} = -40 mA		0.1	0.25	V
		I_{DRV} = 100 mA		0.2	0.50	V
		I_{DRV} = 5 mA, V_{IN} = 6 V		0.9	1.50	V

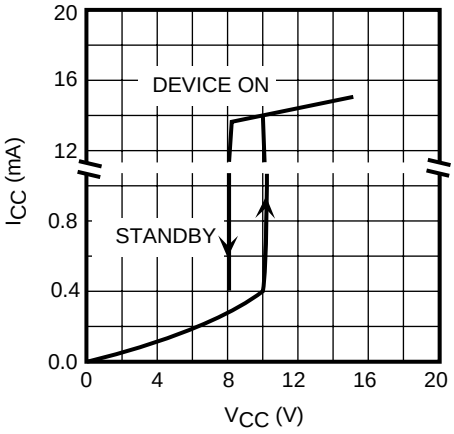
Note 1: Power dissipation for both packages (TK75005M and TK75005D) is 800 mW when mounted. Derate at 6.4 mW/°C for operation above 25 °C.
Note 2: For temperature dependence refer to "Slope Compensation Peak Current vs. Temperature" graph.
Note 3: Guaranteed by design; not 100% tested.

TEST CIRCUIT

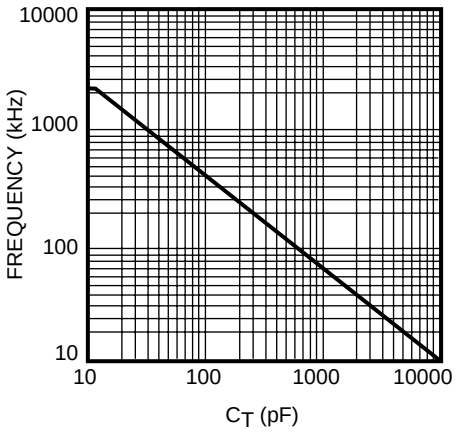


TYPICAL PERFORMANCE CHARACTERISTICS

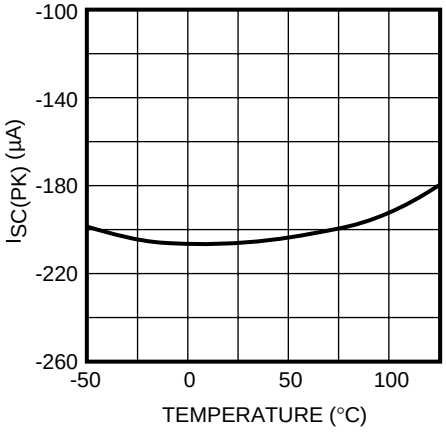
SUPPLY CURRENT vs. SUPPLY VOLTAGE



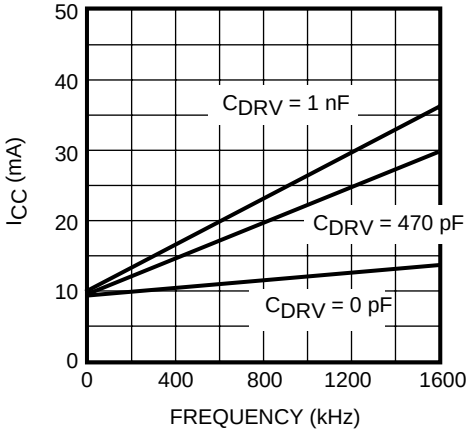
FREQUENCY AT DRV PIN vs. TIMING CAPACITANCE (-25 TO 85 °C)



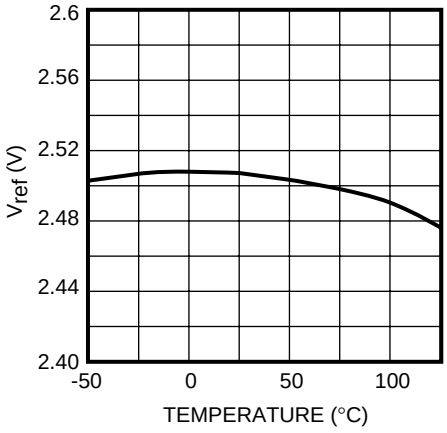
SLOPE COMPENSATION PEAK CURRENT vs. TEMPERATURE



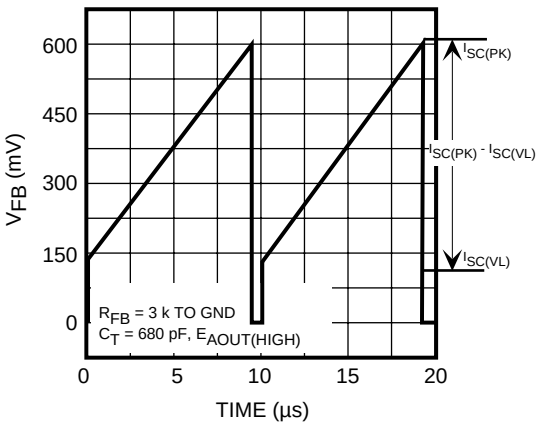
SUPPLY CURRENT vs. FREQUENCY AT DRV



REFERENCE VOLTAGE vs. TEMPERATURE



SLOPE COMPENSATION RAMP



PIN DESCRIPTIONS

DRIVE PIN (DRV)

This pin drives the external MOSFET with a totem pole output stage capable of sinking or sourcing a peak current of about 1 A. In standby mode, the DRV pin can sink about 5 mA while keeping the drive pin pulled down to about 1 V. This ensures that the external MOSFET can not be inadvertently turned on by leakage currents. The maximum duty cycle of the output signal is typically 89%.

GROUND PIN (GND)

This pin provides ground return for the IC.

OVERVOLTAGE PROTECTION INPUT PIN (OVP)

This pin provides a means of turning off the external transistor drive output independent of the PWM loop. This pin is normally used for overvoltage protection, but can also be used to provide a drive disabled function. The pin is the input to comparator with its other input referenced to 2.6 V, which tracks V_{ref} of error amp over temperature. and its output controlling the output driver of the IC. Therefore, if a voltage appears at this pin over 2.6 V, the voltage at the DRV pin drops to zero.

TIMING CAPACITOR PIN (C_T)

The external timing capacitor is connected to the C_T pin. That capacitor is the only component needed for setting the clock frequency. The frequency measured at the C_T pin is the same frequency as measured at the DRV pin. As the frequency of operation increases above 200 kHz, the maximum duty cycle decreases from a typical 89% at 200 kHz to 82% at 1.6 MHz. The maximum recommended clock frequency of the device is 1.6 MHz. At normal operation, during the rising section of the timing-capacitor voltage, a trimmed internal current of 175 μA flows out from the C_T pin and charges the capacitor. During the falling section of the timing-capacitor voltage, an internal current of about 1.8 mA discharges the capacitor.

FEEDBACK INPUT PIN (FB)

The feedback pin normally receives the sum of three signals: the switch current signal, the error signal (from the internal error amplifier and the GM stage), and a voltage ramp (from an internal sawtooth-shaped current with a peak value of about 205 μA) generated across the external terminating resistance. The switch current signal is needed in current-mode controlled converters and in converters with cycle-by-cycle overload protection. The error signal is needed for stabilizing the output voltage or current. The voltage ramp is needed for slope compensation (necessary for avoiding subharmonic instability in constant-frequency peak-current controlled current-mode converters above 50% duty ratio), or for Pulse Width Modulation (PWM) (in voltage-mode controlled converters).

At higher clock frequencies, the bandwidth limitation of the internally-generated sawtooth-shaped current source becomes more apparent. The degree to which ramp bandwidth is tolerable depends on performance requirements at narrow pulse widths. A low impedance at the feedback pin can effectively eliminate the internally-generated ramp effects and an external ramp can be readily created to attain higher performance at high frequencies, if desired.

ERROR AMPLIFIER COMPENSATION INPUT PIN (EA_{IN})

This pin is the inverting input of an operational amplifier which has its non-inverting input connected to 2.5 V. This is called the error amp because it amplifies the error between this pin's voltage and 2.5 V reference, which should reflect the error in the power supply's output regulation. The error amp provides a high gain stage so that the voltage loop gain can be high enough to provide good output voltage regulation.

ERROR AMPLIFIER COMPENSATION OUTPUT PIN (EA_{OUT})

This pin is the output of the operational amplifier mentioned in the EA_{IN} pin description. By picking the proper resistor and capacitor network connected between pins 6 and 7, the gain and frequency response of the error amp block of the voltage loop can be set, thus providing gain and frequency compensation into the PWM voltage loop as needed. This pin also acts as the input to the GM stage of the voltage control loop.

SUPPLY VOLTAGE PIN (V_{CC})

This pin is connected to the supply voltage. The IC is in a low-current (250 μA typ.) standby mode before the supply voltage exceeds 10 V (typ.), which is the upper threshold of the undervoltage lockout circuit. The IC switches back to standby mode when the supply voltage drops below 8 V (typ.).

THEORY OF OPERATION

The TK75005 is intended for use as a highly flexible primary-side PWM controller. The TK75005 is much like the TK75003 with the addition of an error amplifier, a GM stage and an overvoltage comparator, and the deletion of the TK75003 overcurrent frequency reduction feature. The many features integrated into a simple 8-pin design allow it to be easily configured for voltage-mode or current-mode control, fixed frequency or fixed off-time operation, off-line boot-strapping, and direct drive of a power MOSFET. Using a control technique referenced in the “Application Information” section, the TK75005 can be used as a highly cost-effective controller for power factor correction.

The most noteworthy integrated feature in the TK75005 is the way in which the feedback control pin is configured to receive the error signal and the current signal for current-mode control. Rather than receiving both inputs into a comparator, a single input receives both signals summed together and compares them against a fixed internal reference. This yields two desirable effects: 1) a current-limit threshold is automatically established, and 2) the required error-signal polarity is the inverse of that of a standard two-input current-mode control system. Generally, the signal summation requires no additional external components and adds the flexibility to add more control signals if desired.

Another function is integrated into the FB pin. A current ramp, which can be used to establish either the slope-compensation ramp for a current-mode control design or the voltage-comparison ramp for a voltage-mode control design, flows out of the FB pin. By adjusting the terminating resistance at the FB pin, the desired ramp magnitude is established.

The switching frequency is determined by an internal current source charging an external timing capacitor. The timing capacitor is ramped between internally-fixed thresholds, valley to peak, and then quickly discharged. A fixed off-time control technique can readily be implemented by using a small transistor to keep the timing capacitor discharged during the on-time. When the on-pulse is terminated, the timing capacitor ramps up to a fixed threshold at a fixed rate to set the off-time.

The Undervoltage Lockout (UVLO) feature with hysteresis minimizes the start-up current which allows a low-power boot-strap technique to be used for the housekeeping power. The duty ratio of the TK75005 is limited to approximately 89% by the time required to discharge the timing ramp.

UC3842 COMPARISON

Similarities to the UC3842

1) a single-ended transistor driver output with similar drive performance
2) an inverting error amplifier referenced to 2.5 V with similar electrical characteristics
3) a maximum threshold of ~1V on the current sense voltage used to terminate the PWM pulse
4) an 8-pin SOP-8 or DIP-8 package

Unique features of the TK75005

1) a multi-signal summation point at the FB pin, instead of a single function UC1842 C/S pin
2) built-in slope compensation sawtooth current coming out of the FB pin, reduced parts
3) an overvoltage protection pin compared to 2.6 V
4) switching frequency set using a single capacitor, reduced parts
5) different UVLO thresholds 10 V / 8 V
6) maximum duty cycle set at 89%

APPLICATIONS INFORMATION

BOOST POWER FACTOR CORRECTOR APPLICATION CIRCUIT

Figure 7 shows a universal-input, 100 W boost power factor corrector application circuit. The control technique is called "current-clamped control." Both the control technique and the application circuit with waveforms are described in the paper "Low-Cost Power Factor Correction/Line-Harmonics Reduction with Current-Clamped Boost Converter," published in the conference proceedings of Power Conversion Electronics '95/Powersystems World™ '95. A copy of the paper can be obtained by contacting Toko.

For designers who wish to explore other performance optimizations of the current-clamped boost power factor corrector, aside from the conference paper Toko offers a Mathcad© file which can accurately display current waveforms and predict power factor, harmonic distortion, and individual harmonic currents. The Mathcad file and the text which describes how to use it are available from the Colorado Springs Toko IC Design Center.

The power factor corrector in Figure 7 has been optimized for general wide-range-input use. In order to obtain the same performance at power levels other than 100 W, the control components do not need to change. The power component values change as follows: C_8 scales in proportion to the power level, and L_1 and R_8 scales in inverse proportion to the power level. Typically, although not directly related to the line-current shaping capability of the application circuit, C_1 and C_{10} would scale in proportion to the power level. All the components in the power stage should have a current rating as needed to accommodate the power level.

Below is a step-by-step design example, showing how to determine the resistance of R_7 terminating the feedback pin and the resistance of the current-sense resistor R_8, for the boost corrector of Figure 7.

Assumptions:

Output power:	P_{OUT} = 100 W
Output voltage:	V_{OUT} = 380 Vdc
Minimum line voltage:	$V_{I(MIN)}$ = 85 Vrms
Efficiency at 85 Vrms:	EFF = 0.93
Switching frequency:	f = 100 kHz
Inductance of boost inductor:	L_1 = 2.5 mH
Maximum duty ratio of TK75005:	D_{MAX} = 0.88
Peak value of ramp current flowing out of the FB pin:	$I_{SC(PK)}$ = 200 µA
Threshold voltage of the current-control detector:	V_{CCD} = 0.98 V

Calculations:

Peak value of minimum line voltage:

$$V_{I(MIN)(PK)} = \sqrt{2} \times V_{I(MIN)} = 120\ V_{PK}$$

Switch duty ratio at peak of minimum line voltage:

$$D = 1 - V_{I(MIN)(PK)} / V_{OUT} = 0.684$$

Peak-to-peak ripple current in inductor L_1:

$$I = V_{I(MIN)(PK)} \times D / (f \times L_1) = 0.33\ A$$

Input power at minimum line voltage:

$$P_I = P_{OUT} / EFF = 107.5\ W$$

Peak current in L_1 (at peak of minimum line voltage):

$$I_{L1(PK)} = \sqrt{2} \times P_I / V_{I(MIN)(PK)} + I/2 = 1.95\ A$$

Resistance of resistor R_7 (Note 1):

$$R_7 = D_{MAX} \times V_{CCD} / I_{SC(PK)} = 4.312\ kohms$$

APPLICATIONS INFORMATION (CONT.)

Select for R_7:

R_7 = 4.3 kohms

Resistance of current-sense resistor R_8 (Note 2):

$R_8 = (V_{CCD} - I_{SC(PK)} \times R_7 \times D) / I_{L1(PK)} = 0.201$ ohms

Select for R_8:
R_8 = 0.18 ohms

Note 1: This value of R_7 ensures that the line current will be zero around the zero-crossing of the line voltage, which is the required condition for low-distortion line current.

Note 2: This value of R_8 ensures that the sum of the voltage drop across R_8 (caused by the peak inductor current) and the voltage drop across R_7 (caused by the instantaneous value of the stabilizing current) is equal to the threshold voltage of the current-control detector at the peak of the line voltage.

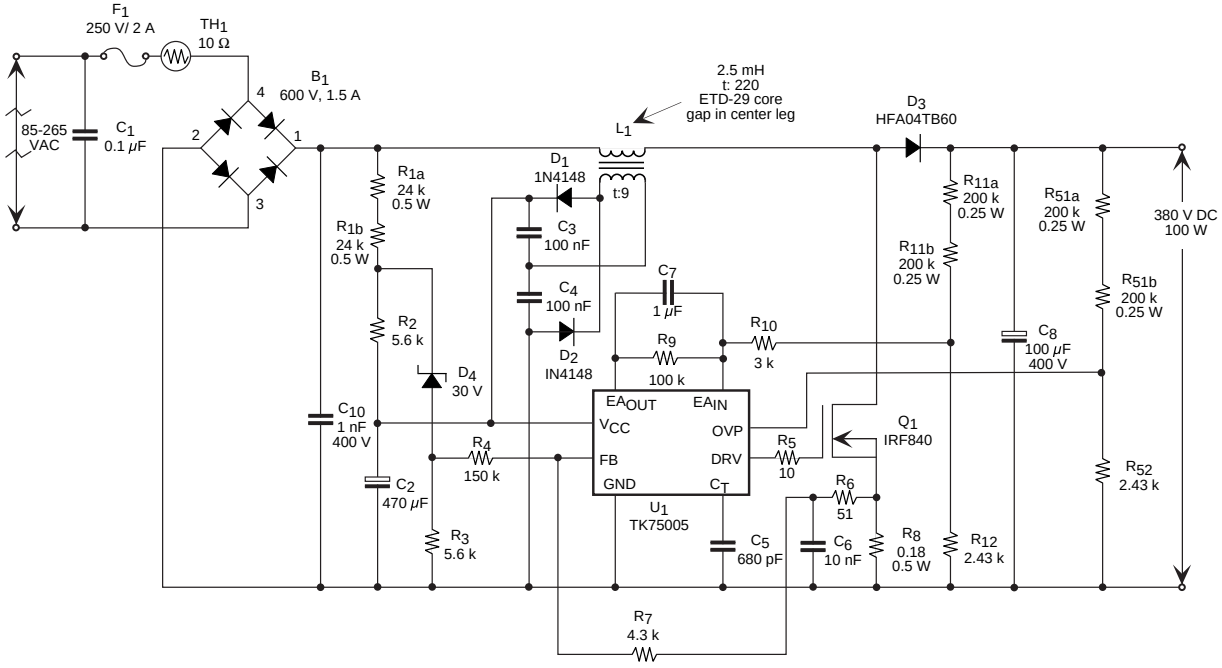


FIGURE 7: BOOST POWER FACTOR CORRECTOR APPLICATION CIRCUIT

PACKAGE OUTLINE

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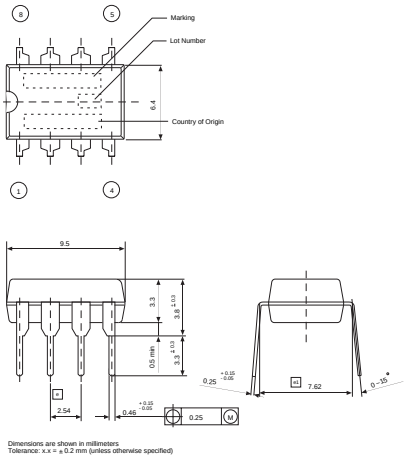

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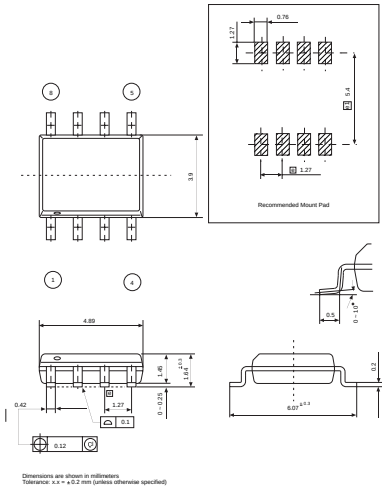

Marking Information

	Marking
TK75005	xxx

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