

# TOSHIBA INTEGRATED CIRCUIT TECHNICAL DATA

## TA7240AP, TA7241AP

TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT  
SILICON MONOLITHIC

Unit in mm

5.8W DUAL AUDIO POWER AMPLIFIER.  
19W BTL AUDIO POWER AMPLIFIER.

The TA7240AP/TA7241AP are dual audio power amplifier for consumer applications. It is designed for high power, low distortion and low noise.

It also contains various kind of protectors.

It is suitable for car-audio power amplifier with high performance.

• Two Kinds of Pin Configuration are Available :  
Normal (TA7240AP) and Reverse (TA7241AP) for Easier Layout Design of Pc-board when Used in BTL-Stereo Application.

• Operating Supply Voltage Range :  $V_{CC(opr)}=9 \sim 18V$

• High Power

$V_{CC}=13.2V, f=1kHz, R_L=4\Omega$

BTL	19W (Typ.)	THD=10%
	15W (Typ.)	THD=1%
DUAL	5.8W (Typ.)	THD=10%

• Low Distortion

$V_{CC}=13.2V, f=1kHz, R_L=4\Omega$

BTL	0.03% (TYP.)	$P_{OUT}=4W, G_V=40dB$
DUAL	0.06% (TYP.)	$P_{OUT}=1W, G_V=52dB$

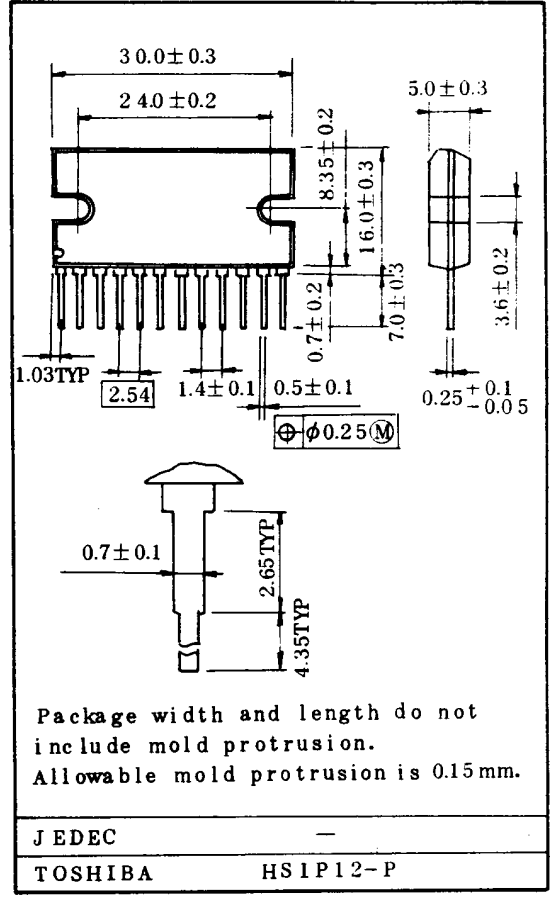
• Low Noise

$V_{CC}=13.2V, R_L=4\Omega$

BTL	0.14mV <sub>rms</sub> (TYP.)	$G_V=40dB, R_g=0, \text{DIN NOISE : DIN 45405}$
DUAL	0.7mV <sub>rms</sub> (TYP.)	$G_V=52dB, R_g=10k\Omega, BW=20Hz \sim 20kHz$

• Protector : Thermal Shut Down, Over Voltage Protection.

BTL-OCL DC Short Protection.



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# TOSHIBA INTEGRATED CIRCUIT

## TECHNICAL DATA

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### MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Peak Supply Voltage (0.2 sec)	VCC surge	45	V
DC Supply Voltage	VCC DC	25	V
Operating Supply Voltage	VCC opr	18	V
Output Current (peak)	IO(peak)	4.5	A
Power Dissipation	PD	25	W
Operating Temperature	Topr	-30 ~ 75	°C
Storage Temperature	Tstg	-55 ~ 150	°C

### ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, VCC=13.2V, RL=4Ω, Rg=600Ω, f=1kHz, Ta=25°C)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent Current		ICCQ	2	VIN=0	-	80	145	mA
BTL CONNECTION MODE	Output Power	POUT(1)	1	THD=10%	16	19	-	W
		POUT(2)	1	THD=1%	12	15	-	W
	Total Harmonic Distortion	THD(1)	1	POUT=4W, Gv=40dB	-	0.03	0.25	%
	Output Offset Voltage	VOFF	1	VIN=0	-	0	0.35	V
	Voltage Gain	Gv(1)	1	VOUT=0dBm	-	40	-	dB
	Output Noise Voltage	VNO(1)	1	Rg=0 DIN45405 Noise Filter	-	0.14	-	mVrms
Ripple Rejection Ratio	R.R(1)	1	fripple=100Hz Vripple=0dBm	-	-52	-40	dB	
DUAL MODE	Output Power	POUT(3)	2	THD=10%	5	5.8	-	W
	Total Harmonic Distortion	THD(2)	2	POUT=1W	-	0.06	0.30	%
	Voltage Gain	Gv(2)	2	VOUT=0dBm	50	52	54	dB
	Voltage Gain Ratio	4Gv	2	VOUT=0dBm	-1	0	1	dB
	Output Noise Voltage	VNO(2)	2	Rg=10kΩ BW=20Hz ~ 20kHz	-	0.7	1.5	mVrms
	Ripple Rejection Ratio	R.R(2)	2	fripple=100Hz Vripple=0dBm	-	-52	-40	dB
	Cross Talk	C.T	2	VOUT=0dBm	-	-57	-	dB
Input Resistance	RIN	2	f=1kHz	-	33	-	kΩ	

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# TOSHIBA INTEGRATED CIRCUIT

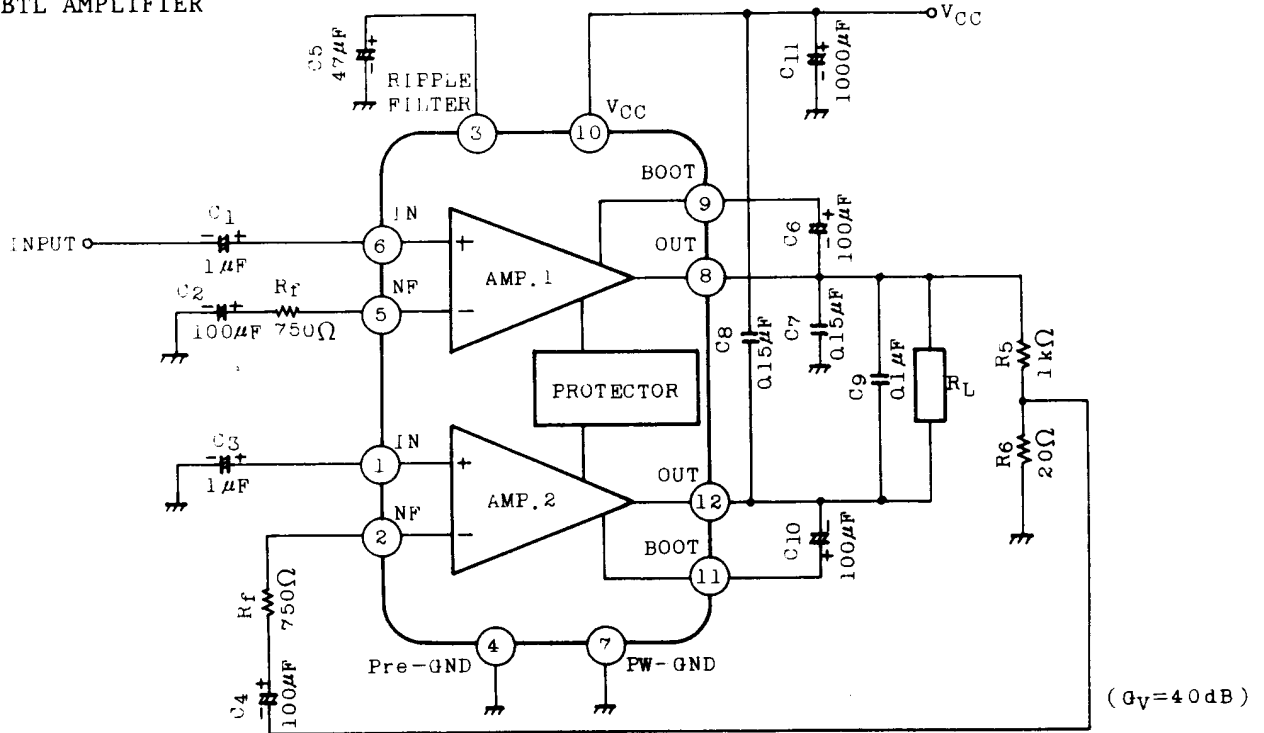
## TECHNICAL DATA

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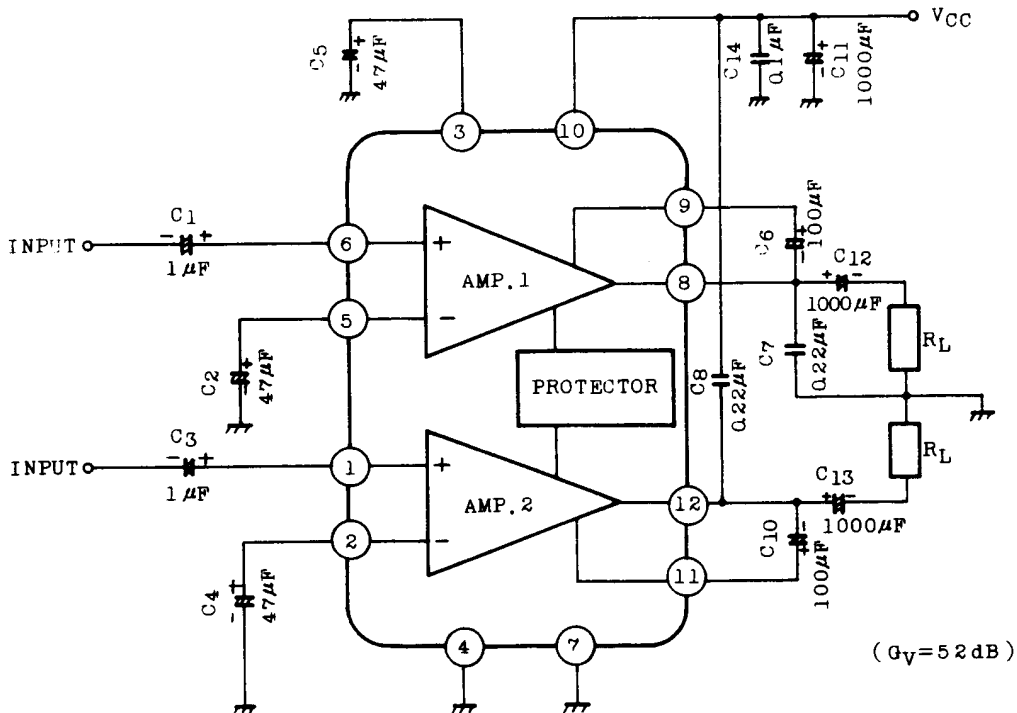
### TEST CIRCUIT/APPLICATION CIRCUIT

TA7240AP

#### (1) BTL AMPLIFIER



#### (2) DUAL AMPLIFIER



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# TOSHIBA INTEGRATED CIRCUIT

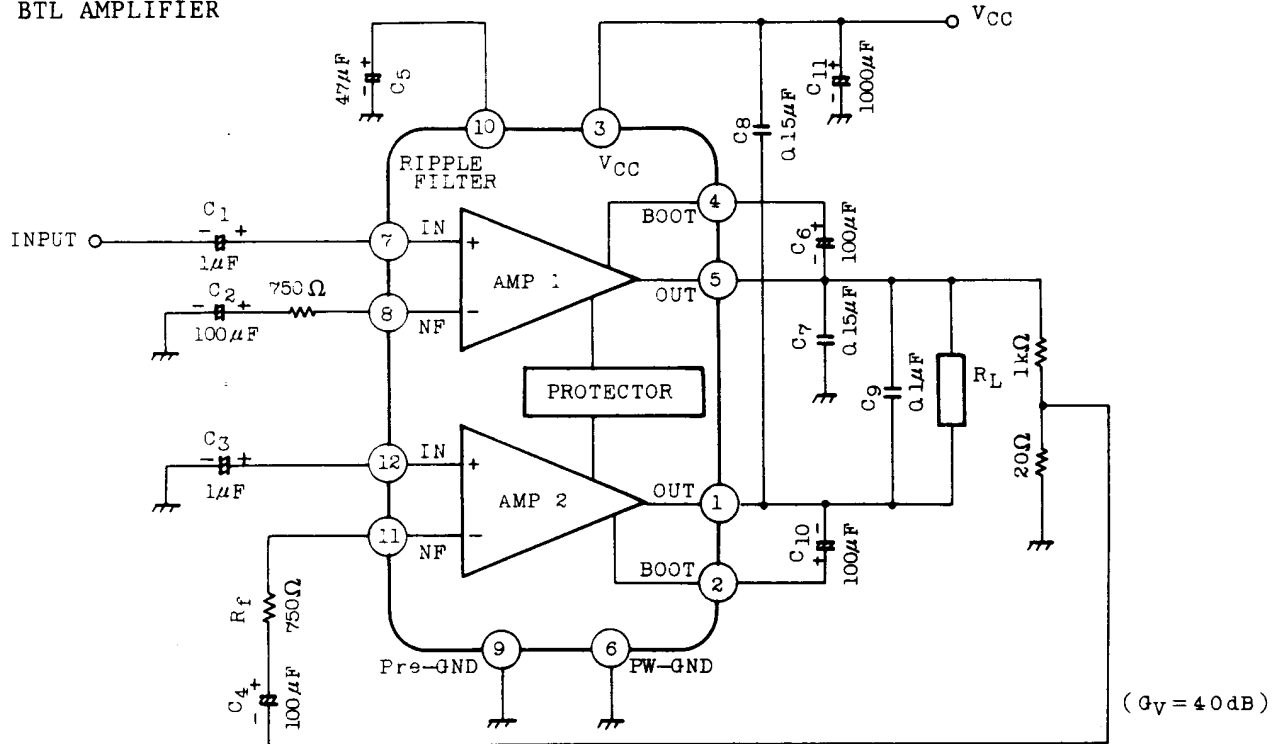
## TECHNICAL DATA

TA7240AP, TA7241AP

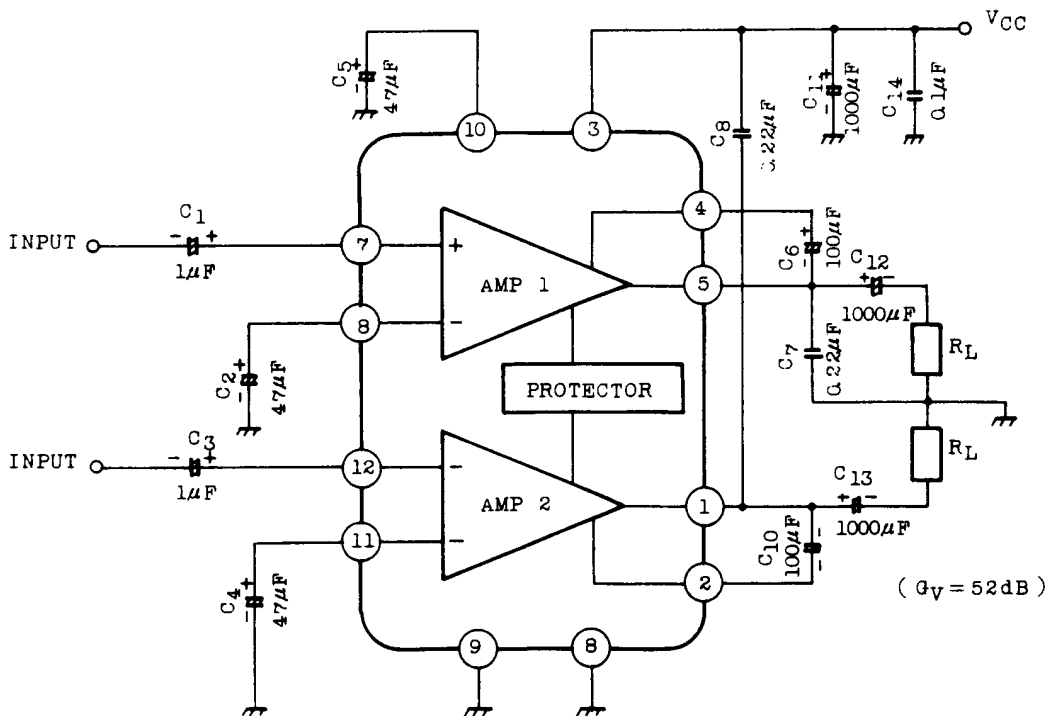
### TEST CIRCUIT/APPLICATION CIRCUIT

TA7241AP

#### (1) BTL AMPLIFIER



#### (2) DUAL AMPLIFIER



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TYPICAL DC VOLTAGE OF EACH TERMINAL

(V<sub>CC</sub>=13.2V, T<sub>a</sub>=25°C, DUAL MODE TEST CIRCUIT)

TERMINAL No.		1	2	3	4	5	6	7	8	9	10	11	12
DC Voltage (V)	TA7240AP	1.5	1.5	4.4	GND	1.5	1.5	GND	6.6	12.7	V <sub>CC</sub>	12.7	6.6
	TA7241AP	6.6	12.7	V <sub>CC</sub>	12.7	6.6	GND	1.5	1.5	GND	4.4	1.5	1.5

APPLICATION INFORMATION

(This explanatory terminal number is for TA7240AP)

1. VOLTAGE GAIN

(1) Dual Mode

The closed loop voltage gain G<sub>v</sub> is determined by R<sub>1</sub>, R<sub>2</sub>, R<sub>3</sub>, R<sub>4</sub> and R<sub>f</sub>.

$$G_v \approx 20 \log \frac{R_2 + R_f + R_1}{R_f + R_1} + 20 \log \frac{R_3 + R_4}{R_4} \text{ (dB)}$$

when R<sub>f</sub>=0, G<sub>v</sub>=52dB(Typ.)

is given.

The recommended voltage gain is more than 40dB.

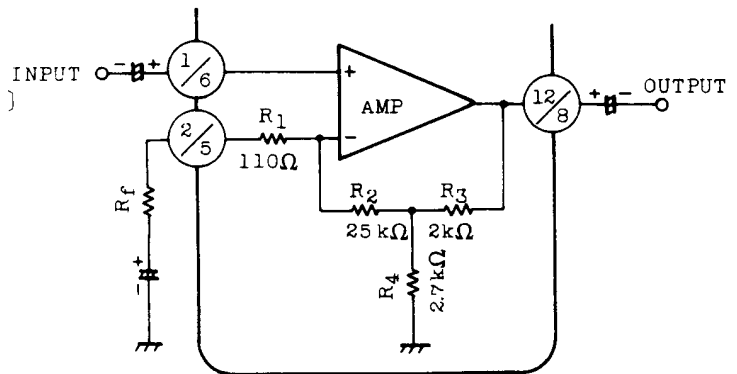


Fig 1

(2) BTL Mode

The recommended BTL connection amplifier is shown in Figure 2.

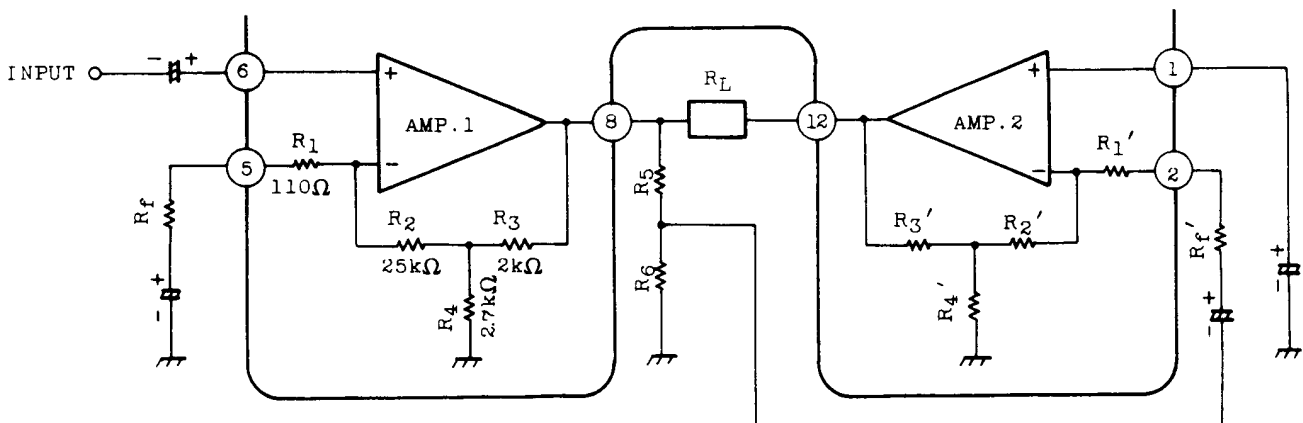


Fig. 2

AMP.1 is noninverting amplifier and AMP.2 is inverting one. The output voltage is divided by resistors R<sub>5</sub> and R<sub>6</sub>.

This divided voltage is applied to inverting input of AMP.2. R<sub>5</sub> and R<sub>6</sub> are determined in the following equation.

$$\frac{R_5+R_6}{R_5} = 20 \log \frac{R_1'+R_f'+R_2'}{R_1'+R_f'} + 20 \log \frac{R_3'+R_4'}{R_4'} \dots G_v \text{ in Dual Mode}$$

The voltage gain in this circuit is 6dB higher than that in dual mode.

$$G_v = 20 \log \frac{R_1+R_f+R_2}{R_1+R_f} + 20 \log \frac{R_3+R_4}{R_4} + 6 \quad [\text{dB}]$$

In case of R<sub>f</sub>=0

$$G_v = 52+6=58[\text{dB}]$$

In case of R<sub>f</sub>=750Ω

$$G_v = 34+6=40[\text{dB}]$$

## 2. MUTING

Audio muting can be accomplished by connecting pin ③ (ripple filter) to GND as shown in Fig.3.

Then, the bias circuits are cut off.

Amount of muting attenuation is more than 60dB.

Precaution in muting operation is as follows.

- (1) The recovery time at muting off depends on Capacitance C<sub>2</sub>, C<sub>4</sub> and C<sub>5</sub> in the test Circuit.
- (2) As this muting system is operated by the short-circuit of ripple filter : C<sub>5</sub>, the ripple rejection ratio becomes worse in a muting mode.  
Note that some "POP-Noise" occur when bias is shut off with mute-on.

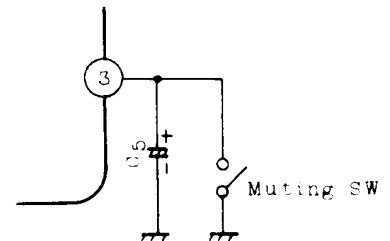


Fig.3

## 3. CAPACITOR C<sub>7</sub>, C<sub>8</sub>

The purpose of capacitor C<sub>7</sub>, C<sub>8</sub> is to prevent oscillation.

These capacitors need to be small temperature coefficient. So celamic capacitor is unsuitabel.

A voltage gain less than 40dB results occasionally in a parastic oscillation.

Stability for parastic oscillation is promoted by connecting capacitor of 500 ~ 1000pF between pin ① and pin ② (pin ⑤ and pin ⑥ ).

The additional capacitors are recommended to be inserted.

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4. PRECAUTION AT PRINT BOARD DESIGN

- (1) Print Pattern board should be designed in consideration of stability for parastic oscillation.

The following parts-layout is recommended.

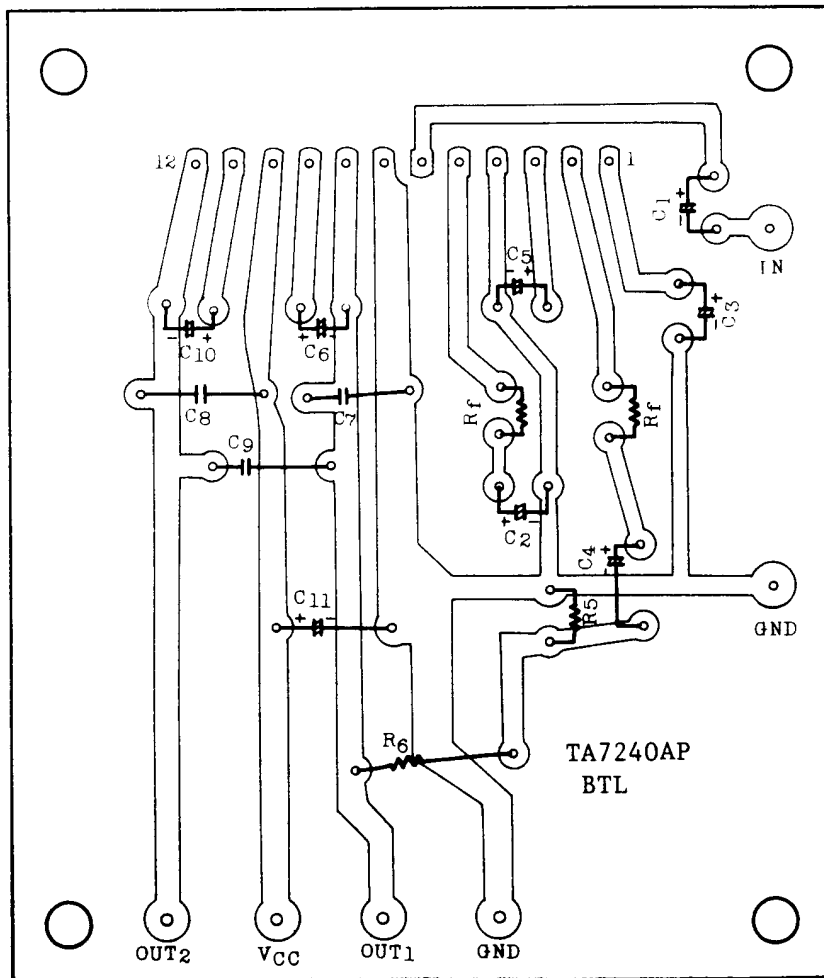
- 1st. Capacitors C6 and C10 are spaced most close to the output pin.
  - 2nd. Capacitor C7 or C8 is spaced close to the output pin next to C6 and C10.
  - 3rd. Capacitor C9 is spaced close to it next to C7 and C8.
  - 4th. Capacitor C11 is spaced close to it next to C9.
- (2) Input line (pin ⑥) and PW-GND line (pin ⑦) should not be spaced in parallel. In the paralld layout, output current signal in PW-GND line is bed back to input line by electromagnetic coupling. Then it deteriorates the total harmonic distortion, especially at high audio frequency region.
- (3) Undesirable terminating of capacitors deteriorates "pop" noise or THD. Capacitors C2, C4 and C5 should be terminated to Pre-GND (pin ④). Capacitors C7, C11, and C14 should be terminated to PW-GND (pin ⑦).
- (4) It is recommended to refer the standard print board.

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TECHNICAL DATA

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STANDARD P.C.B

(TA7240AP BTL AMPLIFIER)



BOTTOM VIEW

TA7240AP-8

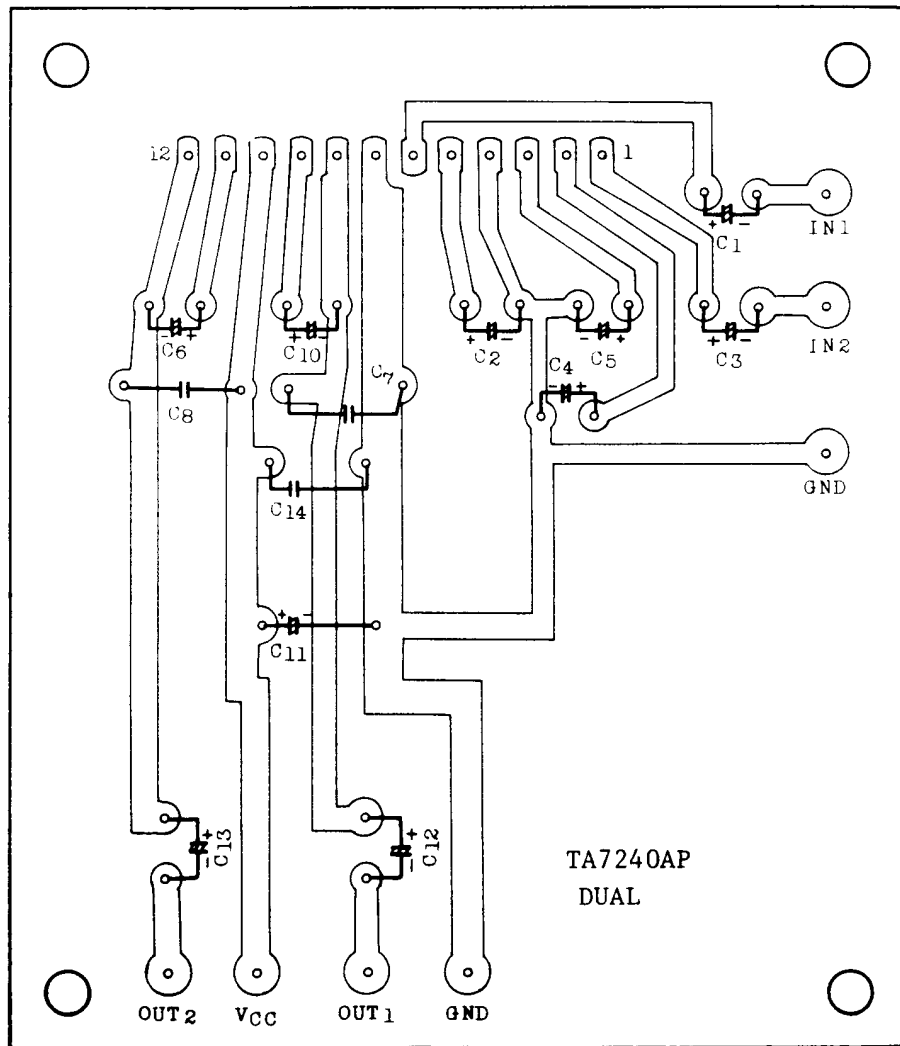
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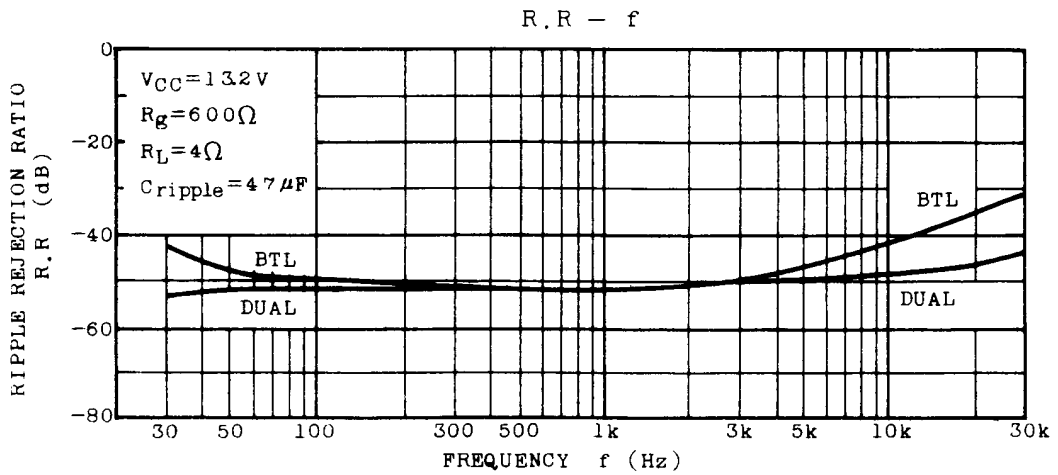
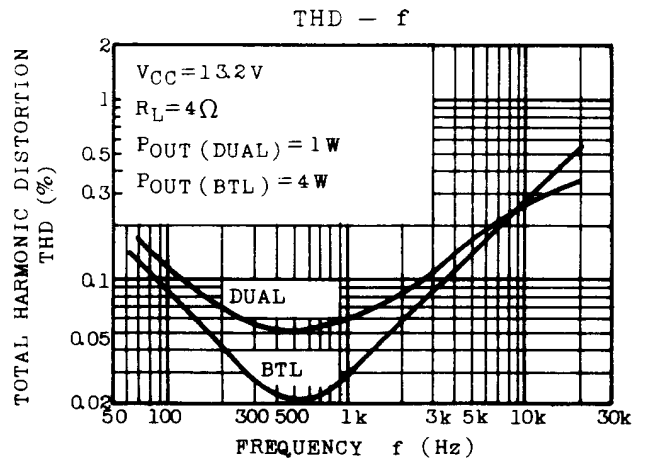
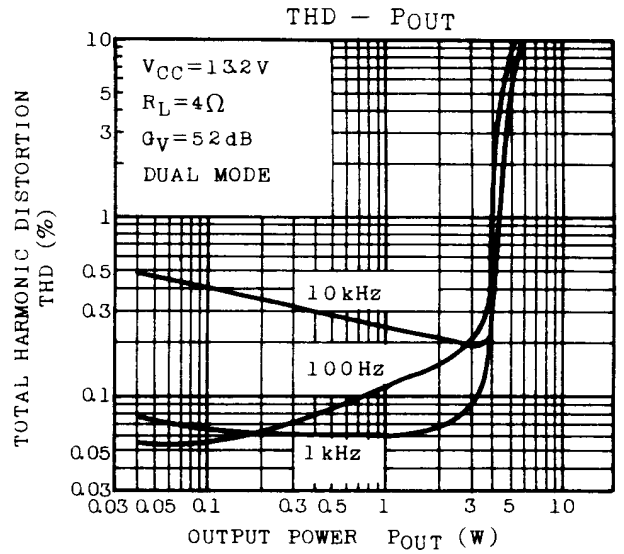
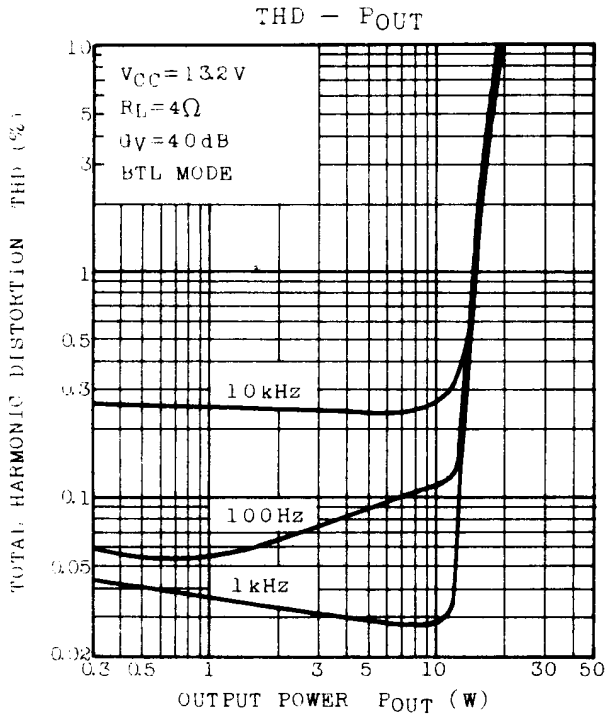
STANDARD P.C.B

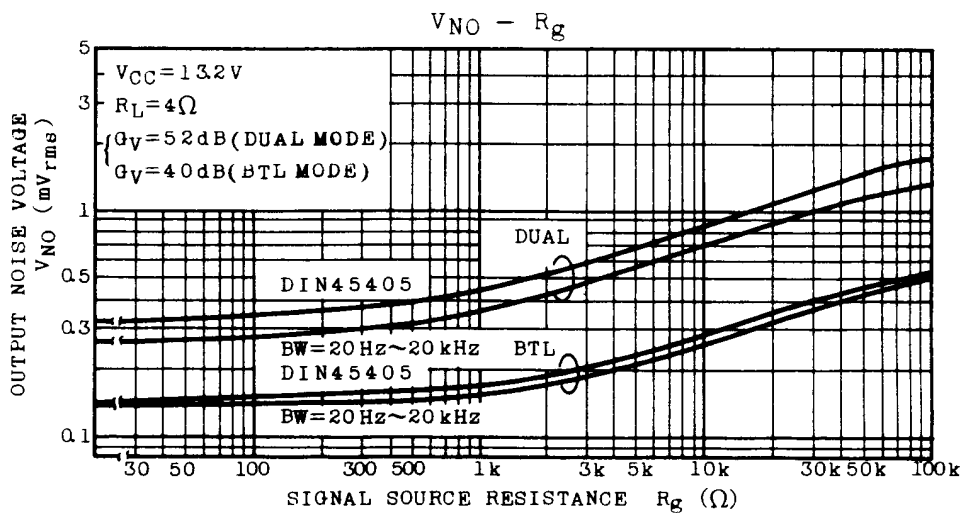
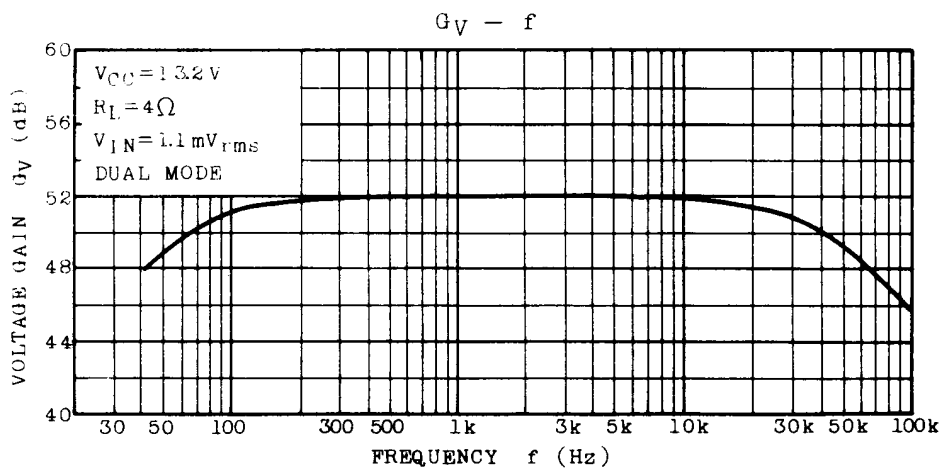
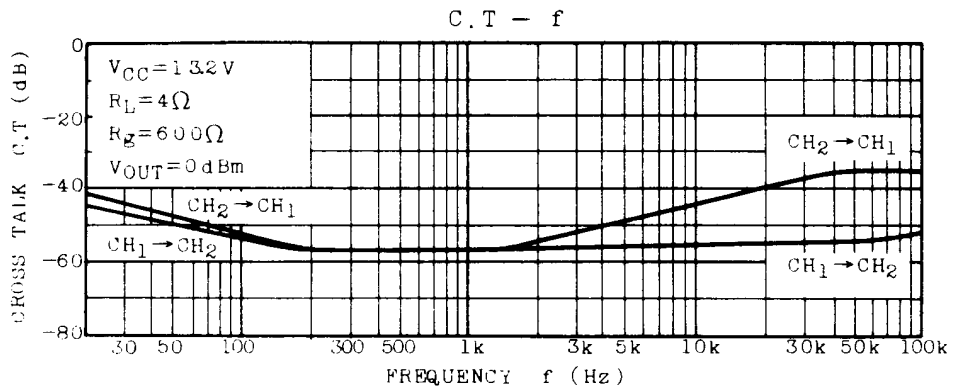
(TA7240AP DUAL AMPLIFIER)



BOTTOM VIEW

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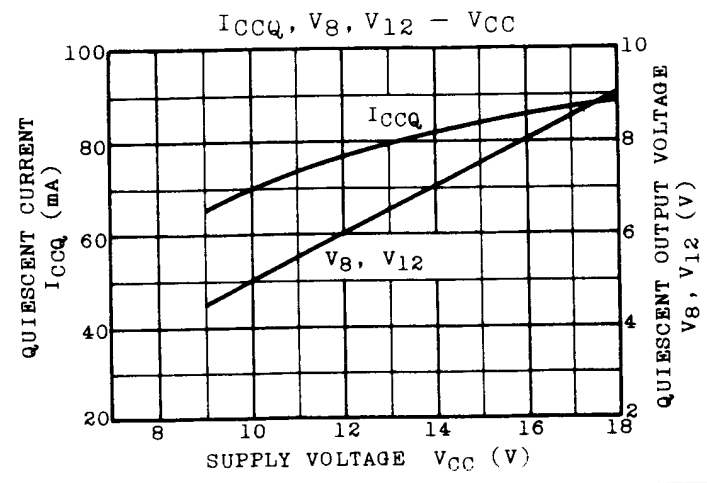
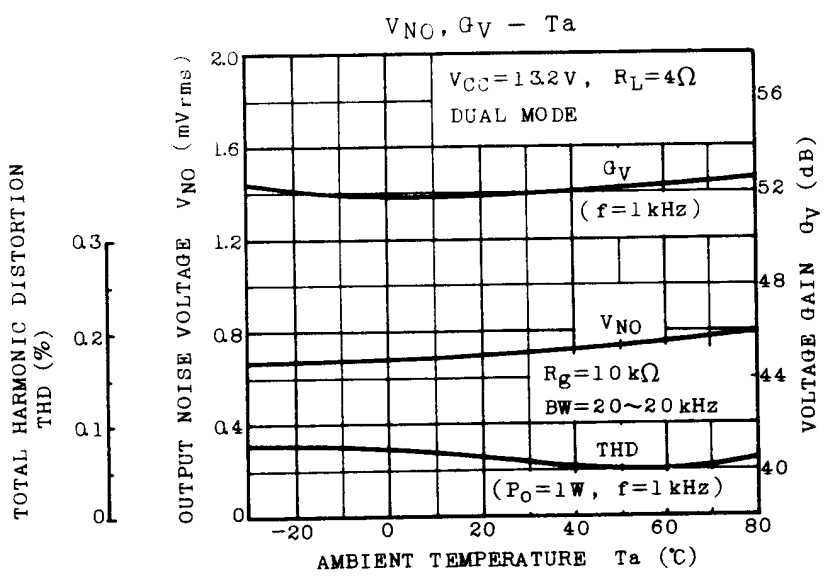
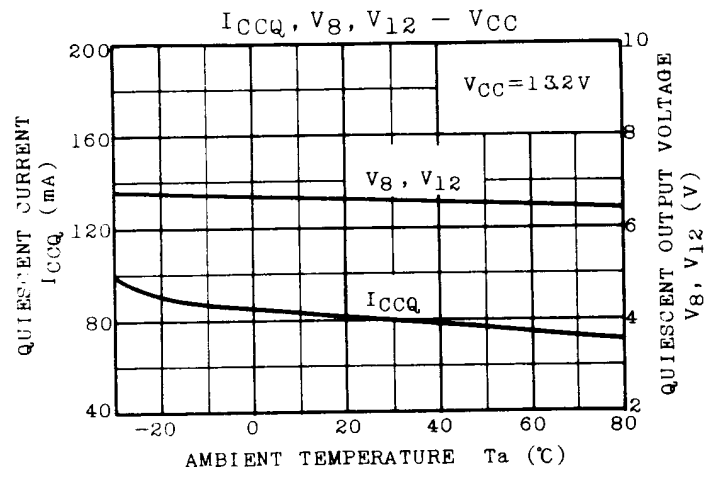




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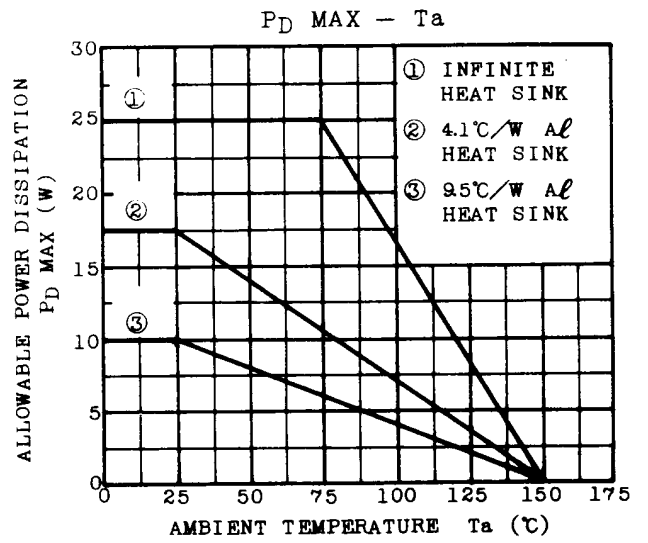
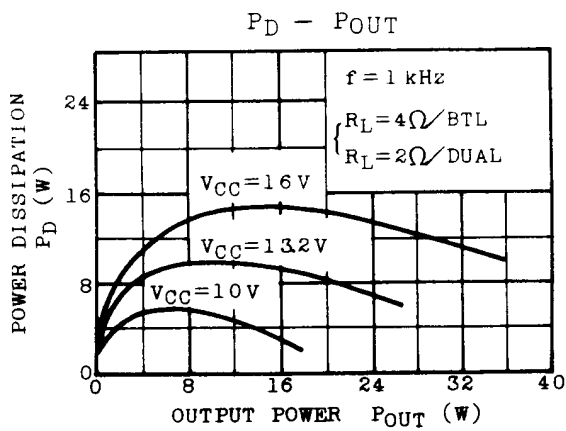
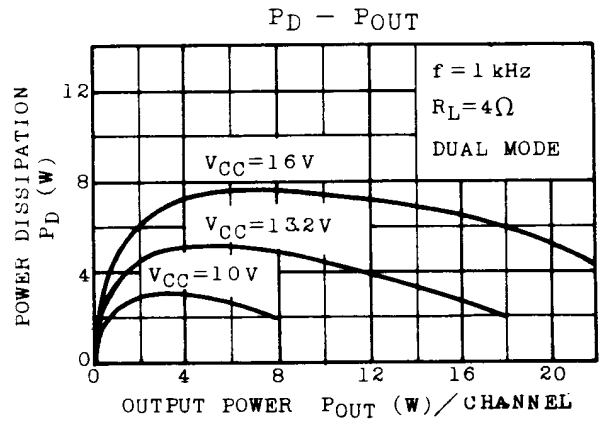
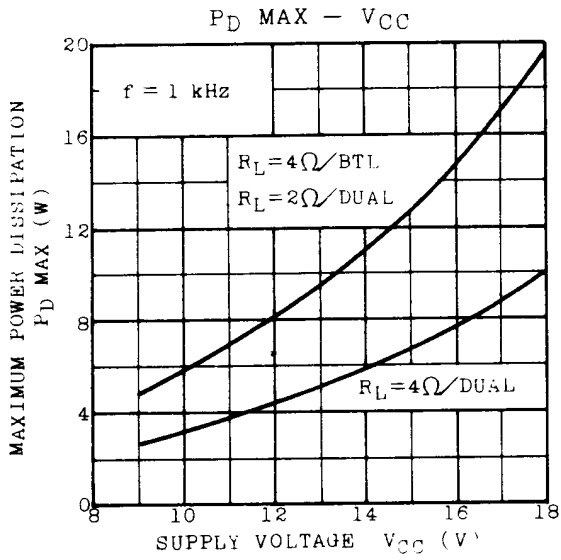
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