TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

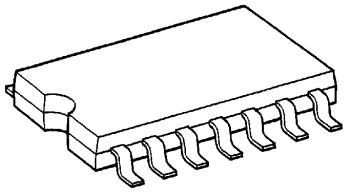
TC74LVX74F, TC74LVX74FN, TC74LVX74FT

DUAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR

The TC74LVX74 is a high speed CMOS D-FLIP FLOP fabricated with silicon gate C^2MOS technology.
Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. This device is suitable for low voltage and battery operated systems.
The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CK pulse.
$\overline{CLR}$ and $\overline{PR}$ are independent of the CK and are accomplished by setting the appropriate input low.
An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

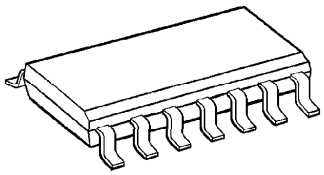
(Note) The JEDEC SOP (FN) is not available in Japan.

TC74LVX74F



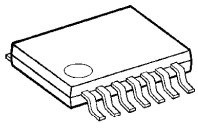
SOP14-P-300-1.27

TC74LVX74FN



SOL14-P-150-1.27

TC74LVX74FT



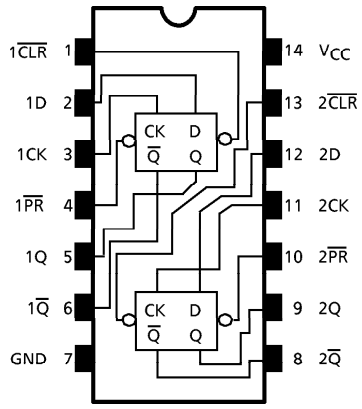
TSSOP14-P-0044-0.65

Weight
SOP14-P-300-1.27 : 0.18g (Typ.)
SOL14-P-150-1.27 : 0.12g (Typ.)
TSSOP14-P-0044-0.65 : 0.06g (Typ.)

FEATURES

- High speed : f_{MAX} = 145MHz (Typ.) (V_{CC} = 3.3V)
- Low power dissipation : I_{CC} = 2μA (Max.) (Ta = 25°C)
- Input voltage level : V_{IL} = 0.8V (Max.) (V_{CC} = 3V)
  V_{IH} = 2.0V (Min.) (V_{CC} = 3V)
- Power down protection is provided on all inputs.
- Balanced propagation delays : $t_{pLH} \simeq t_{pHL}$
- Pin and function compatible with 74HC74

PIN ASSIGNMENT



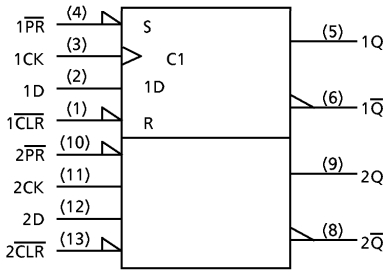
(TOP VIEW)

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	X	↓	Q_n	$\overline{Q}_n$	NO CHANGE

X : Dont't care

IEC LOGIC SYMBOL



MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC} / Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise And Fall Time	dt / dv	0~100	ns / V

ELECTRICAL CHARACTERISTICS

DC characteristics

PARAMETER		SYM-BOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
Input Voltage	"H" Level	V_{IH}			2.0	1.5	—	—	1.5	—	V
					3.0	2.0	—	—	2.0	—	
					3.6	2.4	—	—	2.4	—	
	"L" Level	V_{IL}			2.0	—	—	0.5	—	0.5	
					3.0	—	—	0.8	—	0.8	
					3.6	—	—	0.8	—	0.8	
Output Voltage	"H" Level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	2.0	1.9	2.0	—	1.9	—	V
				I_{OH} = −50μA	3.0	2.9	3.0	—	2.9	—	
				I_{OH} = −4mA	3.0	2.58	—	—	2.48	—	
	"L" Level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	2.0	—	0.0	0.1	—	0.1	
				I_{OL} = 50μA	3.0	—	0.0	0.1	—	0.1	
				I_{OL} = 4mA	3.0	—	—	0.36	—	0.44	
Input Leakage Current		I_{IN}	V_{IN} = 5.5V or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current		I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	2.0	—	20.0	μA

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYM-BOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C LIMIT	Ta = −40~85°C LIMIT	UNIT
Minimum Pulse Width (CK)	t_{W} (L)		2.7	8.5	10.0	ns
	t_{W} (H)		3.3±0.3	6.0	7.0	
Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	t_{W} (L)		2.7	8.5	10.0	ns
			3.3±0.3	6.0	7.0	
Minimum Set-up Time	t_s		2.7	8.0	9.5	ns
			3.3±0.3	5.5	6.5	
Minimum Hold Time	t_h		2.7	0.5	0.5	ns
			3.3±0.3	0.5	0.5	
Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	t_{rem}		2.7	6.5	7.5	ns
			3.3±0.3	5.0	5.0	

AC characteristics (Input $t_r = t_f = 3ns$)

PARAMETER	SYM-BOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	C_L (pF)	MIN.	TYP.	MAX.	MIN.	MAX	
Propagation Delay Time (CK-Q, $\overline{Q}$)	t_{pLH}		2.7	15	—	7.3	15.0	1.0	18.5	ns
				50	—	9.8	18.5	1.0	22.0	
	t_{pHL}		3.3 ± 0.3	15	—	5.7	9.7	1.0	11.5	
				50	—	8.2	13.2	1.0	15.0	
Propagation Delay Time ($\overline{CLR}$, $\overline{PR}$-Q, $\overline{Q}$)	t_{pLH}		2.7	15	—	8.4	15.6	1.0	18.5	ns
				50	—	10.9	19.1	1.0	22.0	
	t_{pHL}		3.3 ± 0.3	15	—	6.6	10.1	1.0	12.0	
				50	—	9.1	13.6	1.0	15.5	
Maximum Clock Frequency	f_{MAX}		2.7	15	55	135	—	50	—	MHz
				50	45	60	—	40	—	
			3.3 ± 0.3	15	95	145	—	80	—	
				50	60	85	—	50	—	
Output To Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7	50	—	—	1.5	—	1.5	ns
			3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input Capacitance	C_{IN}	(Note 2)			—	4	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)			—	25	—	—	—	pF

(Note 1) Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

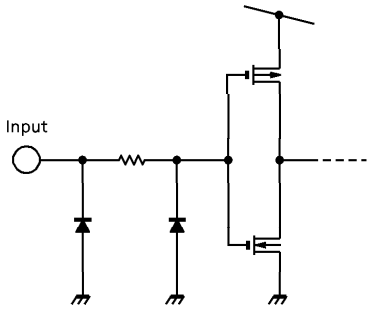
(Note 2) Parameter guaranteed by design.

(Note 3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.
Average operating current can be obtained by the equation :
$I_{CC\,(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2$ (per F / F)

Noise characteristics (Ta = 25°C, Input $t_r = t_f = 3ns$, $C_L = 50pF$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP.	LIMIT	UNIT
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.3	0.5	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	−0.3	−0.5	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	—	0.8	V

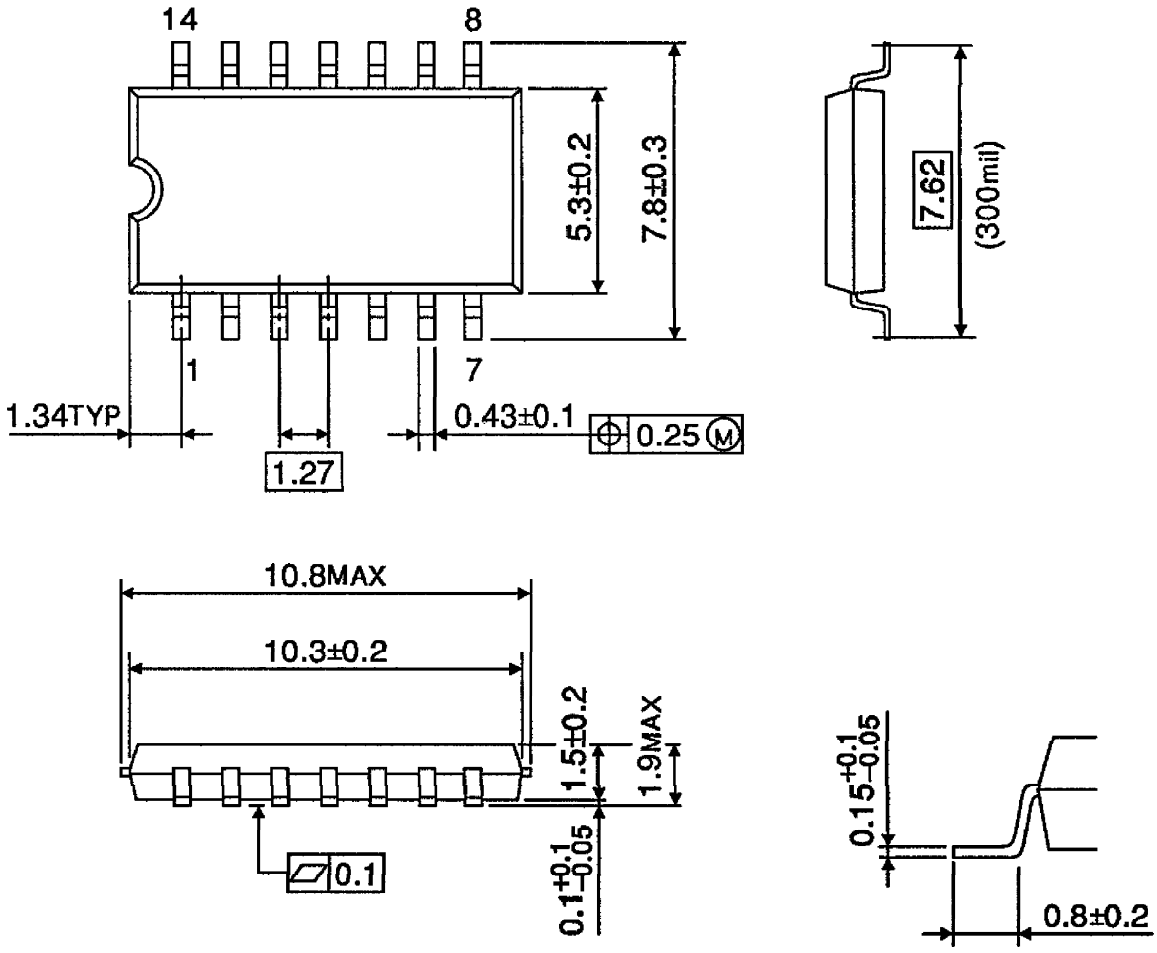
INPUT EQUIVALENT CIRCUIT



OUTLINE DRAWING

SOP14-P-300-1.27

Unit : mm



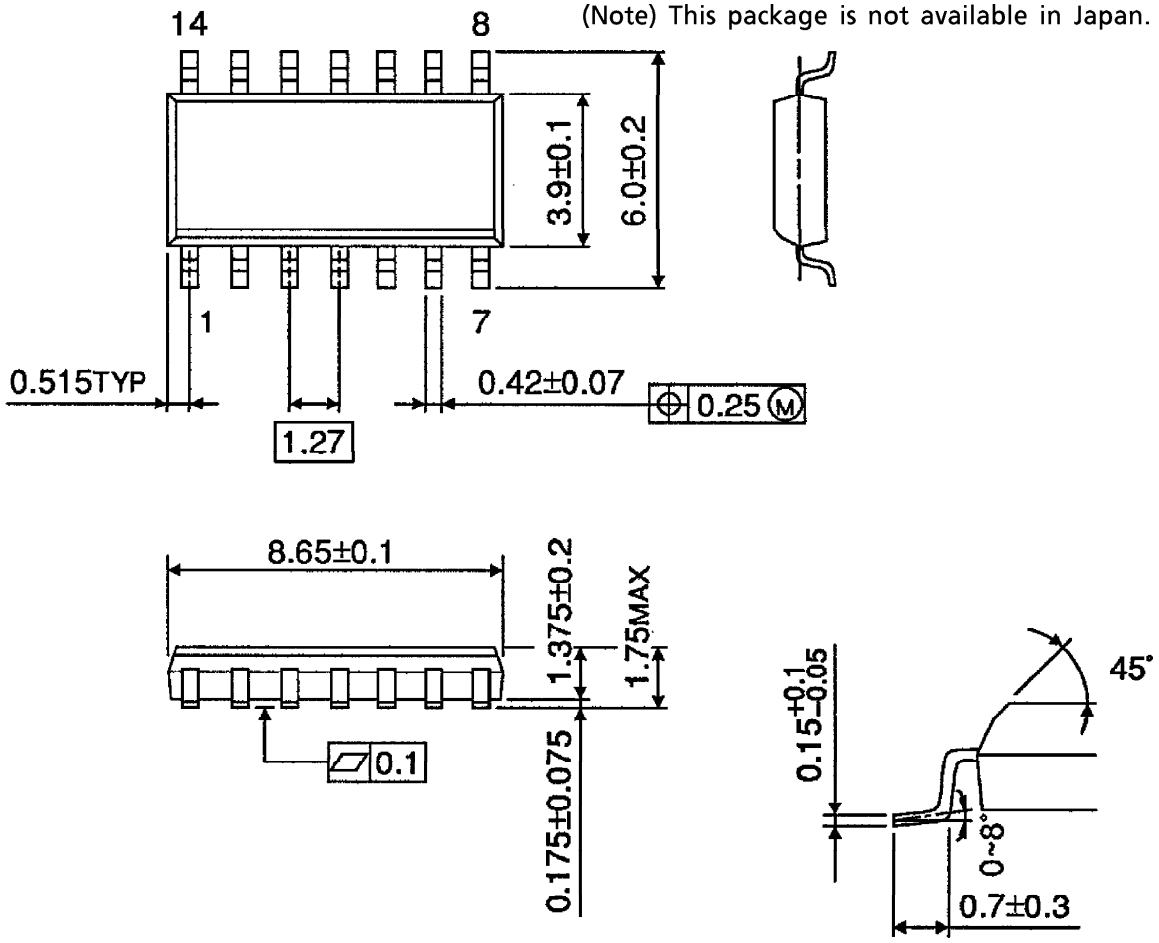
Weight : 0.18g (Typ.)

OUTLINE DRAWING

SOL14-P-150-1.27

Unit : mm

(Note) This package is not available in Japan.

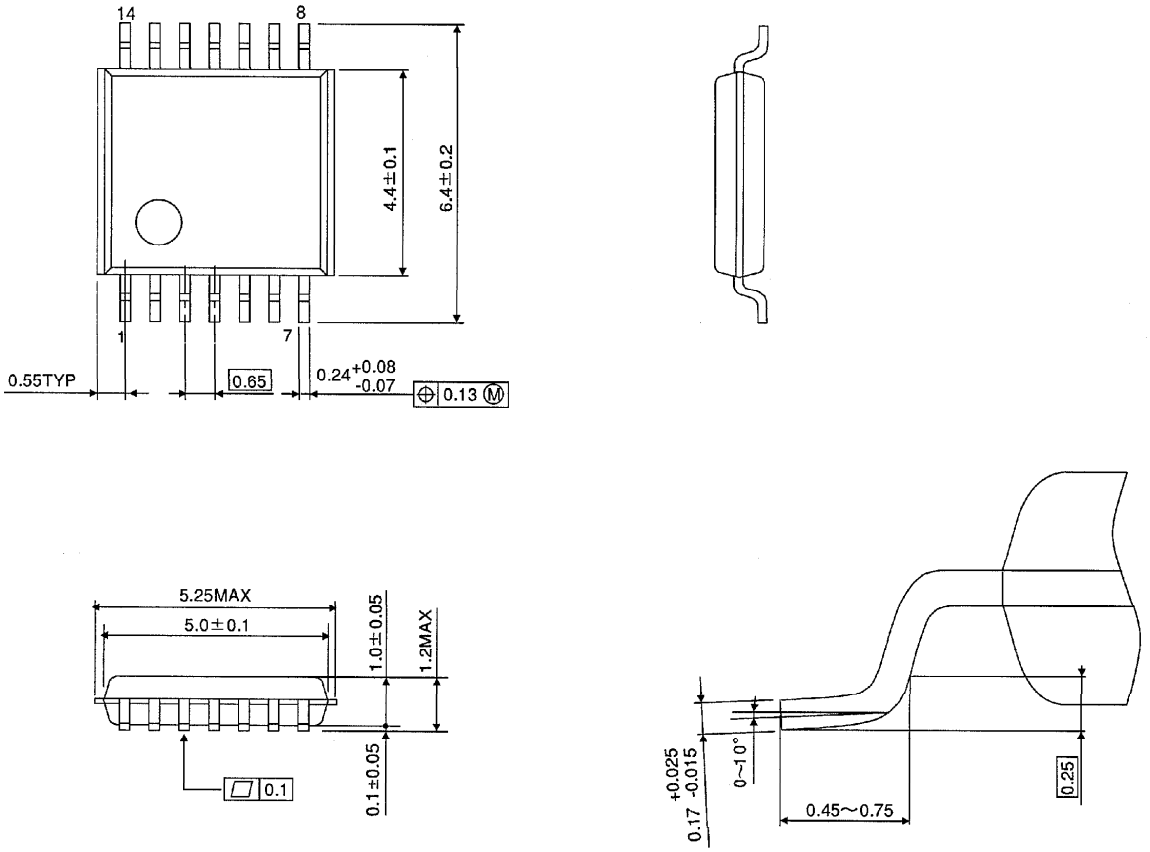


Weight : 0.12g (Typ.)

OUTLINE DRAWING

TSSOP14-P-0044-0.65

Unit : mm



Weight : 0.06g (Typ.)