

TC74LVX74F, TC74LVX74FN, TC74LVX74FT

DUAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR

The TC74LVX74 is a high speed CMOS D-FLIP FLOP fabricated with silicon gate C²MOS technology. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. This device is suitable for low voltage and battery operated systems.

The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CK pulse.

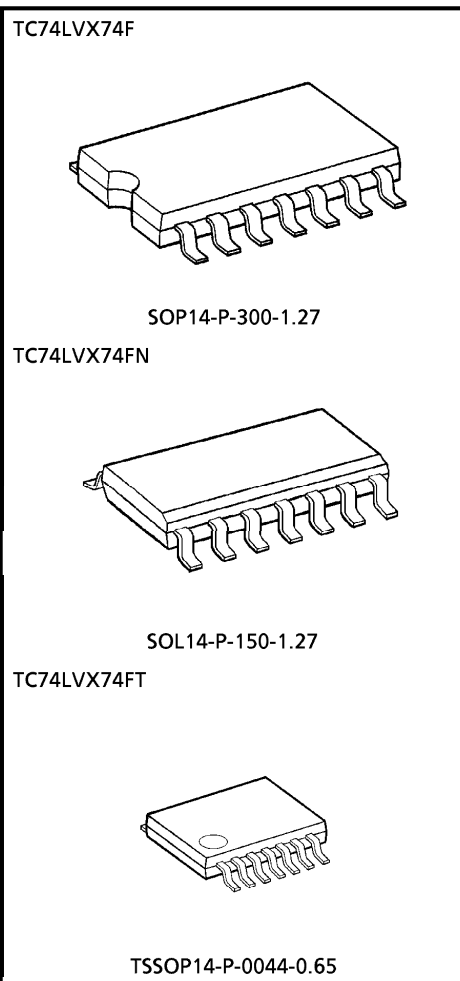
\overline{CLR} and \overline{PR} are independent of the CK and are accomplished by setting the appropriate input low.

An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES

- High speed : $f_{MAX} = 145\text{MHz}$ (Typ.) ($V_{CC} = 3.3\text{V}$)
- Low power dissipation : $I_{CC} = 2\mu\text{A}$ (Max.) ($T_a = 25^\circ\text{C}$)
- Input voltage level : $V_{IL} = 0.8\text{V}$ (Max.) ($V_{CC} = 3\text{V}$)
 $V_{IH} = 2.0\text{V}$ (Min.) ($V_{CC} = 3\text{V}$)
- Power down protection is provided on all inputs.
- Balanced propagation delays : $t_{pLH} \approx t_{pHL}$
- Pin and function compatible with 74HC74

(Note) The JEDEC SOP (FN) is not available in Japan.



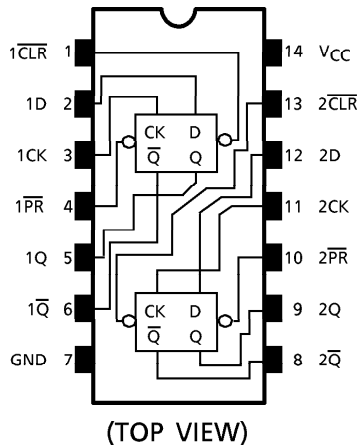
Weight

SOP14-P-300-1.27	: 0.18g (Typ.)
SOL14-P-150-1.27	: 0.12g (Typ.)
TSSOP14-P-0044-0.65	: 0.06g (Typ.)

961001EBA2

● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

PIN ASSIGNMENT

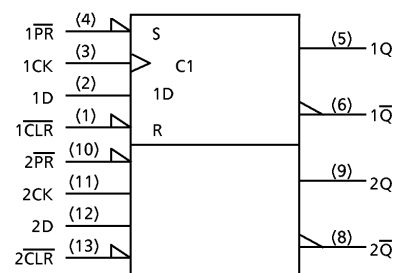


TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
CLR	PR	D	CK	Q	Q̄	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	—
H	H	L		L	H	—
H	H	H		H	L	—
H	H	X		Q _n	Q̄ _n	NO CHANGE

X : Don't care

IEC LOGIC SYMBOL



MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	V _{CC}	-0.5~7.0	V
DC Input Voltage	V _{IN}	-0.5~7.0	V
DC Output Voltage	V _{OUT}	-0.5~V _{CC} +0.5	V
Input Diode Current	I _{IK}	-20	mA
Output Diode Current	I _{OK}	±20	mA
DC Output Current	I _{OUT}	±25	mA
DC V _{CC} / Ground Current	I _{CC}	±50	mA
Power Dissipation	P _D	180	mW
Storage Temperature	T _{stg}	-65~150	°C

961001EBA2'

- The products described in this document are subject to foreign exchange and foreign trade control laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V _{CC}	2.0~3.6	V
Input Voltage	V _{IN}	0~5.5	V
Output Voltage	V _{OUT}	0~V _{CC}	V
Operating Temperature	T _{opr}	-40~85	°C
Input Rise And Fall Time	dt/dv	0~100	ns/V

ELECTRICAL CHARACTERISTICS

DC characteristics

PARAMETER	SYM-BOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT				
				MIN.	TYP.	MAX.	MIN.	MAX.					
Input Voltage	"H" Level		V _{IH}	2.0	1.5	—	—	1.5	—	V			
				3.0	2.0	—	—	2.0	—				
				3.6	2.4	—	—	2.4	—				
	"L" Level			V _{IL}	2.0	—	—	0.5	—		0.5		
					3.0	—	—	0.8	—		0.8		
					3.6	—	—	0.8	—		0.8		
Output Voltage	"H" Level	V _{IN} = V _{IH} or V _{IL}	V _{OH}		I _{OH} = -50 μA	2.0	1.9	2.0	—	1.9	—	V	
					I _{OH} = -50 μA	3.0	2.9	3.0	—	2.9	—		
					I _{OH} = -4mA	3.0	2.58	—	—	2.48	—		
	"L" Level			V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA	2.0	—	0.0	0.1	—		0.1
						I _{OL} = 50 μA	3.0	—	0.0	0.1	—		0.1
						I _{OL} = 4mA	3.0	—	—	0.36	—		0.44
Input Leakage Current	I _{IN}	V _{IN} = 5.5V or GND	3.6			—	—	±0.1	—	±1.0	μA		
Quiescent Supply Current	I _{CC}	V _{IN} = V _{CC} or GND	3.6			—	—	2.0	—	20.0	μA		

TIMING REQUIREMENTS (Input t_r = t_f = 3ns)

PARAMETER	SYM-BOL	TEST CONDITION	V _{CC} (V)	Ta = 25°C	Ta = -40~85°C	UNIT
				LIMIT	LIMIT	
Minimum Pulse Width (CK)	t _W (L) t _W (H)		2.7 3.3 ± 0.3	8.5	10.0	ns
				6.0	7.0	
Minimum Pulse Width (CLR, PR)	t _W (L)		2.7 3.3 ± 0.3	8.5	10.0	ns
				6.0	7.0	
Minimum Set-up Time	t _s		2.7 3.3 ± 0.3	8.0	9.5	ns
				5.5	6.5	
Minimum Hold Time	t _h		2.7 3.3 ± 0.3	0.5	0.5	ns
				0.5	0.5	
Minimum Removal Time (CLR, PR)	t _{rem}		2.7 3.3 ± 0.3	6.5	7.5	ns
				5.0	5.0	

AC characteristics (Input $t_r = t_f = 3ns$)

PARAMETER	SYM-BOL	TEST CONDITION			Ta = 25°C			Ta = -40~85°C		UNIT
			V _{CC} (V)	C _L (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time (CK-Q, \bar{Q})	t _{pLH}		2.7	15	—	7.3	15.0	1.0	18.5	ns
				50	—	9.8	18.5	1.0	22.0	
	3.3 ± 0.3		15	—	5.7	9.7	1.0	11.5		
			50	—	8.2	13.2	1.0	15.0		
Propagation Delay Time (\bar{CLR} , \bar{PR} -Q, \bar{Q})	t _{pLH}		2.7	15	—	8.4	15.6	1.0	18.5	ns
				50	—	10.9	19.1	1.0	22.0	
	3.3 ± 0.3		15	—	6.6	10.1	1.0	12.0		
			50	—	9.1	13.6	1.0	15.5		
Maximum Clock Frequency	f _{MAX}		2.7	15	55	135	—	50	—	MHz
				50	45	60	—	40	—	
			3.3 ± 0.3	15	95	145	—	80	—	
				50	60	85	—	50	—	
Output To Output Skew	t _{osLH}	(Note 1)	2.7	50	—	—	1.5	—	1.5	ns
	t _{osHL}			50	—	—	1.5	—	1.5	
Input Capacitance	C _{IN}	(Note 2)			—	4	10	—	10	pF
Power Dissipation Capacitance	C _{PD}	(Note 3)			—	25	—	—	—	pF

(Note 1) Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

(Note 2) Parameter guaranteed by design.

(Note 3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

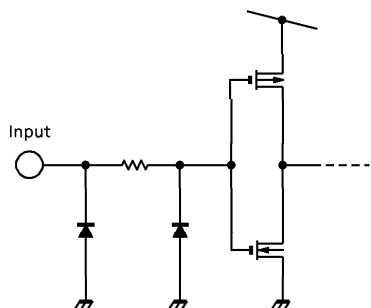
Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per F/F)}$$

Noise characteristics (Ta = 25°C, Input $t_r = t_f = 3ns$, C_L = 50pF)

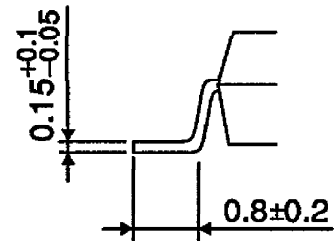
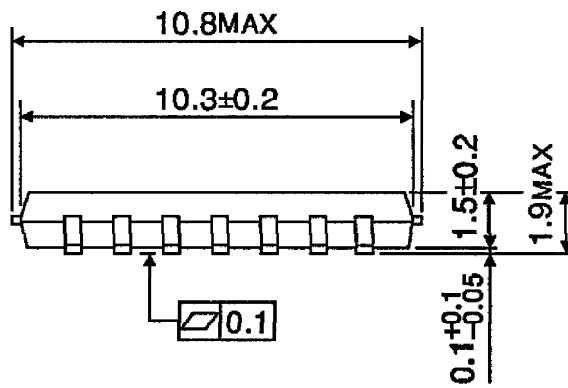
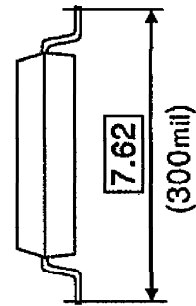
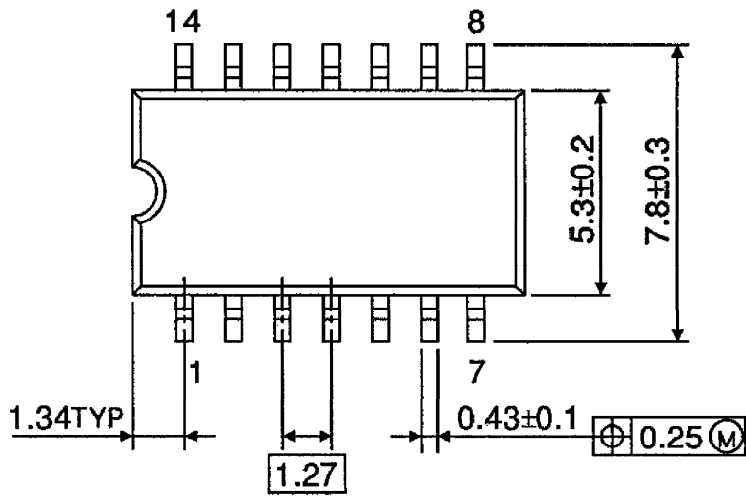
PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	TYP.	LIMIT	UNIT
Quiet Output Maximum Dynamic	V _{OLP}		3.3	0.3	0.5	V
V _{OL}						
Quiet Output Minimum Dynamic	V _{OLV}		3.3	-0.3	-0.5	V
V _{OL}						
Minimum High Level Dynamic Input Voltage	V _{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V _{I LD}		3.3	—	0.8	V

INPUT EQUIVALENT CIRCUIT



OUTLINE DRAWING
SOP14-P-300-1.27

Unit : mm

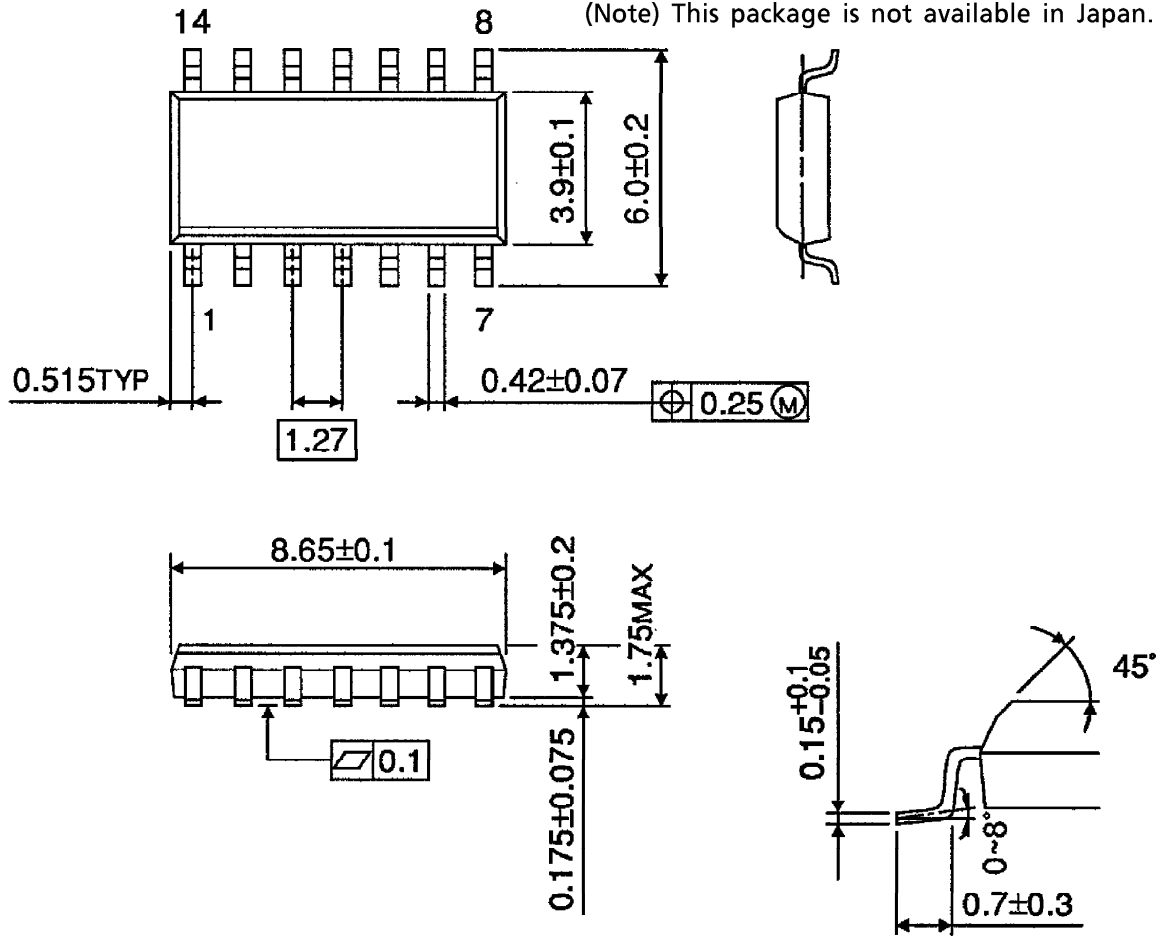


Weight : 0.18g (Typ.)

OUTLINE DRAWING
SOL14-P-150-1.27

Unit : mm

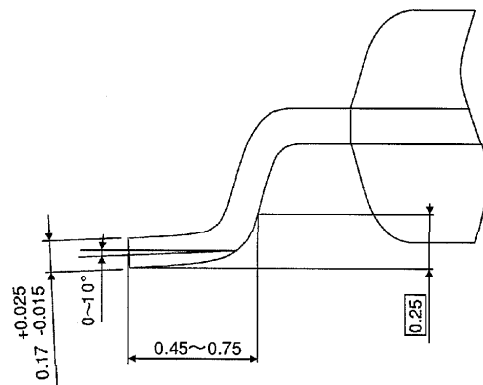
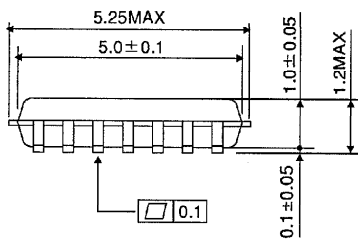
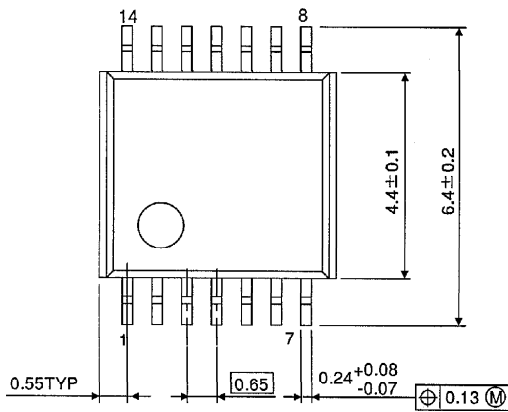
(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)

OUTLINE DRAWING
TSSOP14-P-0044-0.65

Unit : mm



Weight : 0.06g (Typ.)