

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

**TC74VHC161F, TC74VHC161FN, TC74VHC161FT
TC74VHC163F, TC74VHC163FN, TC74VHC163FT**

SYNCHRONOUS PRESETTABLE 4 - BIT COUNTER

TC74VHC161F / FN / FT **BINARY, ASYNCHRONOUS CLEAR**
TC74VHC163F / FN / FT **BINARY, SYNCHRONOUS CLEAR**

(Note) The JEDEC SOP (FN) is not available in Japan.

The TC74VHC 161 and 163 are advanced high speed CMOS SYNCHRONOUS PRESETTABLE 4 BIT BINARY COUNTERS fabricated with silicon gate C²MOS technology. They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The CK input is active on the rising edge. Both $\overline{\text{LOAD}}$ and $\overline{\text{CLR}}$ inputs are active on low logic level.

Presetting of each IC's is synchronous to the rising edge of CK.

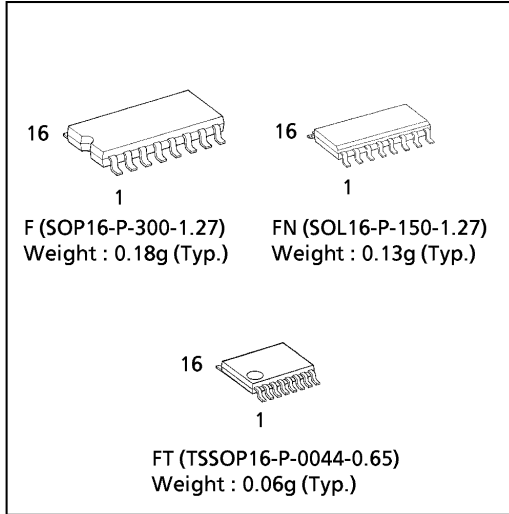
The clear function of the TC74VHC163 is synchronous to CK, while the TC74VHC161 are cleared asynchronously.

Two enable inputs (ENP and ENT) and CARRY OUTPUT are provided to enable easy cascading of counters, which facilitates easy implementation of n - bit counters without using external gates.

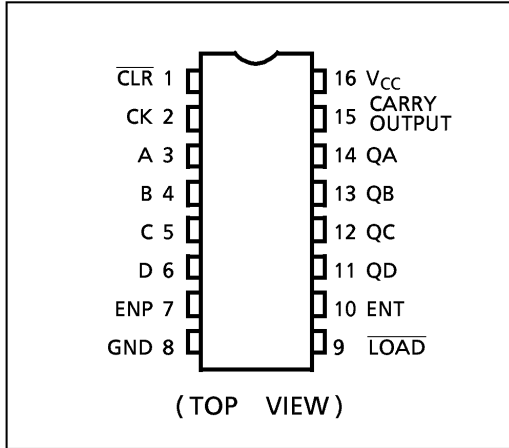
An input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES :

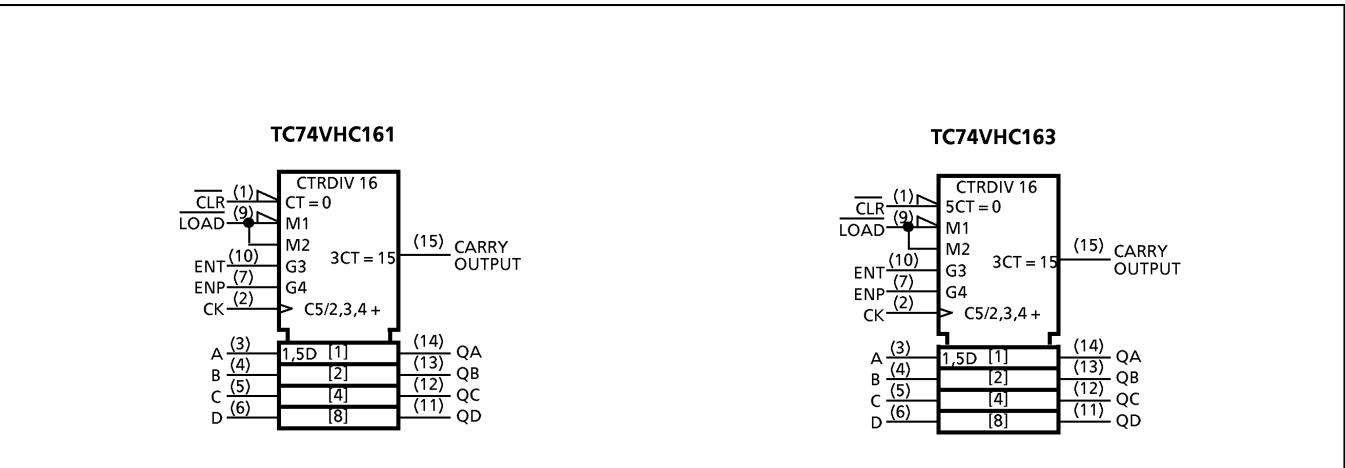
- High Speed $f_{\text{MAX}} = 185\text{MHz (typ.)}$ at $V_{\text{CC}} = 5\text{V}$
- Low Power Dissipation $I_{\text{CC}} = 4\mu\text{A(Max.)}$ at $T_a = 25^\circ\text{C}$
- High Noise Immunity $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}}$ (Min.)
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays... $t_{\text{PLH}} \approx t_{\text{PHL}}$
- Wide Operating Voltage Range... $V_{\text{CC}} (\text{opr}) = 2\text{V} \sim 5.5\text{V}$
- Low Noise $V_{\text{OLP}} = 0.8\text{V (Max.)}$
- Pin and Function Compatible with 74ALS161/163



PIN ASSIGNMENT



IEC LOGIC SYMBOL



980910EBA2

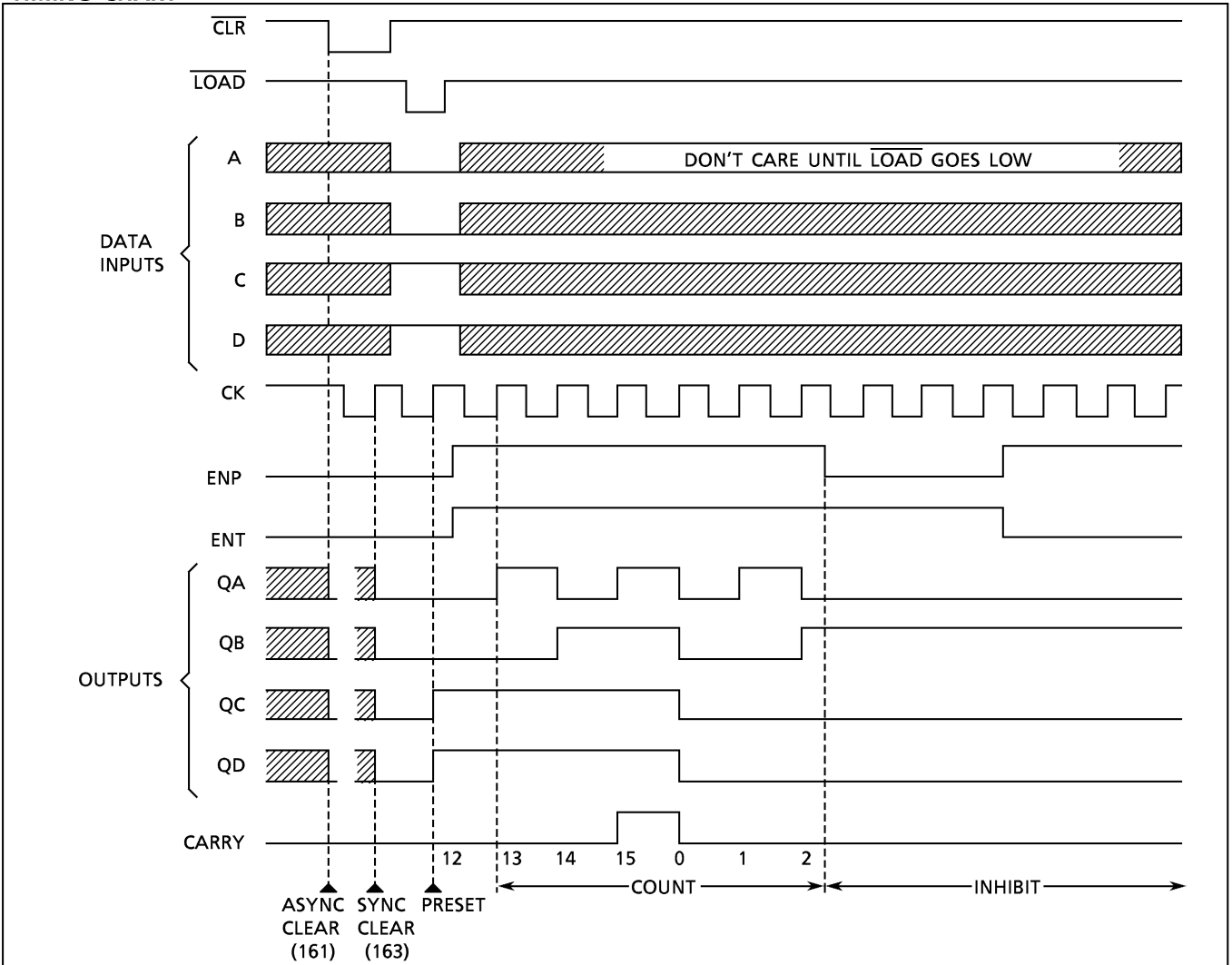
● TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

TRUTH TABLE

TC74VHC161					TC74VHC163					OUTPUTS				FUNCTION
INPUTS					INPUTS					QA	QB	QC	QD	
CLR	LD	ENP	ENT	CK	CLR	LD	ENP	ENT	CK	L	L	L	L	
L	X	X	X	X	L	X	X	X	↑	L	L	L	L	RESET TO "0"
H	L	X	X	↑	H	L	X	X	↑	A	B	C	D	PRESET DATA
H	H	X	L	↑	H	H	X	L	↑	NO CHANGE				NO COUNT
H	H	L	X	↑	H	H	L	X	↑	NO CHANGE				NO COUNT
H	H	H	H	↑	H	H	H	H	↑	COUNT UP				COUNT
H	X	X	X	↓	X	X	X	X	↓	NO CHANGE				NO COUNT

Note X : Don't Care
 A, B, C, D: Logic Level of Data Inputs
 Carry : CARRY = ENT·QA·QB·QC·QD

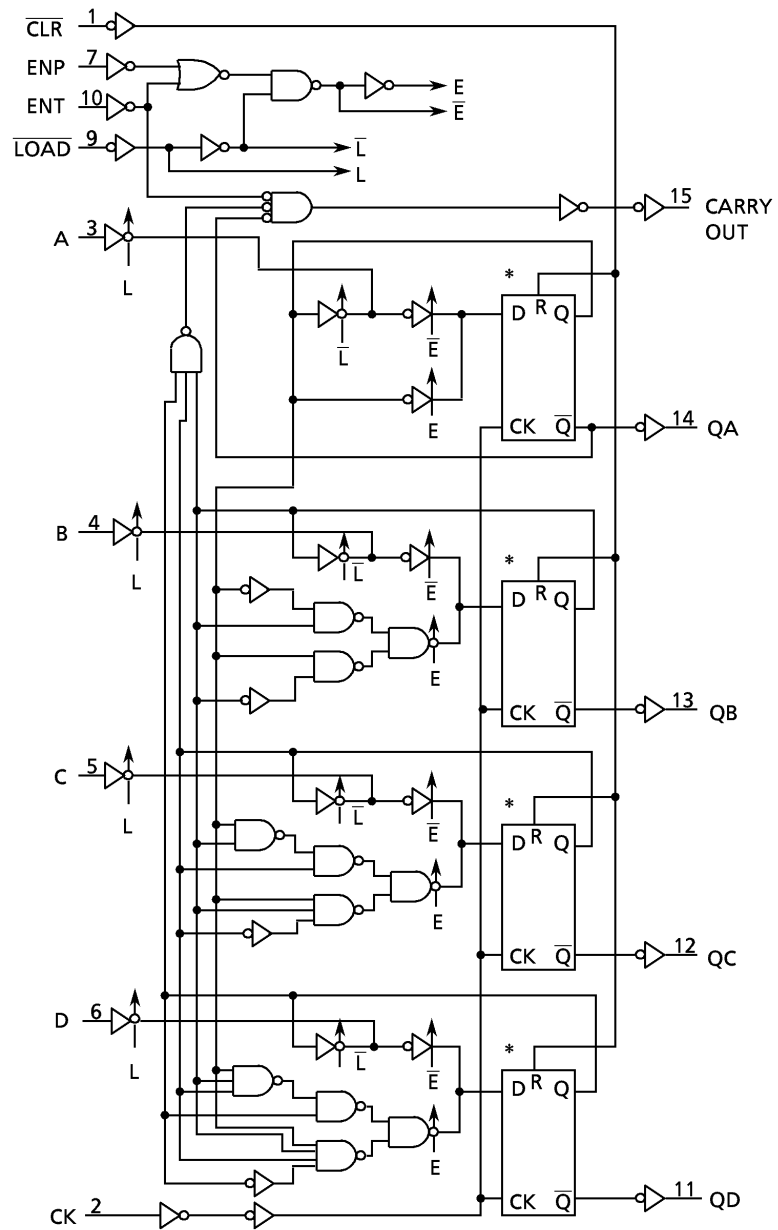
TIMING CHART



980910EBA2'

- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

SYSTEM DIAGRAM



* TRUTH TABLE OF INTERNAL F/F

TC74VHC161					TC74VHC163				
D	CK	R	Q	Q̄	D	CK	R	Q	Q̄
X	X	H	L	H	X	↑	H	L	H
L	↑	L	L	H	L	↑	L	L	H
H	↑	L	H	L	H	↑	L	H	L
X	↓	L	NO CHANGE		X	↓	X	NO CHANGE	

X: Don't Care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~7.0	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} /Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	-65~150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	dt / dv	0~100 ($V_{CC} = 3.3 \pm 0.3V$) 0~20 ($V_{CC} = 5 \pm 0.5V$)	ns / V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^\circ C$			$T_a = -40 \sim 85^\circ C$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V_{IH}		2.0	1.50	—	—	1.50	—	V	
			3.0~ 5.5	$V_{CC} \times 0.7$	—	—	$V_{CC} \times 0.7$	—		
Low - Level Input Voltage	V_{IL}		2.0	—	—	0.50	—	0.50	V	
			3.0~ 5.5	—	—	$V_{CC} \times 0.3$	—	$V_{CC} \times 0.3$		
High - Level Output Voltage	V_{OH}	$V_{IN} =$ V_{IH} or V_{IL}	$I_{OH} = -50 \mu A$	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
Low - Level Output Voltage	V_{OL}	$V_{IN} =$ V_{IH} or V_{IL}	$I_{OL} = 50 \mu A$	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
				3.0	—	—	0.36	—	0.44	
				4.5	—	—	0.36	—	0.44	
Input Leakage Current	I_{IN}	$V_{IN} = 5.5V$ or GND	0~5.5	—	—	± 0.1	—	± 1.0	μA	
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	4.0	—	40.0		

TIMING REQUIREMENTS (Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		Ta = -40~85°C		UNIT
			V _{CC} (V)	LIMIT	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$	Fig. 1	3.3 ± 0.3	5.0	5.0	5.0	ns
			5.0 ± 0.5	5.0	5.0	5.0	
Minimum Pulse Width ($\overline{\text{CLR}}$)*	$t_{W(L)}$	Fig. 4	3.3 ± 0.3 5.0 ± 0.5	5.0 5.0	5.0 5.0		
Minimum Set-up Time (A, B, C, D)	t_s	Fig. 2	3.3 ± 0.3	5.5	6.5		
			5.0 ± 0.5	4.5	4.5		
Minimum Set-up Time (LOAD)	t_s	Fig. 2	3.3 ± 0.3	8.0	9.5		
			5.0 ± 0.5	5.0	6.0		
Minimum Set-up Time (ENT, ENP)	t_s	Fig. 3	3.3 ± 0.3	7.5	9.0		
			5.0 ± 0.5	5.0	6.0		
Minimum Set-up Time ($\overline{\text{CLR}}$)**	t_s	Fig. 5	3.3 ± 0.3	4.0	4.0		
			5.0 ± 0.5	3.5	3.5		
Minimum Hold Time	t_h	Fig. 2, 3	3.3 ± 0.3	1.0	1.0		
			5.0 ± 0.5	1.0	1.0		
Minimum Hold Time ($\overline{\text{CLR}}$)**	t_h	Fig. 5	3.3 ± 0.3	1.0	1.0		
			5.0 ± 0.5	1.5	1.5		
Minimum Removal Time ($\overline{\text{CLR}}$)*	t_{rem}	Fig. 4	3.3 ± 0.3	2.5	2.5		
			5.0 ± 0.5	1.5	1.5		

* for TC74VHC161 only

** for TC74VHC163 only

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT		
			V _{CC} (V)	CL (pF)	MIN.	TYP.	MAX.		MIN.	MAX.
Propagation Delay Time (CK - Q)	t_{pLH} t_{pHL}	Fig. 1, 2	3.3 ± 0.3	15	—	8.3	12.8	1.0	15.0	ns
				50	—	10.8	16.3	1.0	18.5	
			5.0 ± 0.5	15	—	4.9	8.1	1.0	9.5	
				50	—	6.4	10.1	1.0	11.5	
Propagation Delay Time (CK - CARRY, Count Mode)	t_{pLH} t_{pHL}	Fig. 1	3.3 ± 0.3	15	—	8.7	13.6	1.0	16.0	
				50	—	11.2	17.1	1.0	19.5	
			5.0 ± 0.5	15	—	4.9	8.1	1.0	9.5	
				50	—	6.4	10.1	1.0	11.5	
Propagation Delay Time (CK - CARRY, Preset Mode)	t_{pLH} t_{pHL}	Fig. 2	3.3 ± 0.3	15	—	11.0	17.2	1.0	20.0	
				50	—	13.5	20.7	1.0	23.5	
			5.0 ± 0.5	15	—	6.2	10.3	1.0	12.0	
				50	—	7.7	12.3	1.0	14.0	
Propagation Delay Time (ENT - CARRY)	t_{pLH} t_{pHL}	Fig. 6	3.3 ± 0.3	15	—	7.5	12.3	1.0	14.5	
				50	—	10.5	15.8	1.0	18.0	
			5.0 ± 0.5	15	—	4.9	8.1	1.0	9.5	
				50	—	6.4	10.1	1.0	11.5	
Propagation Delay Time (CLR - Q)*	t_{pHL}	Fig. 4	3.3 ± 0.3	15	—	8.9	13.6	1.0	16.0	
				50	—	11.2	17.1	1.0	19.5	
			5.0 ± 0.5	15	—	5.5	9.0	1.0	10.5	
				50	—	7.0	11.0	1.0	12.5	
Propagation Delay Time (CLR - CARRY)*	t_{pHL}	Fig. 4	3.3 ± 0.3	15	—	8.4	13.2	1.0	15.5	
				50	—	10.9	16.7	1.0	19.0	
			5.0 ± 0.5	15	—	5.0	8.6	1.0	10.0	
				50	—	6.5	10.6	1.0	12.0	
Maximum Clock Frequency	f_{MAX}		3.3 ± 0.3	15	80	130	—	70	—	MHZ
				50	55	85	—	50	—	
			5.0 ± 0.5	15	135	185	—	115	—	
				50	95	125	—	85	—	
Input Capacitance	C_{IN}			—	4	10	—	10	pF	
Power Dissipation Capacitance	C_{PD}	(Note 1)		—	23	—	—	—		

Note(1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

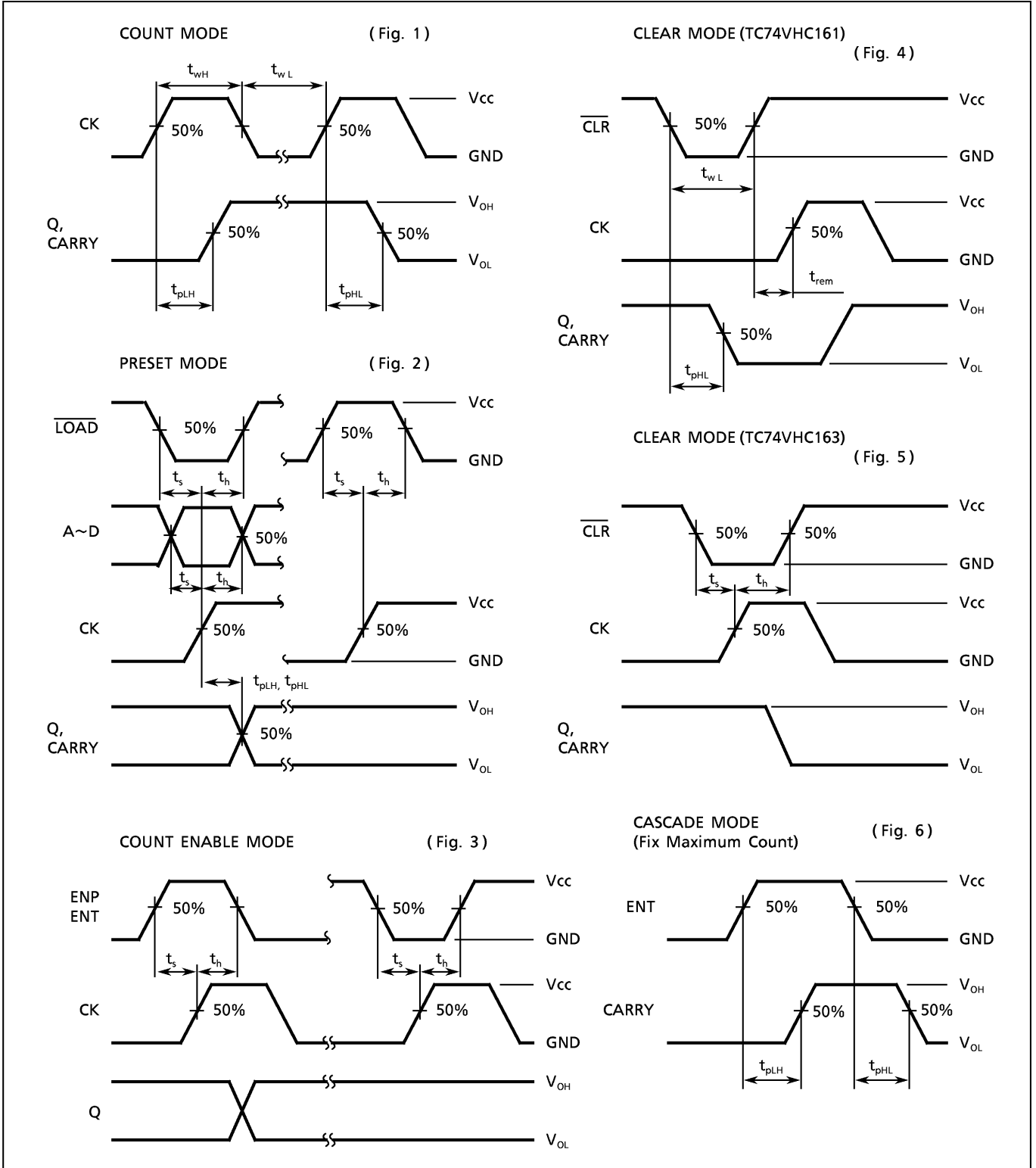
When the outputs drive a capacitive load, total current consumption is the sum of C_{PD} , and ΔI_{CC} which is obtained from the following formula :

$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \left(\frac{C_{QA}}{2} + \frac{C_{QB}}{4} + \frac{C_{QC}}{8} + \frac{C_{QD}}{16} + \frac{C_{CO}}{16} \right)$$

$C_{QA} \sim C_{QD}$ and C_{CO} are the capacitances at QA~QD and CARRY OUT, respectively.
 f_{CK} is the input frequency of the CK.

(2) * for TC74VHC161 only

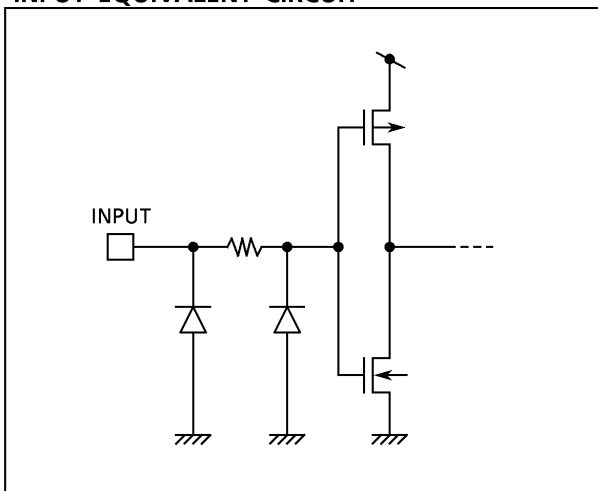
SWITCHING CHARACTERISTICS TEST WAVEFORM



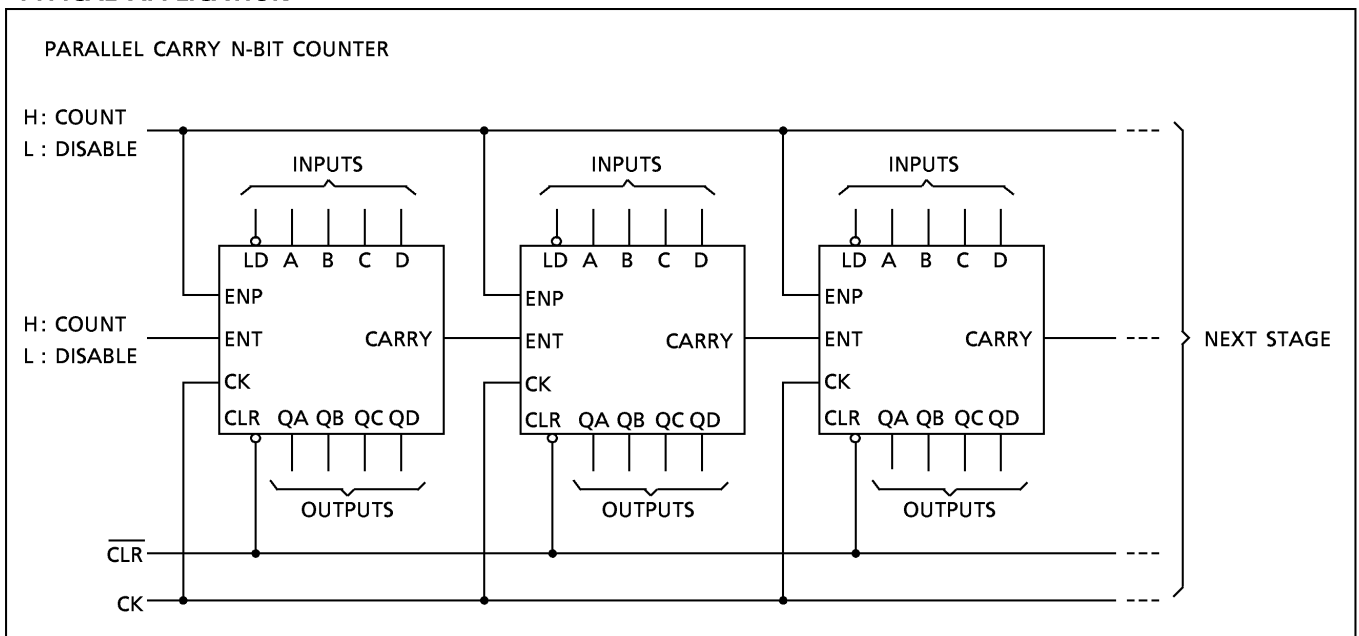
NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION	Ta = 25°C		UNIT	
			V _{CC} (V)	TYP.		MAX.
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	C _L = 50pF	5.0	0.4	0.8	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	C _L = 50pF	5.0	-0.4	-0.8	V
Minimum High Level Dynamic Input Voltage	V _{IHD}	C _L = 50pF	5.0	-	3.5	V
Maximum Low Level Dynamic Input Voltage	V _{ILD}	C _L = 50pF	5.0	-	1.5	V

INPUT EQUIVALENT CIRCUIT

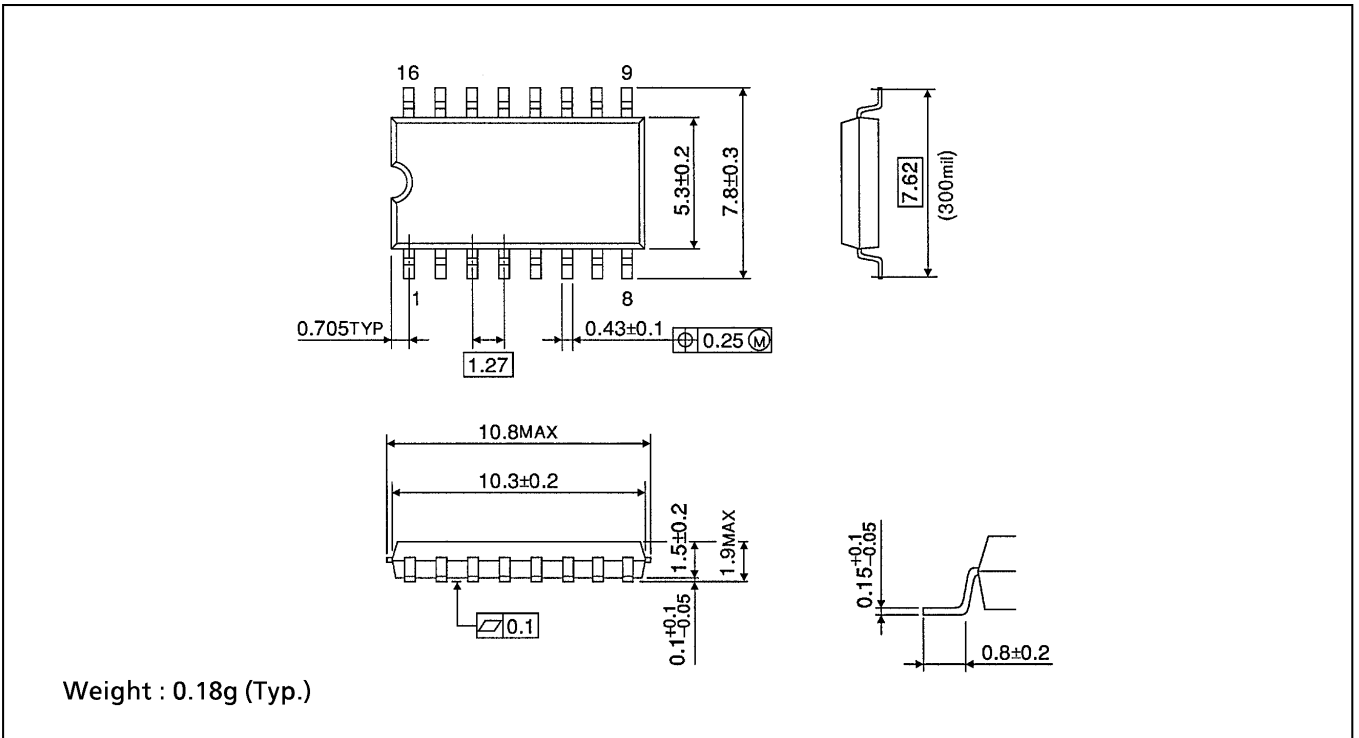


TYPICAL APPLICATION



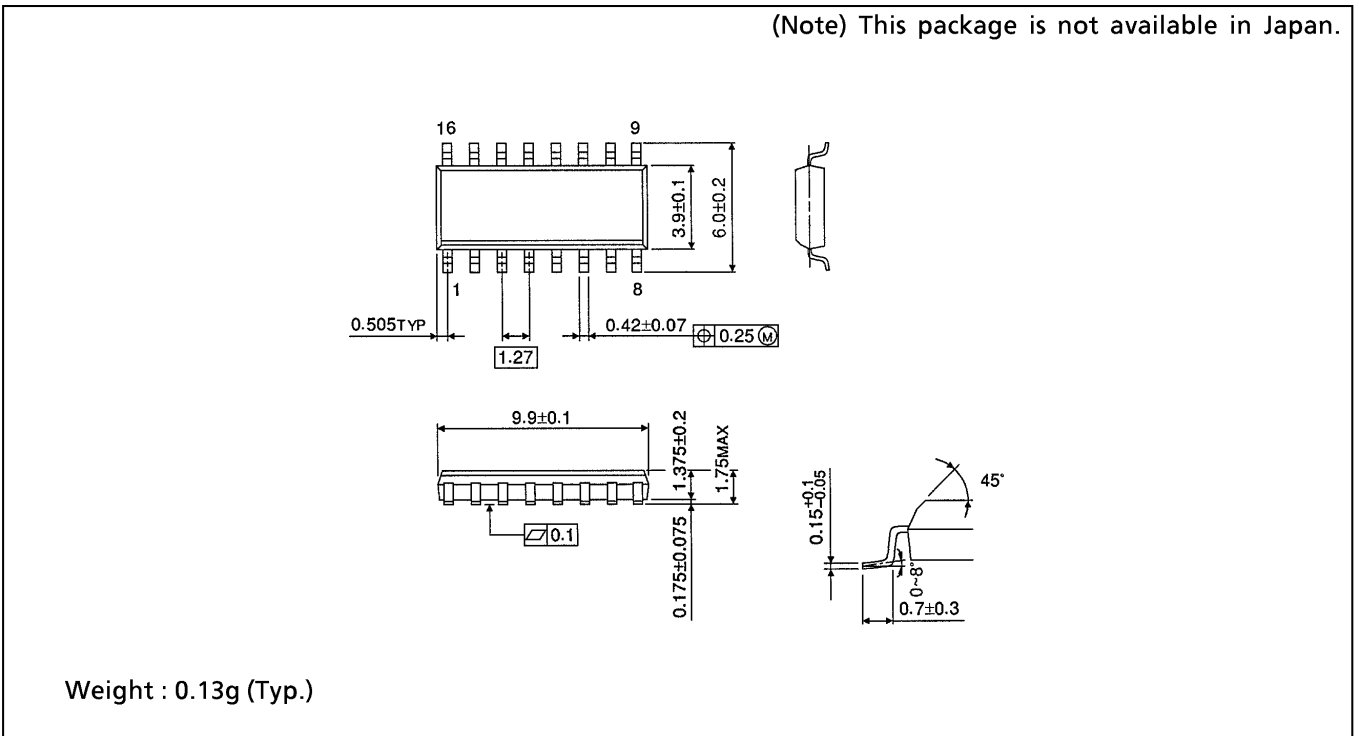
SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)

Unit in mm



SOP 16PIN (150mil BODY) PACKAGE DIMENSIONS (SOP16-P-150-1.27)

Unit in mm



TSSOP 16PIN PACKAGE DIMENSIONS (TSSOP16-P-0044-0.65)

Unit in mm

