

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

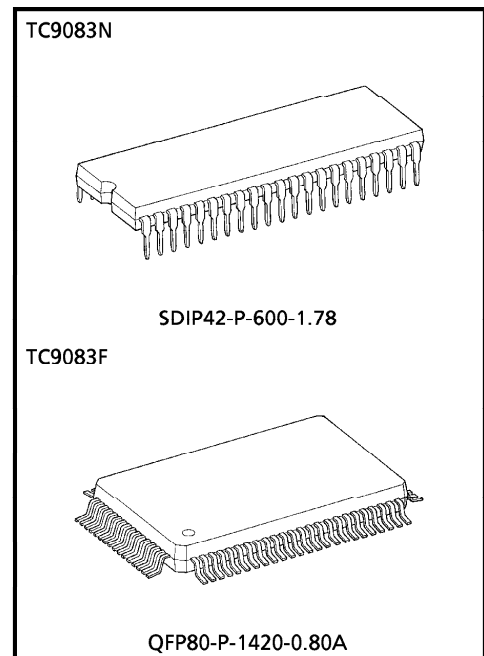
# TC9083N, TC9083F

## 1 CHIP PIP CONTROLLER FOR MULTI COLOR SYSTEM

The TC9083N and the TC9083F provide ADC, DAC and memory. This is a PIP controller IC correspond to MULTI COLOR system. TC9083N and TC9083F can realize PIP processing with only two ICs by combining TC9083N or TC9083F to TA8795BF (PAL/NTSC/SECAM V/C/D IC) or TA8779F (NTSC V/C/D IC).

### FEATURES

- Including 129Kbit DRAM, 6bit ADC×1, 6bit DAC×3, clamp circuit, Multiplexer and controller.
- Corresponding to Multi Color System.
- Sub-picture size are 1/9 and 1/16 (1/16 mode is available in case that horizontal line number of sub-picture is equal to horizontal line number of main picture.)
- Frame color is selectable with Fixed 4 colors (black, red, green and cyan), other programmable 64 colors and no frame.
- Frame width can be controlled.
- Display position is 4 corners. Display position trimming can be controlled independently on each corner.
- Including vertical compensation filter.
- Still picture mode in sub-picture.
- Fixed color display for no program channel.
- I<sup>2</sup>C Bus interface.
- 5V single power supply.
- SDIP42 or QFP80 package.

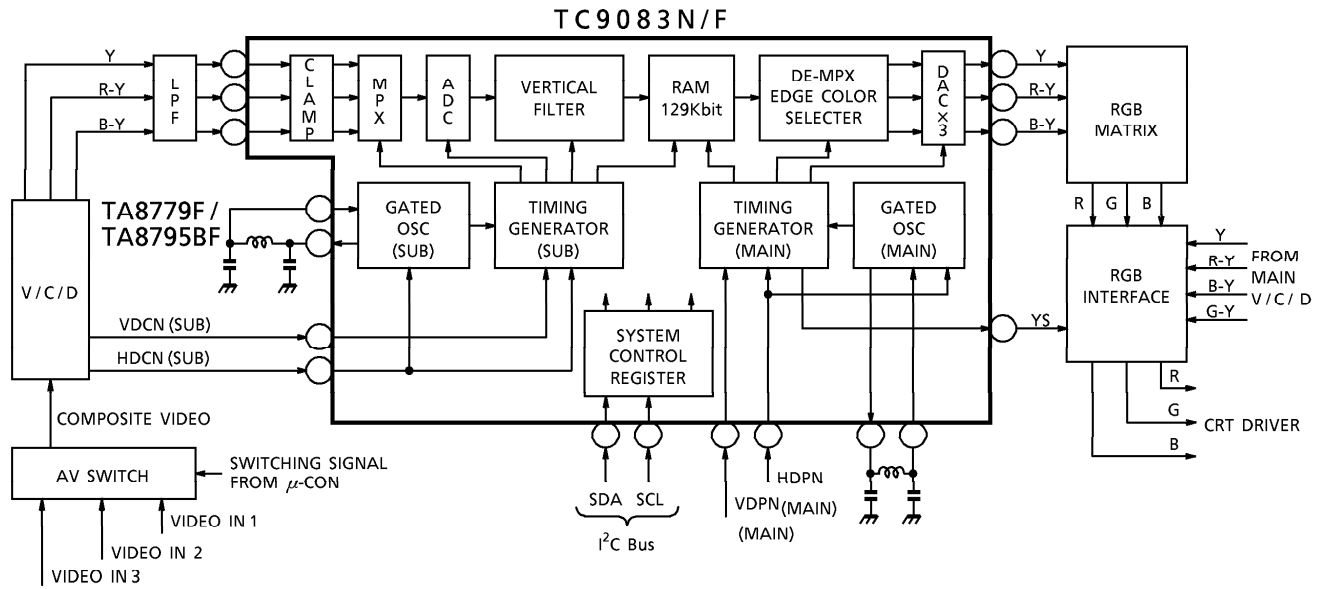


Weight  
 SDIP42-P-600-1.78 : 4.13g (Typ.)  
 QFP80-P-1420-0.80A : 1.6g (Typ.)

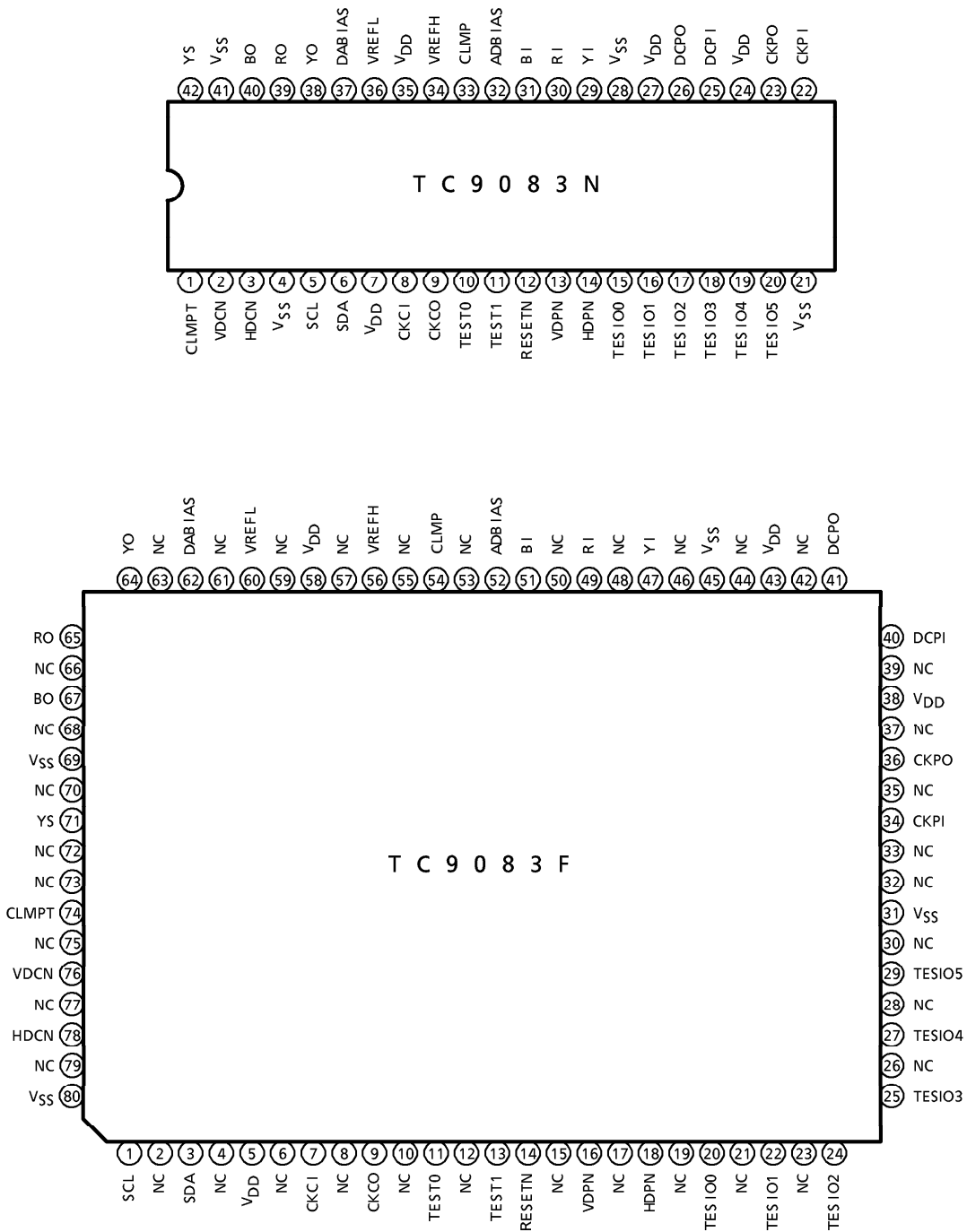
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BLOCK DIAGRAM



TERMINAL CONNECTION DIAGRAM (TOP VIEW)



**TERMINAL FUNCTION**  
 TC9083N (SDIP42 PIN)

PIN No.	PIN NAME	I/O	FUNCTION	CONDITION
1	CLMPT	I	Input for Clamp Timing	Normally : 5.0V <sub>p-p</sub>
2	VDCN	I	Vertical Sync. For Sub-picture	Sync. negative, Normally : 5.0V <sub>p-p</sub>
3	HDCN	I	Horizontal Sync. For Sub-picture	Sync. negative, Normally : 5.0V <sub>p-p</sub>
4	V <sub>SS</sub>		Digital GND For Including RAM	
5	SCL	I	I <sup>2</sup> C Bus Clock Input	
6	SDA	I/O	I <sup>2</sup> C Bus Data Input	
7	V <sub>DD</sub>		Digital V <sub>DD</sub> For Including RAM	Normally : 5.0V
8	CKCI	I	Gated-OSC For Sub-picture	
9	CKCO	O	Gated-OSC For Sub-picture	
10	TEST0	I	Test Terminal	Normally : connect with Digital V <sub>DD</sub>
11	TEST1	I	Test Terminal	Normally : connect with Digital V <sub>DD</sub>
12	RESETN	I	System Reset	Normally : connect with Digital V <sub>DD</sub>
13	VDPN	I	Vertical Sync. For Main-picture	Sync. negative, Normally : 5.0V <sub>p-p</sub>
14	HDPN	I	Horizontal Sync. For Main-picture	Sync. negative, Normally : 5.0V <sub>p-p</sub>
15	TESIO0	I/O	Test Terminal	Normally : connect with Digital GND
16	TESIO1	I/O	Test Terminal	Normally : connect with Digital GND
17	TESIO2	I/O	Test Terminal	Normally : connect with Digital GND
18	TESIO3	I/O	Test Terminal	Normally : connect with Digital GND
19	TESIO4	I/O	Test Terminal	Normally : connect with Digital GND
20	TESIO5	I/O	Test Terminal	Normally : connect with Digital GND
21	V <sub>SS</sub>		Digital GND For Internal Logic	
22	CKPI	I	Gated-OSC For Main-picture	
23	CKPO	O	Gated-OSC For Main-picture	
24	V <sub>DD</sub>		Digital V <sub>DD</sub> For Internal Logic	Normally : 5.0V
25	DCPI	I	External Delay Input For Clamp	
26	DCPO	O	External Delay Output For Clamp	
27	V <sub>DD</sub>		Digital V <sub>DD</sub> For Including RAM-Plate	Normally : 5.0V
28	V <sub>SS</sub>		Analog GND For ADC	
29	YI	I	Analog Luminance Signal Input	Normally : 1.0V <sub>p-p</sub>
30	RI	I	Analog R-Y Signal Input	Normally : 1.0V <sub>p-p</sub>
31	BI	I	Analog B-Y Signal Input	Normally : 1.0V <sub>p-p</sub>
32	ADBIAS	I	Bias For Including ADC	
33	CLMP	I	Clamp Control	
34	VREFH	I	Reference Voltage For A/D	Normally : 5.0V
35	V <sub>DD</sub>		Analog V <sub>DD</sub> For ADC, DAC	Normally : 5.0V
36	VREFL	I	Reference Voltage For DAC	Normally : 3.0V
37	DABIAS	I	Bias For Including DAC	

PIN No.	PIN NAME	I/O	FUNCTION	CONDITION
38	YO	O	Analog Y Signal Output	Normally : 2.0V <sub>p-p</sub>
39	RO	O	Analog R-Y Signal Output	Normally : 2.0V <sub>p-p</sub>
40	BO	O	Analog B-Y Signal Output	Normally : 2.0V <sub>p-p</sub>
41	V <sub>SS</sub>		Analog GND For DAC	
42	YS	O	Main, Sub-picture Switching Timing	Sync. positive, Normally : 5.0V <sub>p-p</sub>

TC9083F (QFP80 PIN)

PIN No.	PIN NAME	I/O	FUNCTION	CONDITION
1	SCL	I	I <sup>2</sup> C Bus Clock Input	
2	NC	—		
3	SDA	I/O	I <sup>2</sup> C Bus Data Input	
4	NC	—		
5	V <sub>DD</sub>		Digital V <sub>DD</sub> For Including RAM	Normally : 5.0V
6	NC	—		
7	CKCI	I	Gated OSC For Sub-picture	
8	NC	—		
9	CKCO	O	Gated OSC For Sub-picture	
10	NC	—		
11	TEST0	I	Test Terminal	Normally : connect with Digital V <sub>DD</sub>
12	NC	—		
13	TEST1	I	Test Terminal	Normally : connect with Digital V <sub>DD</sub>
14	RESETN	I	System Reset	Normally : connect with Digital V <sub>DD</sub>
15	NC	—		
16	VDPN	I	Vertical Sync. For Main-picture	Sync. negative Normally : 5.0V <sub>p-p</sub>
17	NC	—		
18	HDPN	I	Horizontal Sync. For Main-picture	Sync. negative Normally : 5.0V <sub>p-p</sub>
19	NC	—		
20	TESIO0	I/O	Test Terminal	Normally : connect with Digital GND
21	NC	—		
22	TESIO1	I/O	Test Terminal	Normally : connect with Digital GND
23	NC	—		
24	TESIO2	I/O	Test Terminal	Normally : connect with Digital GND
25	TESIO3	I/O	Test Terminal	Normally : connect with Digital GND
26	NC	—		
27	TESIO4	I/O	Test Terminal	Normally : connect with Digital GND
28	NC	—		

PIN No.	PIN NAME	I/O	FUNCTION	CONDITION
29	TESIO5	I/O	Test Terminal	Normally : connect with Digital GND
30	NC	—		
31	V <sub>SS</sub>		Digital GND For Internal Logic	
32	NC	—		
33	NC	—		
34	CKPI	I	Gated OSC For Main-picture	
35	NC	—		
36	CKPO	O	Gated OSC For Main-picture	
37	NC	—		
38	V <sub>DD</sub>		Digital V <sub>DD</sub> For Internal Logic	Normally : 5.0V
39	NC	—		
40	DCPI	I	External Delay Input For Clamp	
41	DCPO	O	External Delay Output For Clamp	
42	NC	—		
43	V <sub>DD</sub>		Digital V <sub>DD</sub> For Including RAM-Plate	Normally : 5.0V
44	NC	—		
45	V <sub>SS</sub>		Analog GND For ADC	
46	NC	—		
47	YI	I	Analog Luminance Signal Input	Normally : 1.0V <sub>p-p</sub>
48	NC	—		
49	RI	I	Analog R-Y Signal Input	Normally : 1.0V <sub>p-p</sub>
50	NC	—		
51	BI	I	Analog B-Y Signal Input	Normally : 1.0V <sub>p-p</sub>
52	ADBIAS	I	Bias For including ADC	
53	NC	—		
54	CLMP	I	Clamp control	
55	NC	—		
56	VREFH	I	Reference Voltage For A/D	Normally : 5.0V
57	NC	—		
58	V <sub>DD</sub>		Analog V <sub>DD</sub> For ADC, DAC	Normally : 5.0V
59	NC	—		
60	VREFL	I	Reference Voltage For DAC	Normally : 3.0V
61	NC	—		
62	DABIAS	I	Bias For including DAC	
63	NC	—		

PIN No.	PIN NAME	I/O	FUNCTION	CONDITION
64	YO	O	Analog Y Signal Output	Normally : 2.0V <sub>p-p</sub>
65	RO	O	Analog R-Y Signal Output	Normally : 2.0V <sub>p-p</sub>
66	NC	—		
67	BO	O	Analog B-Y Signal Output	Normally : 2.0V <sub>p-p</sub>
68	NC	—		
69	V <sub>SS</sub>		Analog GND For DAC	
70	NC	—		
71	YS	O	Main, Sub-picture Switching Timing	Sync. positive Normally : 5.0V <sub>p-p</sub>
72	NC	—		
73	NC	—		
74	CLMPT	I	Input for Clamp timing	
75	NC	—		
76	VDCN	I	Vertical Sync. For Sub-picture	Normally : 5.0V <sub>p-p</sub>
77	NC	—		
78	HDCN	I	Horizontal Sync. For Sub-picture	Normally : 5.0V <sub>p-p</sub>
79	NC	—		
80	V <sub>SS</sub>		Digital GND For Including RAM	

**FUNCTION SUMMARY**

1. Clamp timing

The clamp pulse showed in <Timing fig.1> is generated by inputting composite sync. (negative) or horizontal sync. (negative) to CLMPT terminal (ref. <Circuit fig.1>).

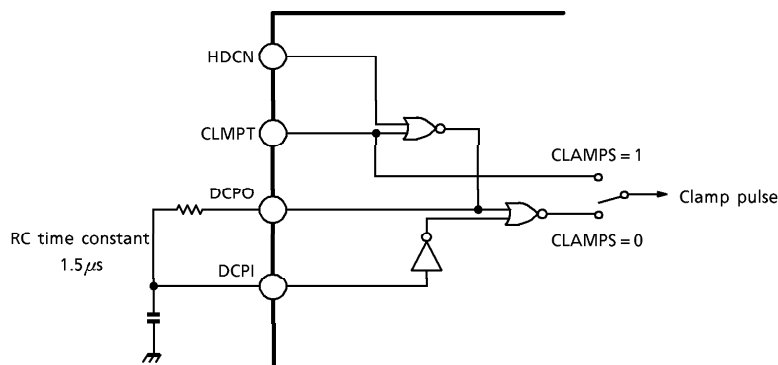
The CLMPT terminal can input clamp pulse from external circuit directly.

In this case, CLMPS of I<sup>2</sup>C bus register (sub-address 10H 3rd data, select clamp circuit) set 1, DCPI terminal is pulled down to GND level and DCPO terminal is open.

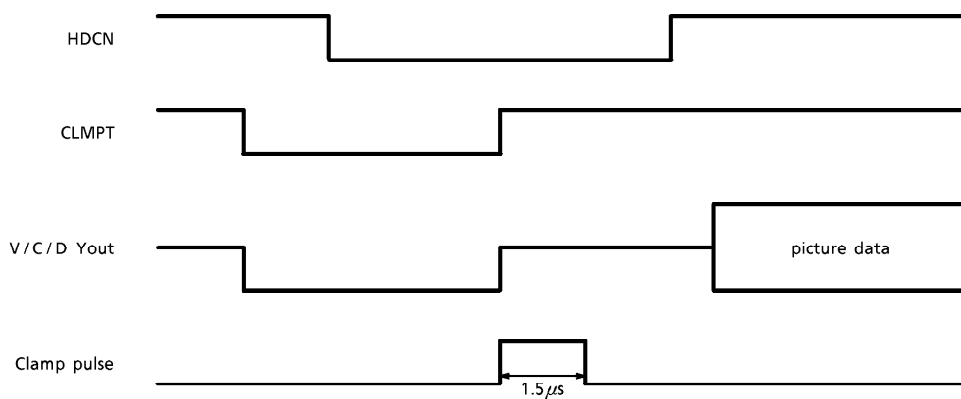
Y, R-Y and B-Y signal, which are outputted from sub-picture demodulator IC, are clamped to match dynamic range of ADC. Clamp level of each signal are

- Y : 0V
- R-Y : 0.5V
- B-Y : 0.5V

<Circuit fig.1>



<Timing fig.1>





2. Multiplex circuit

After clamp circuit, Y, R-Y and B-Y are multiplexed to change to time division video signal.

(Y)→(R-Y)→(Y)→(B-Y)→(Y)→(R-Y)→(Y)→(B-Y) .....

Multiplex is effected above order.

3. AD converter

1V<sub>p-p</sub> analog multiplexed video signal is converted to 6bit digital multiplexed video signal.

Sampling frequency are

when 1/9 size ..... 6.0MHz

when 1/16 size ..... 4.5MHz

4. Vertical compensation filter

Vertical compensation filter improves vertical resolution with compensating each line data by using 2Kbit SRAM when horizontal line data is thinned out to match sub-picture size 1/9, 1/16.

Difference vertical line number is compensated with changing coefficient of filter in 525/625 (horizontal line) Multi display mode.

SUB-PICTURE SIZE	SYSTEM (HORIZONTAL LINE) (MAIN / SUB)	TAP NUMBER	COEFFICIENT
1/9	525/525	3	1/4 1/2 1/4
	625/625	3	1/4 1/2 1/4
	525/625	4	1/8 3/8 3/8 1/8
	625/525	3	1/4 1/2 1/4
1/16	525/525	4	1/8 3/8 3/8 1/8
	625/625	4	1/8 3/8 3/8 1/8

Provided that In 525/625 mode, 2lines are took in with 1/8, 3/8, 3/8, 1/8, 3/8, 3/8, 1/8.

In 625/625 mode, 2lines are took in with 1/4, 1/2, 1/4, 1/2, 1/4.

5. Memory

129Kbit DRAM is used as sub-picture 1 field memory.

6. Sub-picture take in area

Sub-picture size 1/9

Horizontal Y = 168dot  
 R-Y = 42dot  
 B-Y = 42dot

Sub-picture size 1/16

Horizontal Y = 128dot  
 R-Y = 32dot  
 B-Y = 32dot

Vertical (Sub-picture size 1/9)

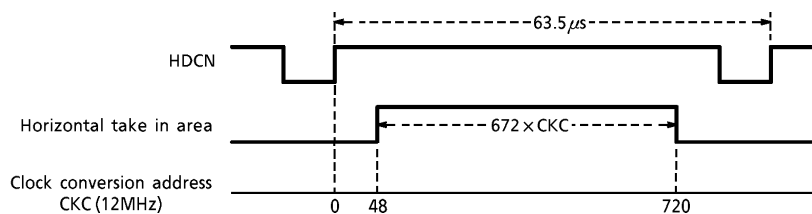
Main/Sub 525line / 625line = 268H  
 625line / 525line = 210H

(Sub-picture size 1/9, 1/16 common)

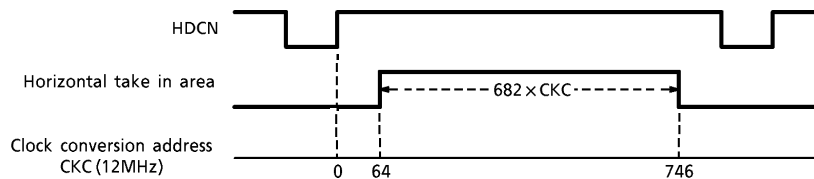
525line / 525line = 228H  
 625line / 625line = 252H

7. Explanation about take in timing

7.1. Horizontal take in area (Sub-picture size 1/9)



7.2. Horizontal take in area (Sub-picture size 1/16)



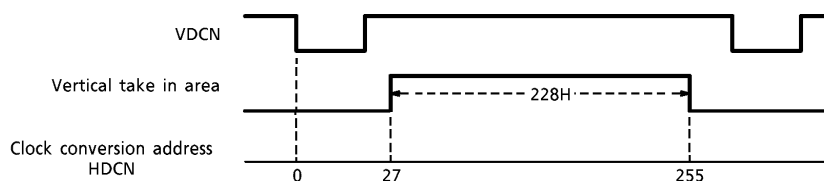
Horizontal take in area can be trimmed as follows ; (Clock conversion)

At 1/9 picture, -24, -12, +12 from preset

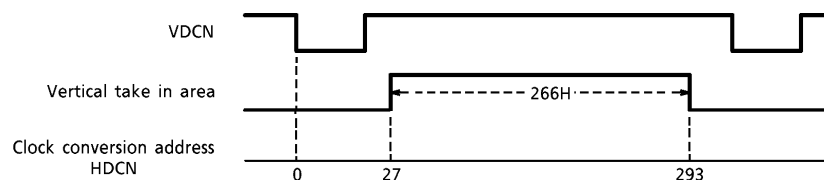
At 1/10 picture, -32, -16, +16 from preset

7.3. Vertical take in area (Sub-picture size 1/9, 1/16 common)

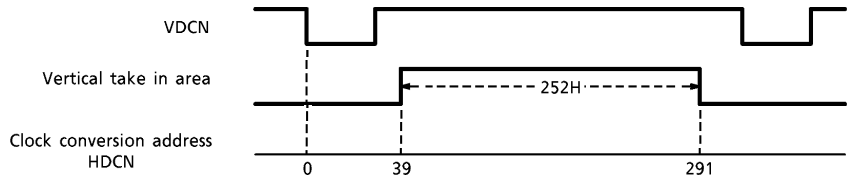
7.3.1. Main = 525line, Sub = 525line



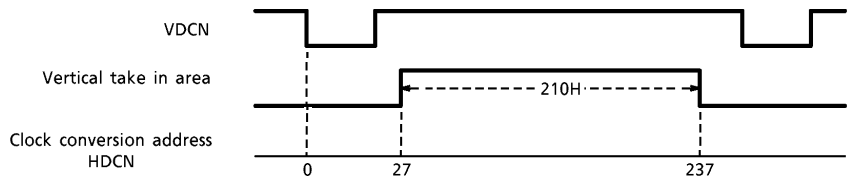
7.3.2. Main = 525line, Sub = 625line (Sub-picture size 1/9)



7.3.3. Main = 625line, Sub = 625line (Sub-picture size 1/9, 1/16 common)



7.3.4. Main = 625line, Sub = 525line (Sub-picture size 1/9)



8. Sub-picture display area

Sub-picture size 1 / 9

Horizontal Y = 160dot  
 R-Y = 40dot  
 B-Y = 40dot

Vertical 525line = 74H  
 625line = 84H

Sub-picture size 1 / 16

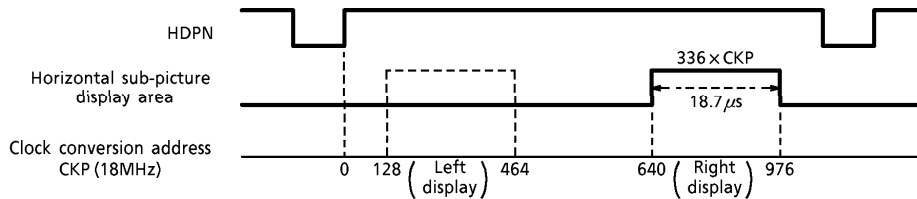
Horizontal Y = 120dot  
 R-Y = 30dot  
 B-Y = 30dot

Vertical 525line = 56H  
 625line = 60H

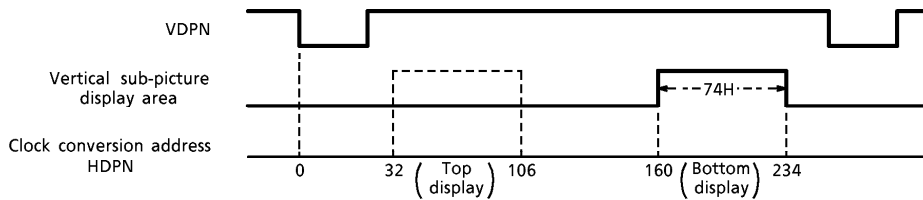
9. Explanation about display timing

9.1. Main = 525line, Sub = 525line or 625line, Size = 1 / 9

9.1.1. Horizontal sub-picture display area

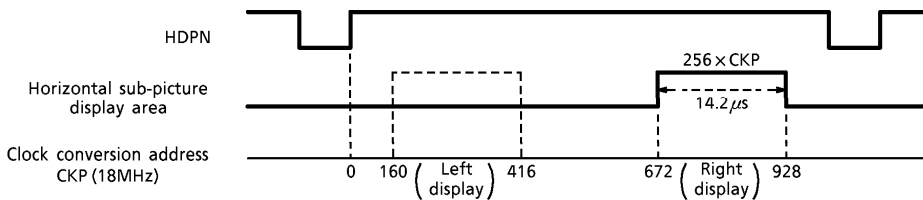


9.1.2. Vertical sub-picture display area

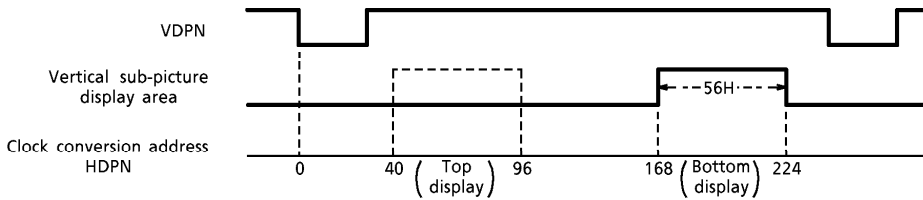


9.2. Main = 525line, Sub = 525line, Size = 1 / 16

9.2.1. Horizontal sub-picture display area



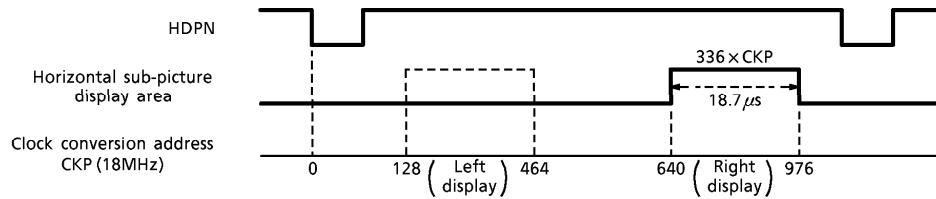
9.2.2. Vertical sub-picture display area



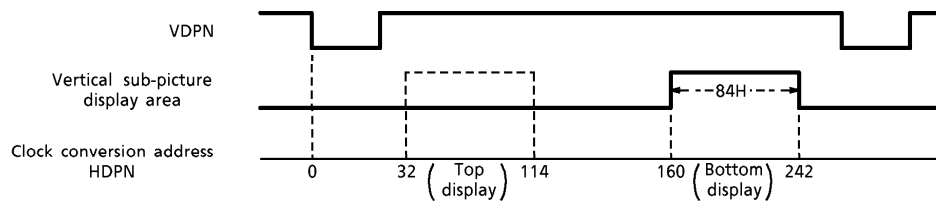
All of above data are preset value.  
 Display area can be trimmed as follows.  
 To horizontal direction, -28~127step (1step is CKP x 4)  
 To vertical direction, -64~63step (1step is 2H)

9.3. Main = 625line, Sub = 525line or 625line, Size = 1 / 9

9.3.1. Horizontal sub-picture display area

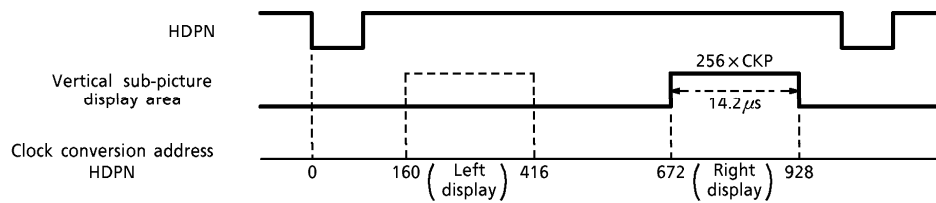


9.3.2. Vertical sub-picture display area

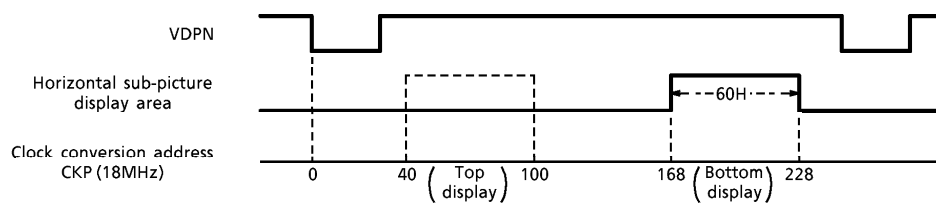


9.4. Main = 625line, Sub = 625line, Size = 1 / 16

9.4.1. Horizontal sub-picture display area



9.4.2. Vertical sub-picture display area



All of above data are preset value.

Display area can be trimmed as follows.

To horizontal direction, - 28~127step (1step is  $CKP \times 4$ )

To vertical direction, - 64~63step (1step is  $2H$ )

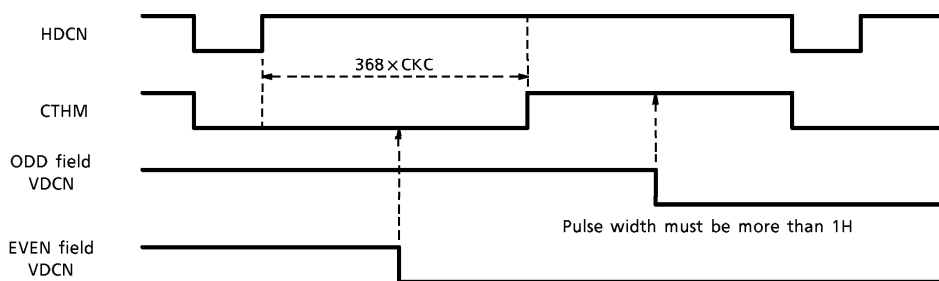
10. ODD/EVEN field detection timing.

TC9083N and TC9083F detect ODD/EVEN field at each main and sub-picture internally. So, the phase of HDCN and VDCN, or, HDPN and VDPN, which are inputted from external, must be controlled. CTHM and PTHM are field detection pulse. These are made by HDCN and CKC (12MHz), or, HDPN and CKP (18MHz). If the trailing of VDCN and VDPN, which are inputted from external, exist during detection pulse is high, ODD field is detected. And if that trailing exist during detection pulse is low, EVEN field is detected.

The leading of VDCD and VDPN must exist in center of detection pulse so that ODD/EVEN field detection is stable.

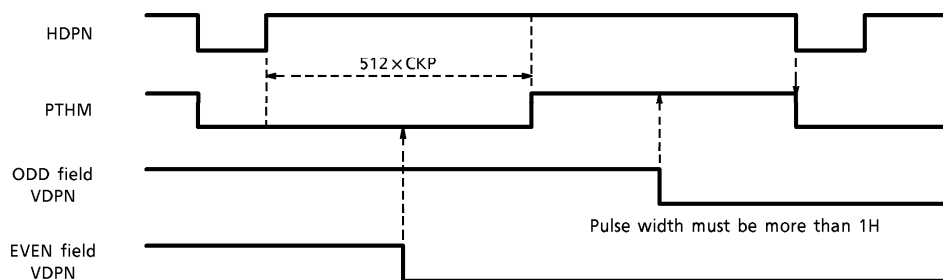
The period of VDCN and VDPN must be more than 1H.

10.1. Write mode (Sub-picture) ODD/EVEN field detection

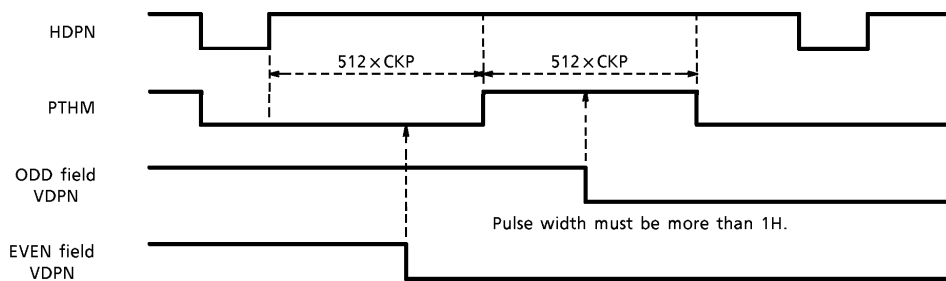


10.2. Read mode (Main-picture) ODD/EVEN field detection

10.2.1. HDPN is "H" < 1024 x CKP



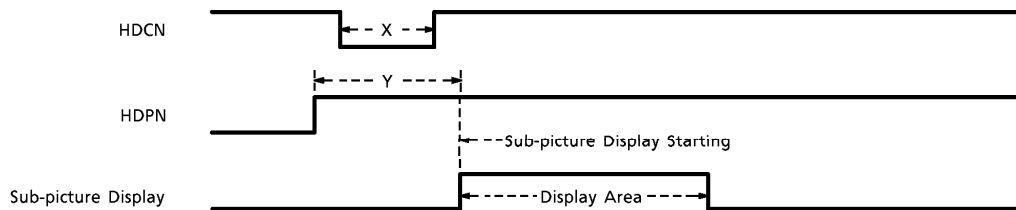
10.2.2. HDPN is "H" > 1024 x CKP



(Note) Limitation about HDCN (Sub-picture Horizontal sync. signal) width (Low period)

1. X is Low period of HDCN.
2. Y is a period start from leading edge of HDPN, and end at start point of sub-picture display.  
X must be smaller than  $\textcircled{A}$ .

$\textcircled{A} : X \leq Y - 25$  (Clock cycle) (Clock : sub-picture)



11. Frame color setting

Frame color can be selected 4 color (black, red, green and cyan) as fixed color via I<sup>2</sup>C BUS. Besides this, frame color can be selected 64 colors with changing upper 2bit in the 6bit for Y, R-Y, B-Y, which structure frame color, via I<sup>2</sup>C BUS. Set frame color with BACKC=0, black color change to selected color to CDATA 5-0 via I<sup>2</sup>C Bus.

12. Frame width control

Frame width can be controlled with changing the pulse width of main/sub switching pulse. Control range is follows;

Horizontal	0~8dot	4dot step
Vertical	0~2line / field	1line step

13. Display position control

Preset position is Lower right. Besides this, display position can be set to upper right, upper left and lower left via I<sup>2</sup>C Bus. Display position can be trimmed with Horizontal 8bit and Vertical 7bit. Control range is follows;

Horizontal	- 128 ~ + 127 steps	4dot / step
Vertical	- 64 ~ + 63 steps	1line / step

14. Still picture mode

Still picture can be displayed with stopping writing to field memory for reading same picture data.

15. Fixed color display for no program channel

Sub-picture is fixed color via I<sup>2</sup>C Bus. Display color can be selected 64 colors with changing upper 2bit in the 6bit for Y, R-Y, B-Y, which structure display color, via I<sup>2</sup>C Bus. Set display color with BACK=1, black color change to selected color to CDATA 5~0 via I<sup>2</sup>C Bus.

16. Multi color mode

		Main-Picture	
		525Line	625Line
Sub-Picture	525Line	○	○
	625Line	○	○

At 525line/625line or 625line/525line mode, 1 field is displayed for avoiding V dancing.

17. DA converter

This DA Converter converts 6bit sub-picture digital data to  $2V_{p-p}$  analog signal. Bandwidth is 9MHz.

18. I<sup>2</sup>C Bus

I<sup>2</sup>C Bus control is provided.

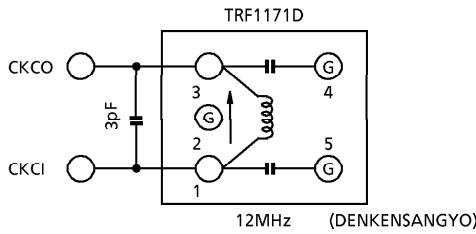
Slave address : 2E (H), 2F (H)

Sub-address : 00 (H), 10 (H), 20 (H), 30 (H)

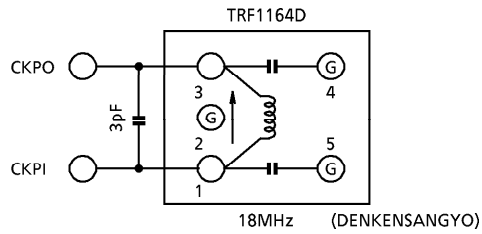
Sub-picture position trimming data (sub-address 20 (H)) should be sent after 20ms in NTSC mode, or 24ms in PAL mode, sending sub-picture position data (sub-address 10 (H)).

APPLICATION CIRCUIT

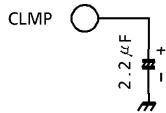
1. GATED OSC SUB CLOCK



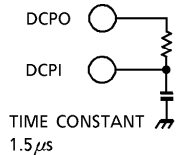
MAIN CLOCK



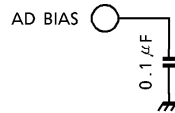
2. CLAMP



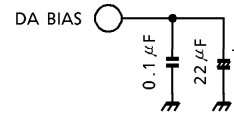
3. CLAMP CONTROL



4. A/D BIAS



5. D/A BIAS

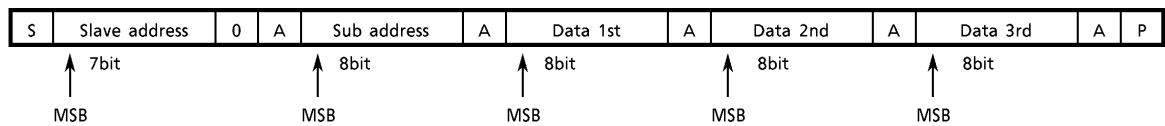




**I<sup>2</sup>C BUS CONTROLLED FORMAT SUMMARY**

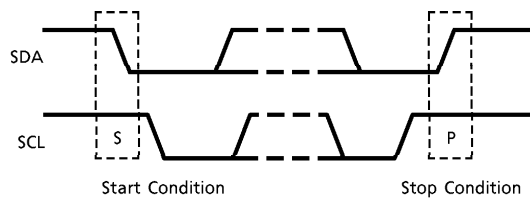
Bus controlled format of TC9083N and TC9083F are based on I<sup>2</sup>C Bus Control format of Philips.

**Data Transfer Format**

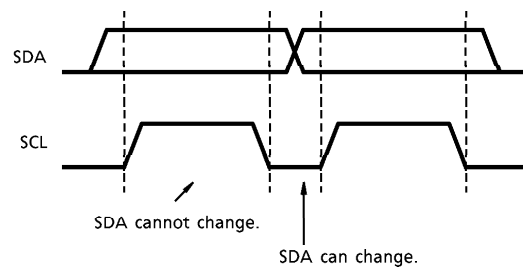


S : Start Condition  
 P : Stop Condition  
 A : Acknowledge

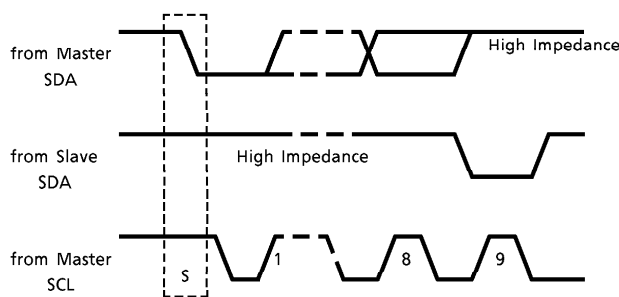
**(1) Start and Stop Condition**



**(2) Bit Transfer**



**(3) Acknowledge**



**(4) Slave Address**

A6	A5	A4	A3	A2	A1	A0	R/ $\bar{W}$
0	0	1	0	1	1	1	0

Purchase of TOSHIBA I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips.

I<sup>2</sup>C Bus Register

TC9083F and TC9083N have write address of 00101110 (2EH).

Sub-address 00H (No program data)

Sub-address 10H

1st DATA (Preset : C0H)

MSB							LSB
POS1	POS0	COLOR1	COLOR0	STILL	0	0	ON/OFF

2nd DATA (Preset : 02H)

MSB							LSB
SPAL	MPAL	BACK	0	0	0	1	0

3rd DATA (Preset : 60H)

MSB							LSB
YCDEL1	YCDEL0	WR1	WR0	0	0	0	CLAMPS

POS1, 0 : Sub-picture display position 4corners (Preset 11 : Right bottom corner)  
 00 → Left top corner, 01 → Right top corner, 10 → Left bottom corner  
 11 → Right bottom corner

COLOR1,0 : Frame color (Preset 00 : Green)  
 00 → Green, 01 → Cyan, 10 → Red, 11 → Variable (\*)  
 (\*) Color setting : Sub-address 20H CDATA5~0, Preset 000000 : Black

STILL : Still mode (Preset 0 : Moving picture)  
 0 → Moving picture, 1 → Still picture

ON/OFF : Sub-picture display ON/OFF (Preset 0 : Undisplay)  
 0 → Undisplay, 1 → Display

SPAL : Sub-picture change 525line/625line (Preset 0 : 525line)  
 0 → 525line, 1 → 625line

MPAL : Main-picture change 525line/625line (Preset 0 : 525line)  
 0 → 525line, 1 → 625line

BACK : No program channel processing (Preset 0 : No processing)  
 0 → no processing,  
 1 → No program channel processing (\*)  
 (\*) Color setting : Sub-address 20H CDATA5~0, Preset 000000 : Black

YCDL1, 0 : Sub-picture's luminance Y phase control (Preset 01 : Luminance Y color difference R-Y/B-Y same phase)  
 00 → Y phase is 1dot fast to R-Y/B-Y  
 01 → Luminance Y color difference R-Y/B-Y same phase  
 10 → Y phase is 1dot delay to R-Y/B-Y  
 11 → Y phase is 2dot delay to R-Y/B-Y

WR1, 0 : Write position (horizontal) (Preset 10 : Write from active area)  
 00 → 4dot fast to default  
 01 → 2dot fast to default  
 10 → Write from active area  
 11 → 2dot delay to default

CLAMP : Clamp circuit (Preset 0 : Internal Circuit)  
 0 → Internal Circuit, 1 → External Circuit

(Note) "0" should be put into open bit in above register

Sub-address 20H

1st DATA (Preset : 00H)

MSB							LSB
H7	H6	H5	H4	H3	H2	H1	H0

2nd DATA (Preset : 00H)

MSB							LSB
V6	V5	V4	V3	V2	V1	V0	BLACKC

3rd DATA (Preset : 00H)

MSB							LSB
CDATA5	CDATA4	CDATA3	CDATA2	CDATA1	CDATA0	0	0

H7-0 : Horizontal display adjustment (Preset 00000000)  
 8bit 2's compliment data (4dot / 1LSB)  
 10000000~00000000~01111111  
 Left Right

V6-0 : Vertical display adjustment (Preset 00000000)  
 7bit 2's compliment data (2Line / 1LSB)  
 1000000~0000000~0111111  
 Bottom Top

BLACKC : Setting the resister for variable color data (Preset 0 : Frame color selection)  
 0 → Frame color setting  
 1 → Display color setting for no program channel is resister

CDATA5-0 : Variable color (Preset 0000000)  
 CDATA5, 4 → MSB, 2ndMSB (Y signal)  
 CDATA3, 2 → MSB, 2ndMSB (R-Y signal)  
 CDATA1, 0 → MSB, 2ndMSB (B-Y signal)

(Note) "0" should be put into open bit in above register

Sub-address 30H

1st DATA (Preset : 57H)

MSB							LSB
9 / 16	YSHW6	YSHW5	YSHW4	YSHW3	YSHW2	YSHW1	YSHW0

2nd DATA (Preset : 98H)

MSB							LSB
YSVW5	YSVW4	YSVW3	YSVW2	YSVW1	YSVW0	YSDEL1	YSDEL0

3rd DATA (Preset : B2H)

MSB							LSB
YSC6	YSC5	YSC4	YSC3	YSC2	YSC1	YSC0	0

- 9 / 16 : Sub-picture size select (Preset 0 : 1/9)  
 0 → 1/9, 1 → 1/16
- YSHW6-0 : YS horizontal width (Preset 1010111)  
 Straight binarydata  
 No frame → 1010110  
 4dot width frame → 1010111  
 8dot width frame → 1011000
- YSVW5-0 : YS vertical width (Preset 100110)  
 Straight binarydata  
 No frame → 100100  
 1Line width frame → 100101  
 2Line width frame → 100110
- YSDL1, 0 : YS horizontal delay (Preset 00 : No delay)  
 00 → No delay 01 → 0.5dot delay  
 10 → 1.0dot delay 01 → 1.5dot delay
- YSC6-0 : YS center (Preset 1011001)  
 Straight binarydata  
 1LSB → 2dot move  
 Recommendation : 1011101

(Note) "0" should be put into open bit in above register

## MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	$V_{SS}, V_{DD}$	$V_{SS} \sim V_{SS} + 6.0$	V
Input Voltage	$V_{IN}$	$-0.3 + V_{SS} \sim V_{DD} + 0.3$	V
Power Dissipation	$P_D$	800	mW
Storage Temperature	$T_{stg}$	$-55 \sim 125$	°C

## RECOMMENDED OPERATING CONDITION

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Supply Voltage	$V_{DD}$		4.5	5.0	5.5	V
Input Voltage	$V_{IN}$		0		$V_{DD}$	V
Operating Temperature	$T_{opr}$		-20		70	°C

**ELECTRICAL CHARACTERISTICS**

**DC CHARACTERISTICS**

Condition :  $V_{DD} = 4.5 \sim 5.5V$ ,  $T_a = -20 \sim 70^\circ C$ ,  $V_{SS} = 0V$

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Current Consumption	$I_{DD}$	—		—	—	140	mA
High Level Input Voltage	CMOS	—	*1	4.0	—	—	V
	SMTC		*2	4.0	—	—	
Low Level Input Voltage	CMOS	—	*1	—	—	1.0	V
	SMTC		*2	—	—	1.0	
Input Current	"H" Level	—	$V_{IN} = V_{DD}$ *3	-10	—	10	$\mu A$
	"L" Level	—	$V_{IN} = V_{SS}$ *3	-10	—	10	
Output Voltage	"H" Level	—	$I_{OH} = -1mA$ *4	$V_{DD} - 1.0$	—	—	V
			$I_{OH} = -4mA$ *5	$V_{DD} - 1.0$	—	—	
	"L" Level	—	$I_{OL} = 1mA$ *6	—	—	1.0	
			$I_{OL} = 4mA$ *5	—	—	1.0	
SMT Hysteresis Voltage	$V_H$	—	*2	—	0.6	—	V

\*1 CKCI, TEST0, 1, RESETN, CKPI, DCPI

\*2 CLMPT, VDCN, HDCN, SCL, SDA, VDPN, HDPN (SDA is inputted)

\*3 CKCI, TEST0, 1, RESETN, CKPI, DCPI, CSN, VDCN, HDCN, SCL, SDA, VDPN, HDPN, TESIO0~5 (SDA is inputted)

\*4 SDA, TESIO0~5 (SDA is outputted) CLMPT

\*5 CKCO, CKPO, DCPO, YS

\*6 TESIO0~5, SDA (SDA is outputted)

**AC CHARACTERISTICS**

Condition :  $V_{DD} = 5.0V$ ,  $T_a = -20 \sim 70^\circ C$ ,  $V_{SS} = 0V$

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operational Frequency Condition	CKP	—	*1	—	18.0	—	MHz
	CKC	—	*1	—	12.0	—	
Output Leading Trailing Time	tr2	—	$CL = 30.0pF$ *2	—	—	10.0	ns
	tf2	—	$CL = 30.0pF$ *2	—	—	10.0	

\*1 CKPI, CKPO

\*2 CKPO, CKCO, DCPO, YS

ADC Characteristics

Condition :  $V_{DD} = 5.0V$ ,  $T_a = -20 \sim 70^\circ C$ ,  $V_{SS} = 0V$

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Non-Linear Error		ILE	—	$V_{DD} = 5V$ , $V_{REFH} = 5V$ $f_{CKCI} = 12MHz$ (ADCK = 6MHz)	-2.5	—	2.5	LSB
Differential Non-linear Error		DLE	—	$V_{DD} = 5V$ , $V_{REFH} = 5V$ $f_{CKCI} = 12MHz$ (ADCK = 6MHz)	-3.0	—	3.0	LSB
Analog Input Voltage	Full SCA	VIFS	—	$V_{DD} = 5V$ , $V_{REFH} = 5V$ $f_{CKCI} = 12MHz$ (ADCK = 6MHz)	0.88	—	1.06	V
	Zero SCA	VIZS	—	$V_{DD} = 5V$ , $V_{REFH} = 5V$ $f_{CKCI} = 12MHz$ (ADCK = 6MHz)	0	—	0.06	

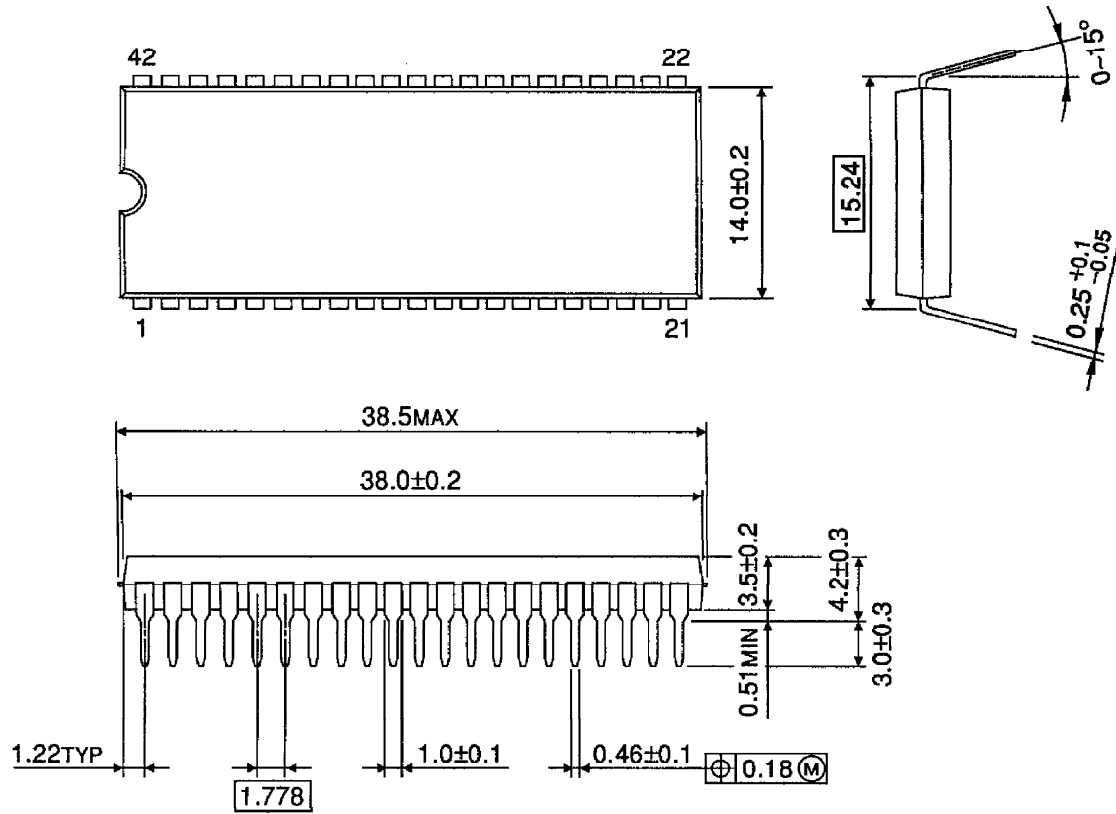
DAC Characteristics

Condition :  $V_{DD} = 5.0V$ ,  $T_a = -20 \sim 70^\circ C$ ,  $V_{SS} = 0V$

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Non-Linear Error		ILE	—	$V_{DD} = 5V$ , $V_{REFL} = 3V$ $f_{CKPI} = 18MHz$ (DACK = 9MHz)	-1.0	—	1.0	LSB
Differential Non-linear Error		DLE	—	$V_{DD} = 5V$ , $V_{REFL} = 3V$ $f_{CKPI} = 18MHz$ (DACK = 9MHz)	-1.0	—	1.0	LSB
Analog Input Voltage	Full SCA	VOFS	—	$V_{DD} = 5V$ , $V_{REFL} = 3V$ $f_{CKPI} = 18MHz$ (DACK = 9MHz)	4.8	—	5.0	V
	Zero SCA	VOZS	—	$V_{DD} = 5V$ , $V_{REFL} = 3V$ $f_{CKPI} = 18MHz$ (DACK = 9MHz)	3.0	—	3.2	
Error Between Channel		Vch	—	$V_{DD} = 5V$ , $V_{REFL} = 3V$ $f_{CKPI} = 18MHz$ (DACK = 9MHz)	-0.2	—	0.2	V
Output Dynamic Range		VReg	—	$V_{DD} = 5V$ , $V_{REFL} = 3V$ $f_{CKPI} = 18MHz$ (DACK = 9MHz)	1.8	—	2.0	$V_{p-p}$

OUTLINE DRAWING  
SDIP42-P-600-1.78

Unit : mm

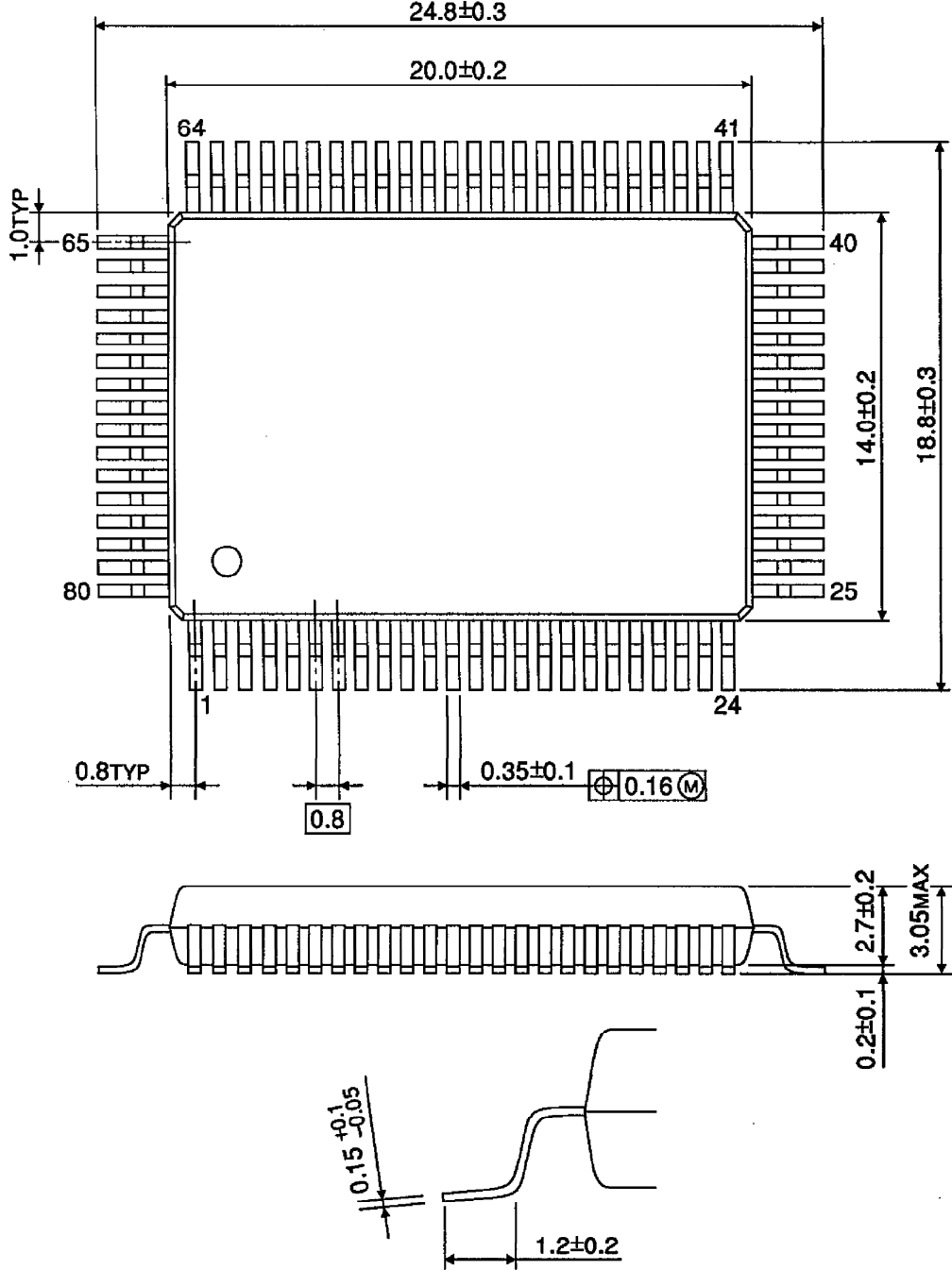


Weight : 4.13g (Typ.)



OUTLINE DRAWING  
QFP80-P-1420-0.80A

Unit : mm



Weight : 1.57g (Typ.)