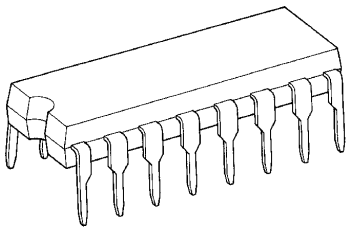
TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB62705CP, TB62705CF, TB62705CFN

8BIT SHIFT REGISTER, LATCHES & CONSTANT CURRENT DRIVERS

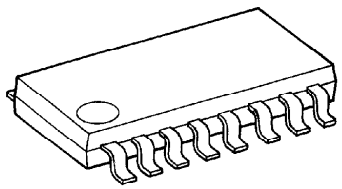
The TB62705CP / CF / CFN are specifically designed for LED and LED DISPLAY constant current drivers.
This constant current output circuits is able to set up external resistor (I_{OUT} = 5~90mA).
This I_C is monolithic integrated circuit designed to be used together with Bi-CMOS process.
The devices consist of 8bit shift register, latch, AND-GATE & Constant Current Drivers.

TB62705CP



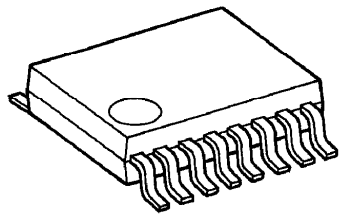
DIP16-P-300-2.54A

TB62705CF



SSOP16-P-225-1.00A

TB62705CFN



SSOP16-P-225-0.65B

FEATURES

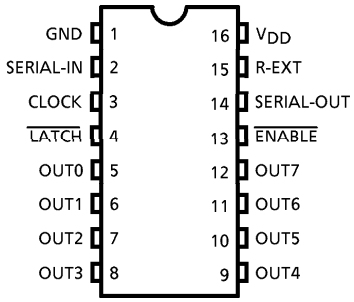
- Constant Current Output : current with one resistor for 5 to 90mA.
- Maximum Clock Frequency : f_{CLK} = 15 (MHz) (Cascade Connecte Operate, T_{opr} = 25°C)
- 5V C-MOS Compatible Input
- Package : DIP16-P-300-2.54A (TB62705CP)
  SSOP16-P-225-1.00A (TB62705CF)
  SSOP16-P-225-0.65B (TB62705CFN)
- Constant Output Current Matching :

OUTPUT-GND VOLTAGE	CURRENT MATCHING	OUTPUT CURRENT
≧0.4V	±6.0%	5~40mA
≧0.7V	±6.0%	5~90mA

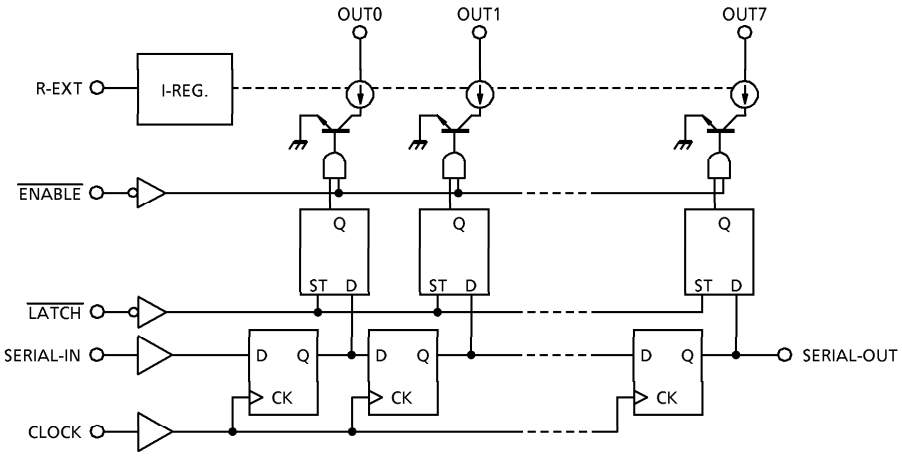
Weight
DIP16-P-300-2.54A : 1.11g (Typ.)
SSOP16-P-225-1.00A : 0.14g (Typ.)
SSOP16-P-225-0.65B : 0.07g (Typ.)

961001EBA1

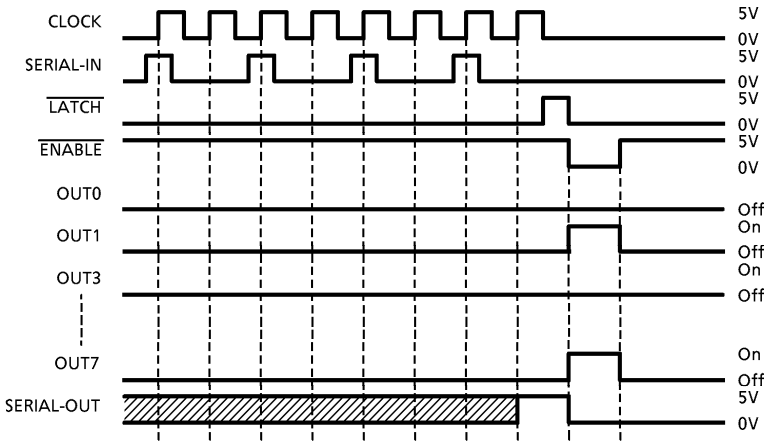
PIN CONNECTION (Top view)



BLOCK DIAGRAM



TIMING DIAGRAM



(Note) Latches are level sensitive, not rising edges sensitive and not syncronus CLOCK.
Input of LATCH-terminal to H Level, data passes latches, and input to L level, data hold latches.
Input of ENABLE-terminal to H level, all output (OUT0~7) do off.

TERMINAL DISCRIPTION

PIN No.	PIN NAME	FUNCTION
1	GND	GND terminal for control logic.
2	SERIAL-IN	Input terminal of a serial-data for shift-register.
3	CLOCK	Input terminal of a clock for data shift to up-edge.
4	$\overline{\text{LATCH}}$	nput terminal of a data strobe. Latches passes data with "H" level input of $\overline{\text{LATCH}}$-terminal, and hold data with "L" level input.
5~12	OUT0~7	Output terminals.
13	$\overline{\text{ENABLE}}$	Input terminal of output enable. All outputs (OUT0~7) do off with "H" level input of $\overline{\text{ENABLE}}$-terminal, and do on with "L" level input.
14	SERIAL-OUT	Output terminal of serial-data for next SELIAL-IN terminal.
15	R-EXT	Input terminal of connects with a resister for to set up all output current.
16	V_{DD}	5V Supply voltage terminal

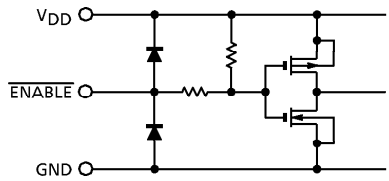
TRUTH TABLE

CLOCK	$\overline{\text{LATCH}}$	$\overline{\text{ENABLE}}$	SERIAL-IN	OUT0 ··· OUT5 ··· OUT7	SERIAL-OUT
UP	H	L	D_n	D_n ··· D_{n-5} ··· D_{n-7}	D_{n-7}
UP	L	L	D_{n+1}	No change	D_{n-6}
UP	H	L	D_{n+2}	D_{n+2} ··· D_{n-3} ··· D_{n-5}	D_{n-5}
DOWN	X	L	D_{n+3}	D_{n+2} ··· D_{n-3} ··· D_{n-5}	D_{n-5}
DOWN	X	H	D_{n+3}	Off	D_{n-5}

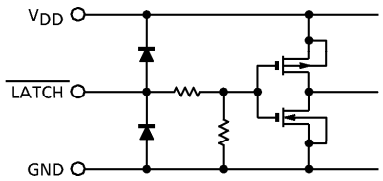
(Note) OUT0~7 = on in case of D_n = H level and OUT0~7 = off in case of D_n = L level.
A resistor is connected with R-EXT and GND accompanied with outside, and it is necessary that a correct power supply voltage is supplied.

EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS

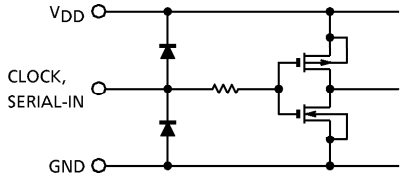
1. $\overline{\text{ENABLE}}$ terminal



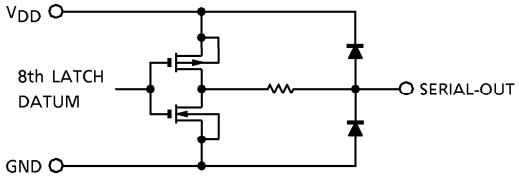
2. $\overline{\text{LATCH}}$ terminal



3. CLOCK, SERIAL-IN terminal



4. SERIAL-OUT terminal



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	0~7.0	V
Input Voltage	V_{IN}	−0.4~V_{DD} + 0.4	V
Output Current	I_{OUT}	90	mA
Output Voltage	V_{CE}	−0.5~17.0	V
Clock Frequency	f_{CK}	15	MHz
GND Terminal Current	I_{GND}	720	mA
Power Dissipation	P_D	1.47 (CP-type : FREE AIR, Ta = 25°C)	W
		0.78 (CF / CFN-type : ON PCB, Ta = 25°C)	
Thermal Resistance	$R_{th\ (j-a)}$	85 (CP-type : FREE AIR, Ta = 25°C)	°C / W
		160 (CF / CFN-type : ON PCB, Ta = 25°C)	
Operating Temperature	T_{opr}	−40~85	°C
Storage Temperature	T_{stg}	−55~150	°C

(Note) CP type : Ambient temperature delated above 25°C in the proportion of 11.8mW / °C
CF and CFN type : Ambient temperature delated above 25°C in the proportion of 6.3mW / °C

RECOMMENDED OPERATING CONDITION (Ta = −40~85°C unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	—	4.5	5.0	5.5	V
Output Voltage	V_{OUT}	—	—	—	15.0	V
Output Current	I_O	OUTn, DC 1 circuit	5	—	88	mA
	I_{OH}	SERIAL-OUT	—	—	1.0	
	I_{OL}	SERIAL-OUT	—	—	−1.0	
Input Voltage	V_{IH}	—	0.7 V_{DD}	—	V_{DD} + 0.3	V
	V_{IL}	—	−0.3	—	0.3 V_{DD}	
LATCH Pulse Width	$t_{w\ LAT}$	V_{DD} = 4.5~5.5V	100	—	—	ns
CLOCK Pulse Width	$t_{w\ CLK}$		50	—	—	ns
ENABLE Pulse Width	$t_{w\ EN}$		4500	—	—	ns
Set-up Time for DATA	$t_{setup\ (D)}$		60	—	—	ns
Hold Time for DATA	$t_{hold\ (D)}$		20	—	—	ns
Set-up Time for LATCH	$t_{setup\ (L)}$		100	—	—	ns
Hold Time for ENABLE	$t_{hold\ (L)}$		60	—	—	ns
Clock Frequency	f_{CK}	Cascade operation	10.0	—	—	MHz
Power Dissipation	P_D	Ta = 85°C (CP-type FREE AIR)	—	—	0.82	W
		Ta = 85°C (CF / CFN-type ON PCB)	—	—	0.40	

ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0V, Ta = 25°C unless otherwise noted)

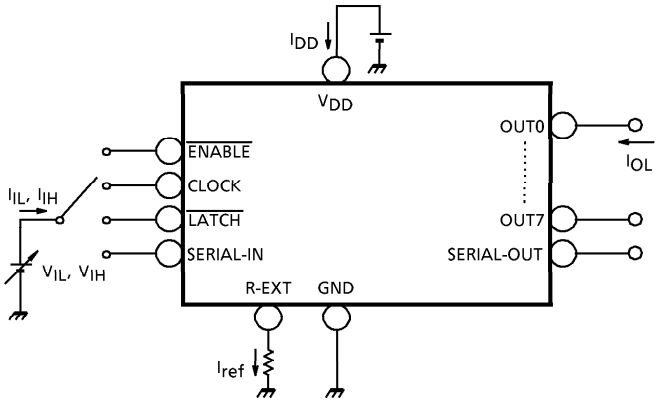
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	CONDITION		MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" Level	V_{IH}	—	—		0.7 V_{DD}	—	V_{DD}	V
	"L" Level	V_{IL}	—	—		GND	—	0.3 V_{DD}	
Output Leakage Current		I_{OH}	—	V_{OH} = 15.0V		—	—	10	μA
Output Voltage	S-OUT	V_{OL}	—	I_{OL} = 1.0mA		—	—	0.4	V
		V_{OH}	—	I_{OH} = − 1.0mA		4.6	—	—	
Output Current 1		I_{OL1}	—	V_{CE} = 0.7V	R_{EXT} = 470Ω (Include skew)	34.1	40.0	45.9	mA
		I_{OL2}	—	V_{CE} = 0.4V		33.7	39.5	45.3	
	Current Skew	ΔI_{OL1}	—	I_O = 40mA, V_{CE} = 0.4V	R_{EXT} = 470Ω	—	± 1.5	± 6.0	%
Output Current 2		I_{OL3}	—	V_{CE} = 0.7V	R_{EXT} = 250Ω (Include skew)	64.2	75.5	86.8	mA
		I_{OL4}	—	V_{CE} = 0.4V		63.8	75.0	86.2	
	Current Skew	ΔI_{OL2}	—	I_O = 75mA, V_{CE} = 0.7V	R_{EXT} = 250Ω	—	± 1.5	± 6.0	%
Supply Voltage Regulation		% / V_{DD}	—	R_{EXT} = 470Ω, Ta = − 40~85°C		—	1.5	5.0	% / V
Pull-Up Resistor		$R_{IN\ (up)}$	—	—		150	300	600	Ω
Pull-Down Resistor		$R_{IN\ (down)}$	—	—		100	200	400	Ω
Supply Current	"OFF"	$I_{DD\ (off)\ 1}$	—	R_{EXT} = OPEN, OUT1~8 = off		—	0.6	1.2	mA
		$I_{DD\ (off)\ 2}$	—	R_{EXT} = 470Ω, OUT1~8 = off		3.5	5.8	8.0	
		$I_{DD\ (off)\ 3}$	—	R_{EXT} = 250Ω, OUT1~8 = off		6.5	10.7	15.0	
	"ON"	$I_{DD\ (on)\ 1}$	—	R_{EXT} = 470Ω, OUT1~8 = on		7.0	12.0	18.0	
		$I_{DD\ (on)\ 2}$	—	R_{EXT} = 250Ω, OUT1~8 = on		10.0	22.0	32.0	

SWITCHING CHARACTERISTICS (Ta = 25°C unless otherwise noted)

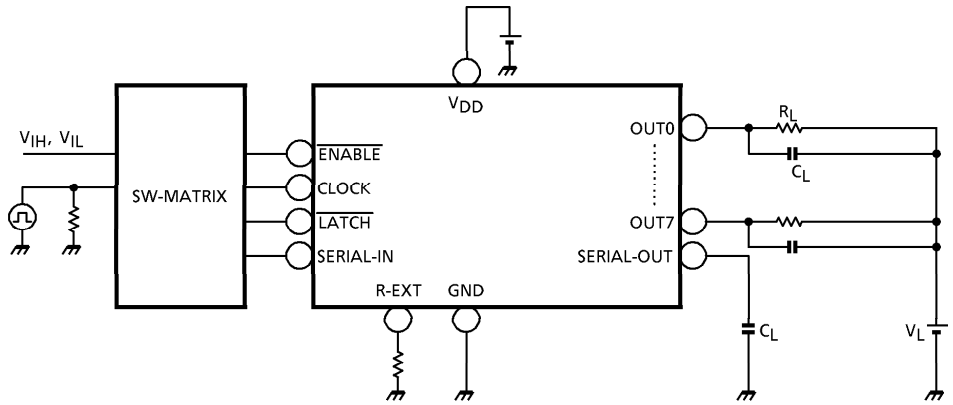
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation Delay Time ("L" to "H")	SIN-OUTn	t_{pLH}	—	V_{DD} = 5.0V V_{CE} = 0.4V V_{IH} = V_{DD} V_{IL} = GND R_{EXT} = 470Ω I_{OUT} = 40mA V_L = 3.0V R_L = 65Ω C_L = 10.5pF	—	1200	1500	ns
	$\overline{LATCH}$-OUTn				—	1200	1500	
	$\overline{ENABLE}$-OUTn				—	1200	1500	
	CLK-SOUT				—	30	70	
Propagation Delay Time ("H" to "L")	SIN-OUTn	t_{pHL}	—		—	700	1000	ns
	$\overline{LATCH}$-OUTn				—	700	1000	
	$\overline{ENABLE}$-OUTn				—	700	1000	
	CLK-SOUT				—	30	70	
Pulse Width	CK	$t_{w\ CLK}$	—		—	20	30	ns
	LATCH	$t_{w\ LAT}$	—		—	10	25	
Set-Up Time for LATCH	L-H	t_{setup}	—		—	25	50	ns
	H-L				—	25	50	
Hold Time for LATCH	L-H	t_{hold}	—		—	0	30	ns
	H-L				—	0	30	
Maximum CLOCK Rise Time		t_r	—		—	—	10	μs
Maximum CLOCK Fall Time		t_f	—		—	—	10	μs
Output Rise Time		t_{or}	—		300	600	1000	ns
Output Fall Time		t_{of}	—		150	300	600	ns

TEST CIRCUIT

DC characteristic



AC characteristic

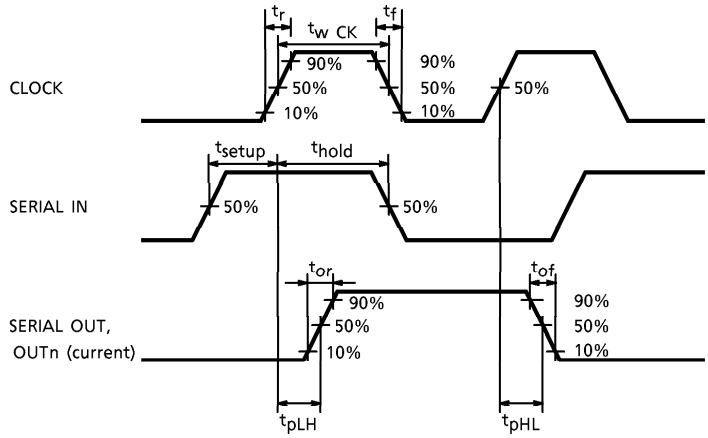


PRECAUTIONS for USING

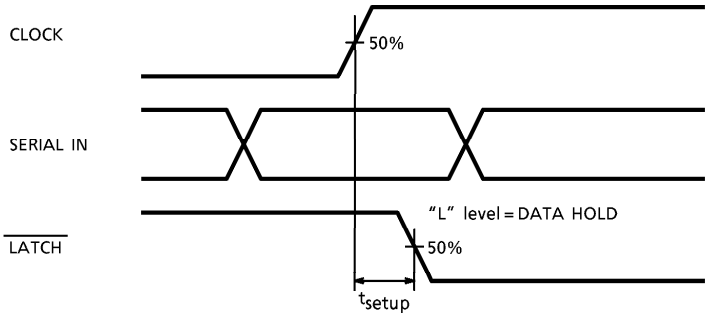
Utmost care is necessary in the design of the output line, V_{CC} (V_{DD}) and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

TIMING WAVEFORM

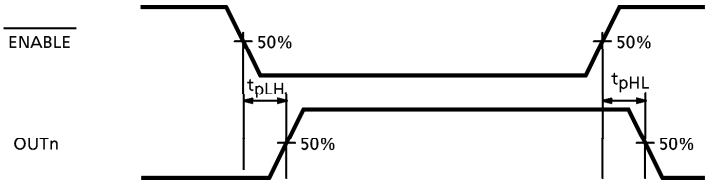
1. CLOCK-SERIAL OUT, OUTn



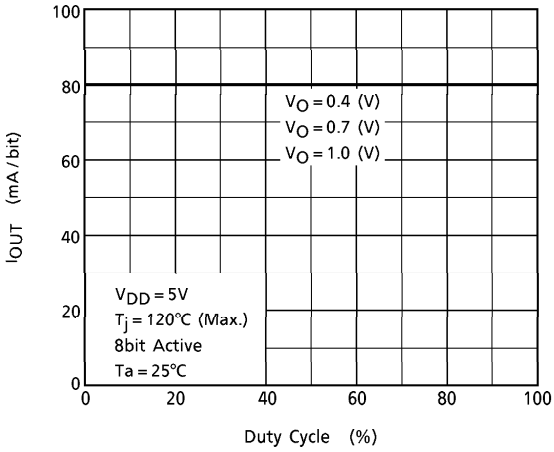
2. CLOCK-$\overline{\text{LATCH}}$



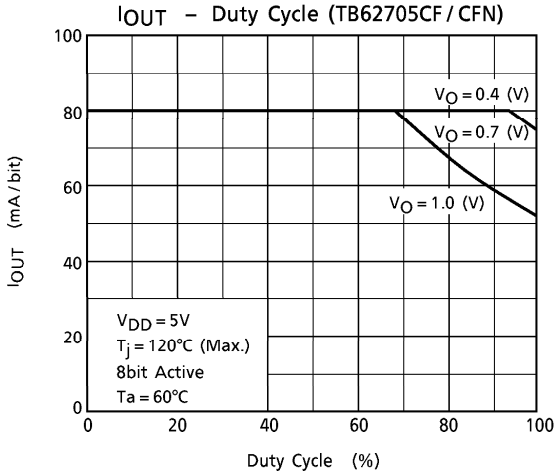
3. $\overline{\text{ENABLE}}$-OUTn



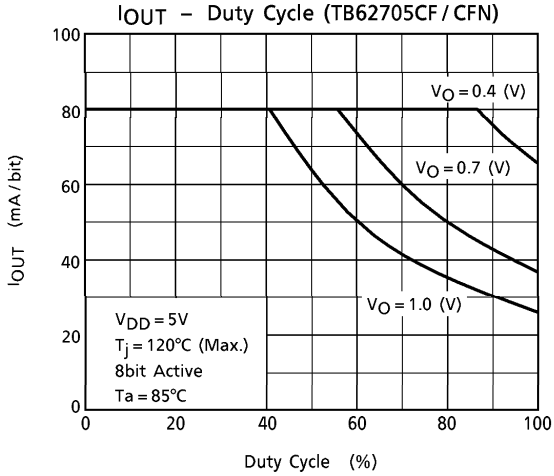
I_{OUT} – Duty Cycle (TB62705CF / CFN)



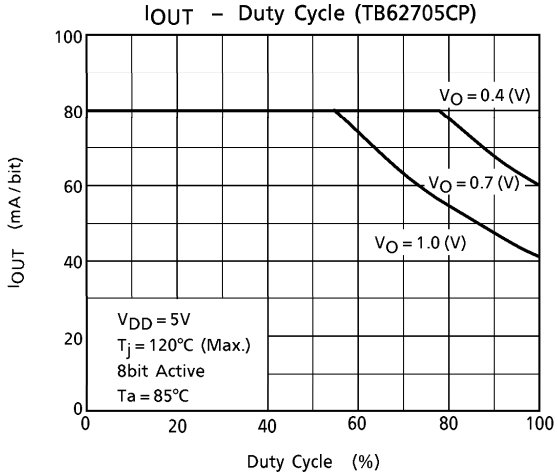
I_{OUT} – Duty Cycle (TB62705CF / CFN)



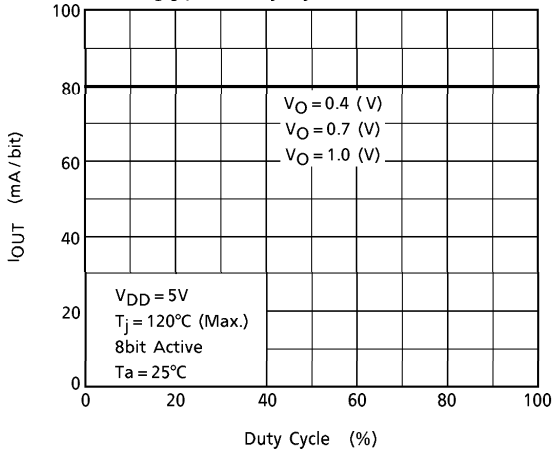
I_{OUT} – Duty Cycle (TB62705CF / CFN)



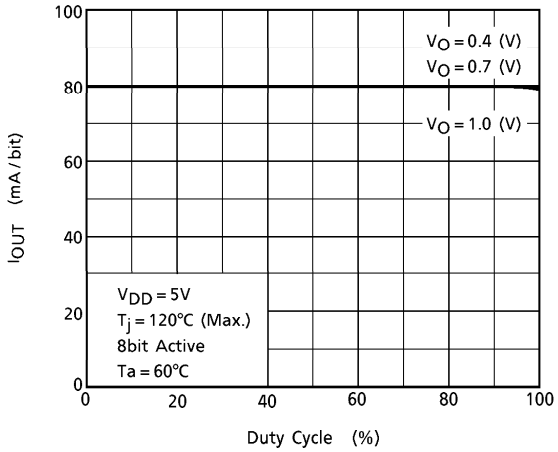
I_{OUT} – Duty Cycle (TB62705CP)



I_{OUT} – Duty Cycle (TB62705CP)



I_{OUT} – Duty Cycle (TB62705CP)



LED DRIVER TB6270X SERIES APPLICATION NOTE

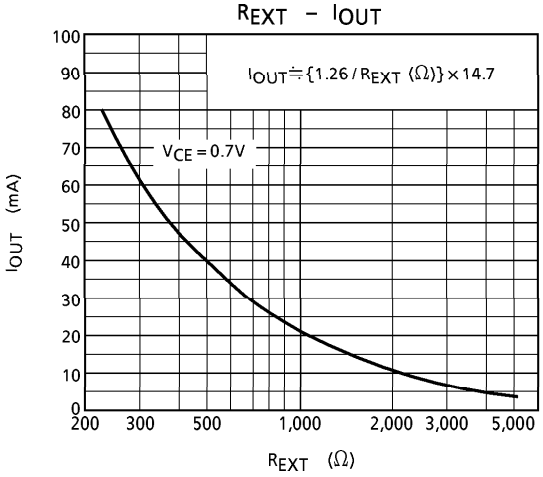
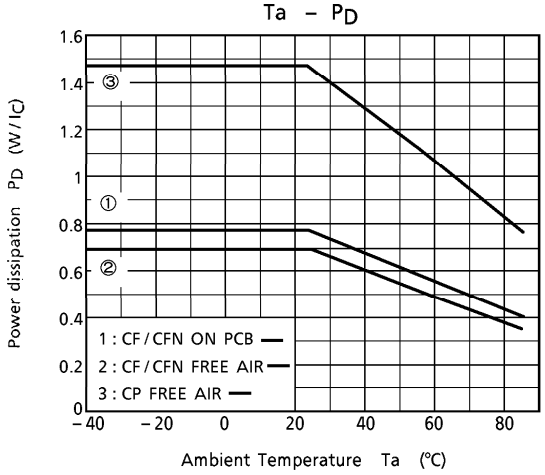


Fig. 1



[1] Output current (I_{OUT})

I_{OUT} is set by the enternal resistor (R-EXT) as shown in Fig1.

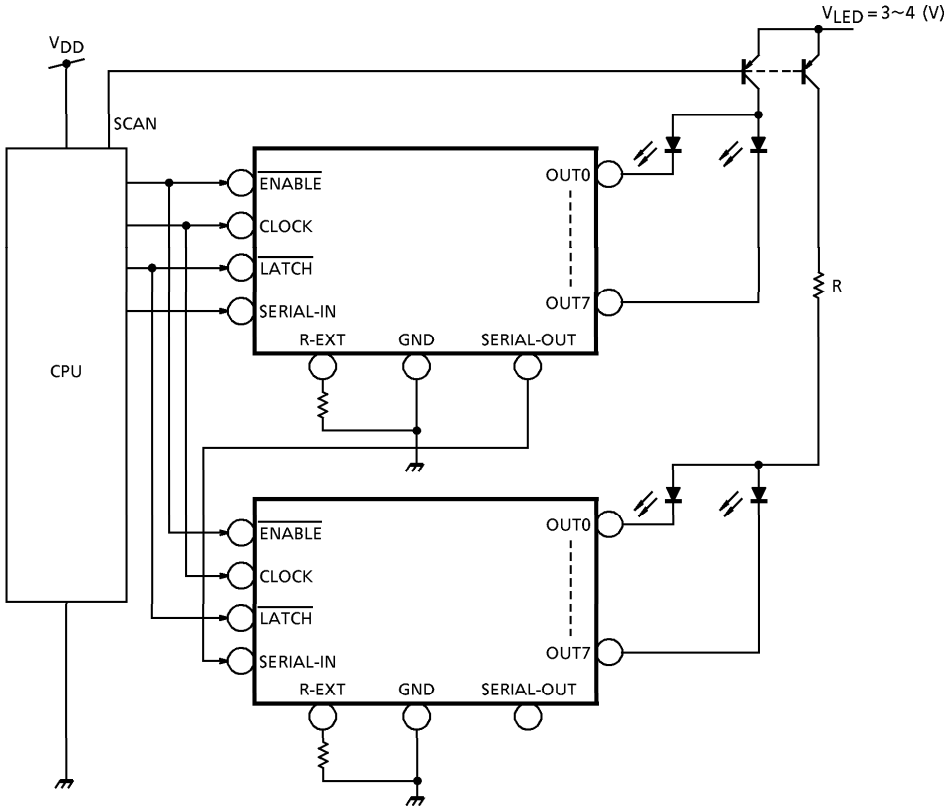
[2] Total supply voltage (V_{LED})

This device can operate 0.4~0.7V (V_O).
When a higher voltage is input to the device, the excess voltage is consumed inside the device, that leads to power dissipation.
In order to minimize power dissipation and loss, we would like to recommend to set the total supply voltage as shown below,

V_{LED} (total supply voltage) = V_{CE} (T_r V_{sat}) + V_f (LED Forward voltage) + V_O (I_C supply voltage)

When the total supply is too high considering the power dissipation of this device, an additional R can decrease the supply voltage (V_O).

PATTERN LAYOUT



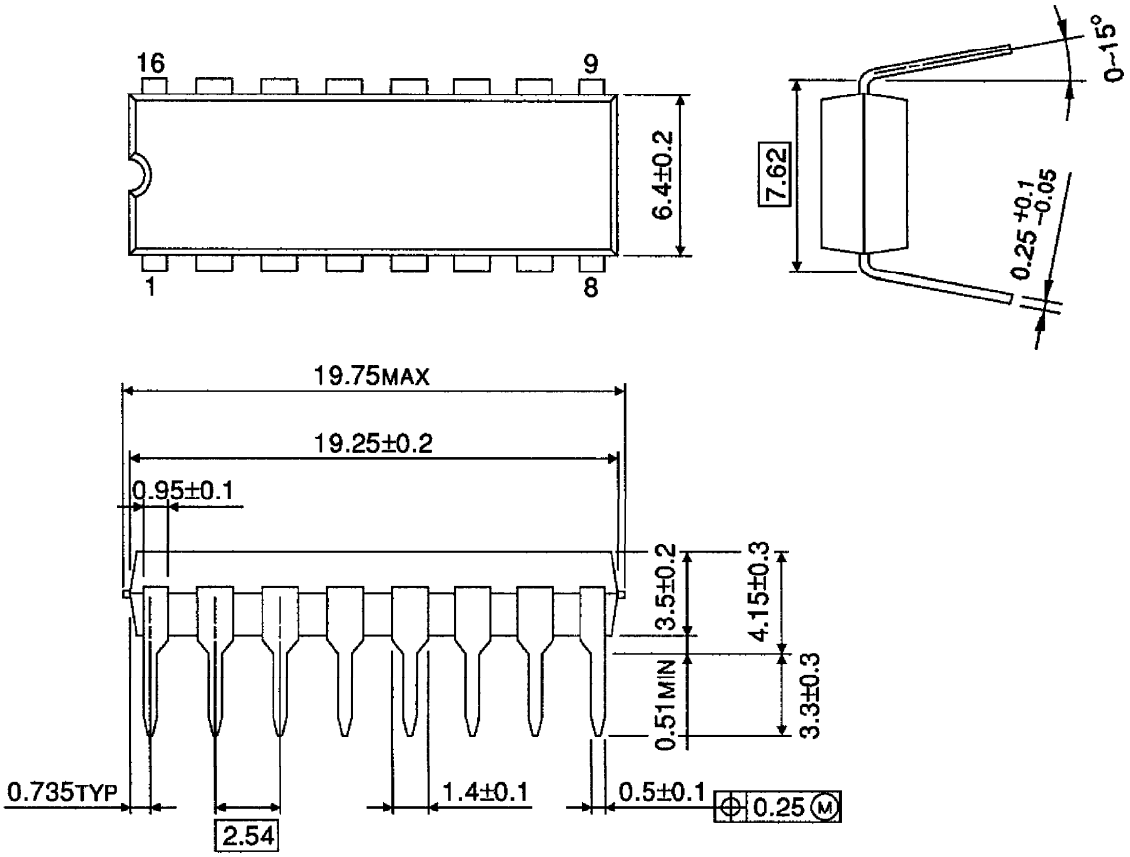
[3] Pattern layout

This device owns only one ground pin that means signal ground pin and power ground pin are common.
If ground pattern layout contains large inductance and impedance, and the voltage between ground and LATCH, CLOCK terminals exceeds 2.5V by switching noise in operation, this device may miss-operate. So we would lile you to pay attention to pattern layout to minimize inductance.

OUTLINE DRAWING

DIP16-P-300-2.54A

Unit : mm

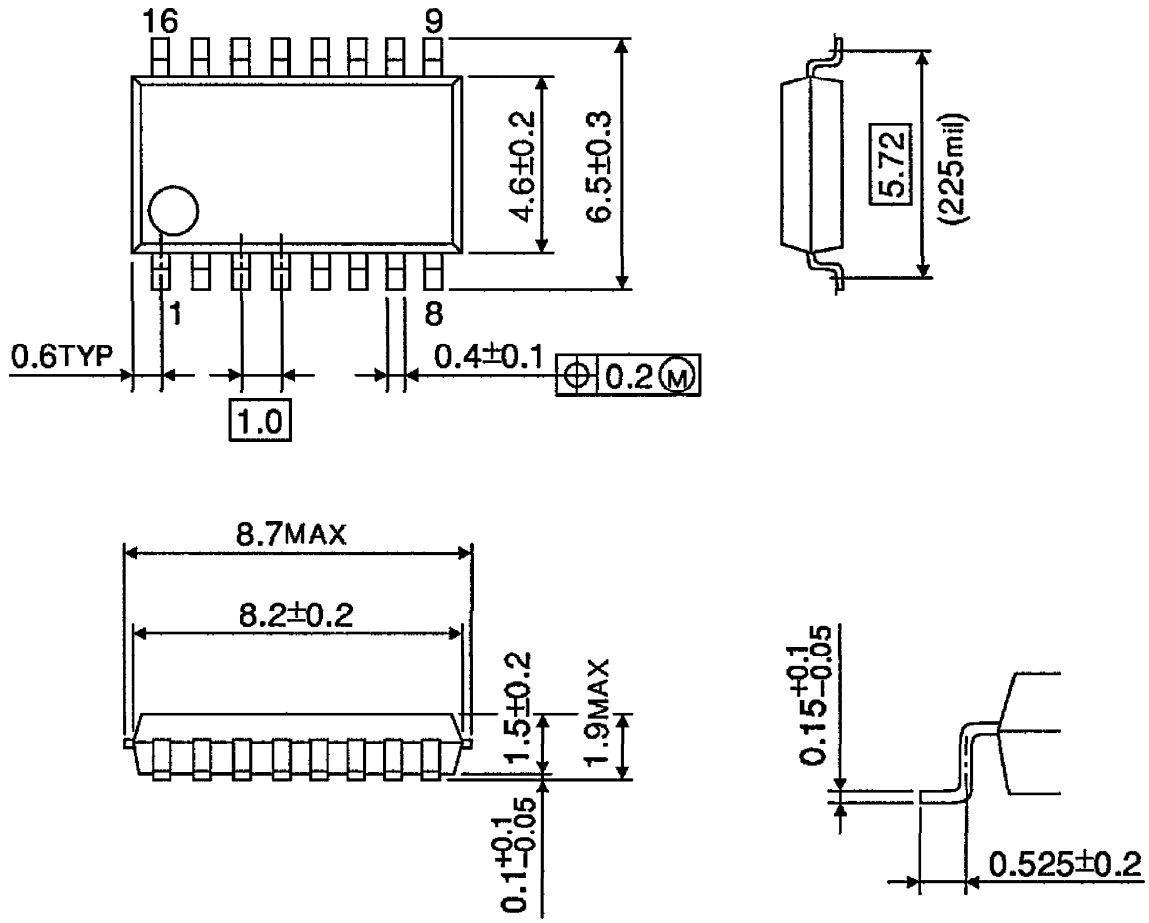


Weight : 1.11g (Typ.)

OUTLINE DRAWING

SSOP16-P-225-1.00A

Unit : mm

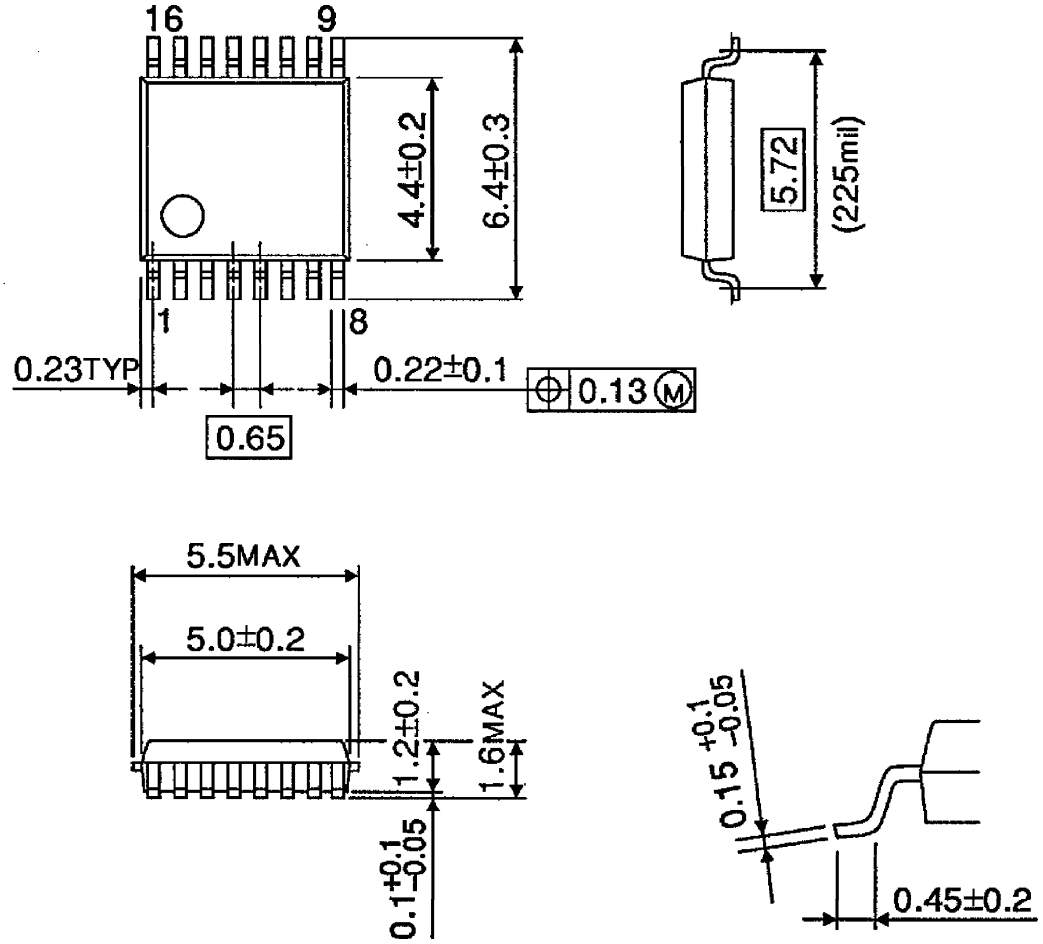


Weight : 0.14g (Typ.)

OUTLINE DRAWING

SSOP16-P-225-0.65B

Unit : mm



Weight : 0.07g (Typ.)