

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

# TC9028AP, TC9028AF

## INFRARED REMOTE CONTROL TRANSMITTING CMOS LSI WITH MICROCONTROLLING

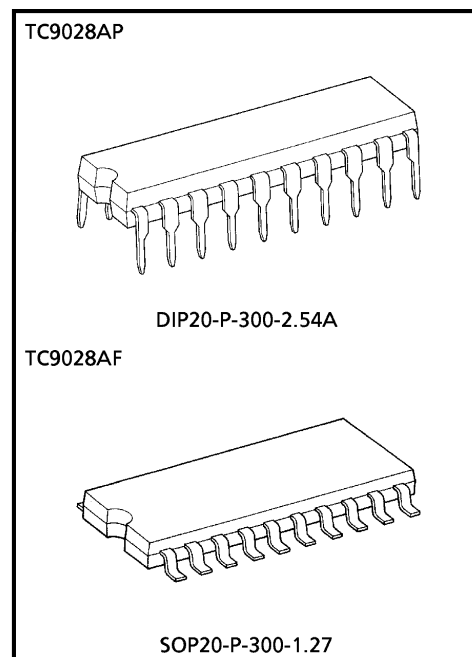
TC9028AP, TC9028AF is CMOS LSI for Infrared Remote Control Transmitting suitable for Remote Controlling TV, VCR, Video Disk, CD-Player etc.

Using a 4bit Microcontroller, various transmittings are structured by a programming.

### FEATURES

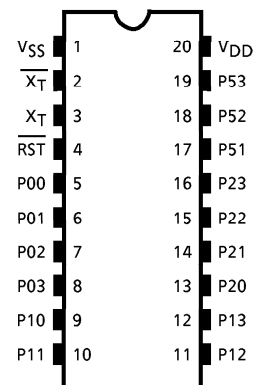
- Low voltage operation : 2.0~4.0V
- Low power dissipation :  $\leq 1\mu A$  (at Hold Function)
- Program memory (ROM) capacity : 768 × 8bit
- Data memory (RAM) capacity : 16 × 4bit
- Instruction : 44kinds
- Timer / Counter : 10~15bit
- I/O port (15pins)
  - I/O : 2ports 8pins
  - Input : 1port 4pins
  - Output : 1port 3pins  
(Including High Current Output)
- Subcarrier frequency :  $f_{osc} / 12, f_{osc} / 8$   
 $f_{osc} / 24, f_{osc} / 16$  (Option)
- Oscillating frequency : 400~800kHz
- Instruction execution time : 11 $\mu s$  (at 455kHz)
- Package : DIP20 [TC9028AP]  
SOP20 [TC9028AF]

(Note) This device is Vulnerable to surge voltages.  
Take it into account when using this device in your system.



Weight  
 DIP20-P-300-2.54A : 1.4g (Typ.)  
 SOP20-P-300-1.27 : 0.48g (Typ.)

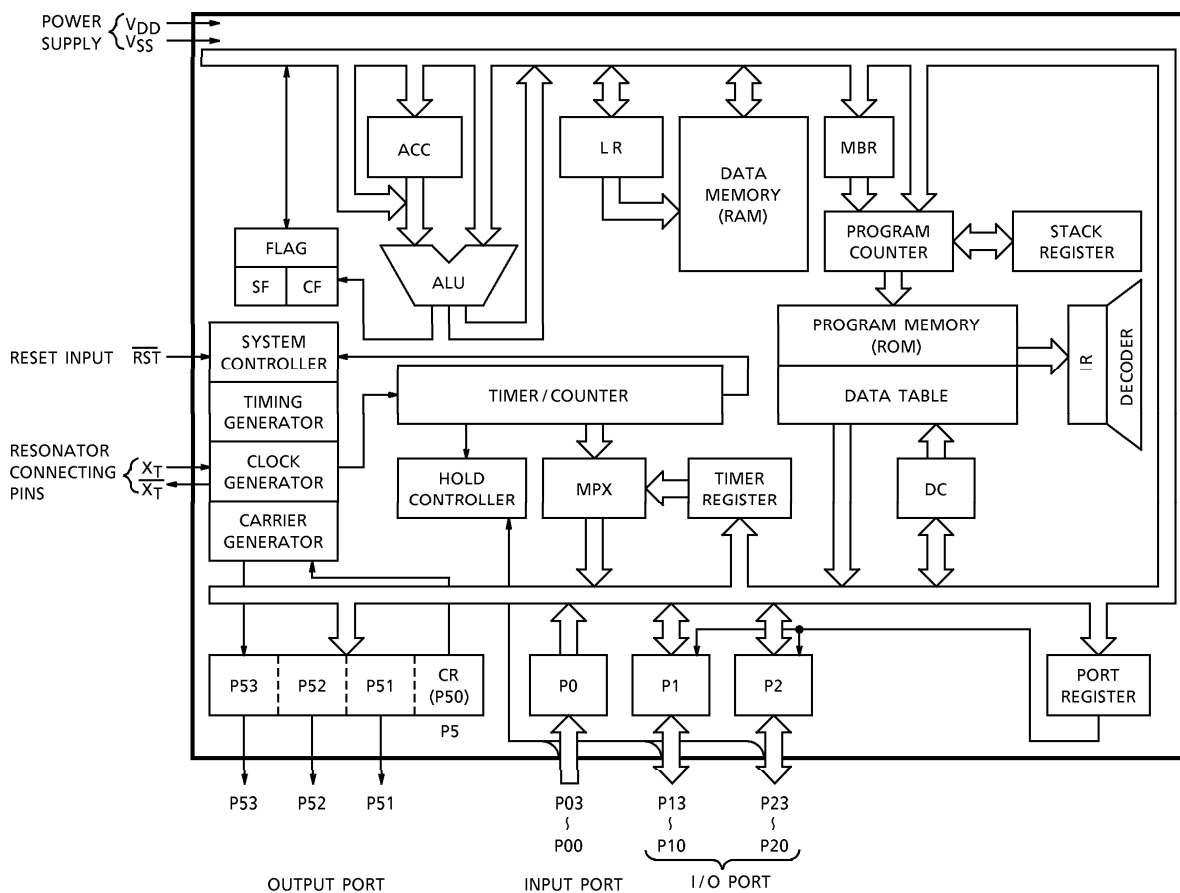
### PIN CONNECTION (TOP VIEW)



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BLOCK DIAGRAM



PIN FUNCTION

PIN No.	SYMBOL	PIN NAME	FUNCTION
1	V <sub>SS</sub>	Power Supply	V <sub>DD</sub> = 2.0~4.0V, 3V (Typ.)
20	V <sub>DD</sub>		
2	X <sub>T</sub>	Output for Osc.	Resonator connecting pins. Connects ceramic resonator with capacitor. Built-in feedback resistance.
3	X <sub>T</sub>	Input for Osc.	
4	R <sub>ST</sub>	Reset Input	R <sub>ST</sub> for going reset. Be held to "L" (≥ 3 instruction cycles)
5~8	P00~P03	Input Port P0	4bit input port. Built-in pulldown resistance.
9~12	P10~P13	I/O Port P1	4bit I/O ports with latch. Input/output mode can be specified by [MOV A, P] instruction. Built-in pulldown resistance.
13~16	P20~P23	I/O Port P2	
17	P51	Output Port P51	Pch open drain output port.
18	P52	Output Port P52	High current output port. For driving indication LED.
19	P53	Output Port P53	High current output port. For driving infrared LED.

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**OPERATION**

## 1. Configuration

- (1) Program counter (PC)
- (2) Memory bank register (MBR)
- (3) Stack register (STACK)
- (4) Data counter (DC)
- (5) Program memory (ROM)
- (6) L register (LR)
- (7) Data memory (RAM)
- (8) Arithmetic and Logic Unit (ALU), Accumulator
- (9) Flags
- (10) Clock generator, Timing generator
- (11) I/O ports
  - a. Port register (PR)
  - b. Command register (CR)
- (12) Timer counter
  - a. Timer register (TR)
  - b. Timer counter output
  - c. Watch dog timer output
- (13) Hold mode control circuit
- (14) Reset circuit

Following is a description of the hardware configuration and operation of the components listed above.

## 2. Internal CPU functions

## 2.1 Program counter (PC)

The program counter is a 10bit binary counter which holds the program memory address of the next instruction to be executed.

The program counter is normally incremented for each instruction fetch.

When branch instructions and subroutine instructions are executed, the values specified in Table 2.1 are set. The program counter is initialized to 0 at reset.

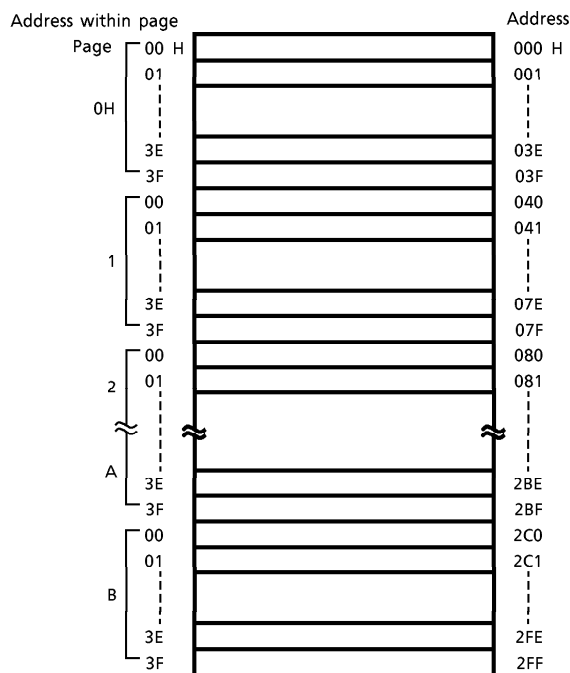


Figure 2.1 Program memory configuration

Table 2.1 Program counter values depending on conditions

INSTRUCTION OR OPERATION		CONDITION		PROGRAM COUNTER (PC)								
				PAGE ASSIGNMENT				ADDRESS SPECIFICATION WITHIN PAGE				
				PC <sub>9</sub>	PC <sub>8</sub>	PC <sub>7</sub>	PC <sub>6</sub>	PC <sub>5</sub>	PC <sub>4</sub>	PC <sub>3</sub>	PC <sub>2</sub>	PC <sub>1</sub>
Instruction Execution	LD MBR, #k + BSS a	SF = 1 (when branch condition is satisfied)		Memory bank register contents				Value directly specified by BSS instruction				
		SF = 0 (when branch condition is not satisfied)		+ 2								
	BSS a	SF = 1	Lower 6 bits of address ≠ 111111		No change				Value directly specified by instruction			
			Lower 6 bits of address = 111111		+ 1				Value directly specified by instruction			
	SF = 0		+ 1									
	CALLS a	—		0	0	0	0	0	Value directly specified by instruction			0
	RET	—		Value restored from stack								
	Instructions other than above	—		+ 1								
Reset	—		0	0	0	0	0	0	0	0	0	0

**2.2 Memory bank register (MBR)**

The memory bank register is a 4bit write-only register. It holds the page specification (upper 4 bits of the program counter) when a branch is made anywhere in program memory.

**2.3 Stack register (STACK)**

The stack is a 10bit register. When the [CALLS a] instruction is executed, the stack register saves the contents of the program counter (return address) before the program jumps to the processing routine.

Only one level of subroutines can be used. When there are two calls, the first return address is overwritten when the second return address is saved to the stack register. When the program returns from the processing routine, execution of the [RET] instruction restores the contents of the stack register to the program counter.

**2.4 Data counter (DC)**

When fixed data stored in the data table in program memory (ROM) are read, the data counter (DC) are used to specify 4 bits of the address.

In addition to transferring data to the accumulator, the data counter is also equipped with increment and decrement functions and can therefore be used as a general-purpose register.

Fixed data stored in the data table can be read using the table look-up instruction.

When the table look-up instruction is executed, the upper 6 bits of the ROM address are "101111" and the lower 4 bits are the contents of the data counter (DC). These bits specify the last 16 bytes (addresses 2F0~2FFH) of program memory for fixed data.

**2.5 Program memory (ROM)**

Program memory stores program and fixed data. The next instruction to be executed is read from the address indicated by the program counter.

Physical program memory doesn't exist in addresses 300~3FFH.

When this area is read on the program, 7FH ([NOP] instruction) is read.

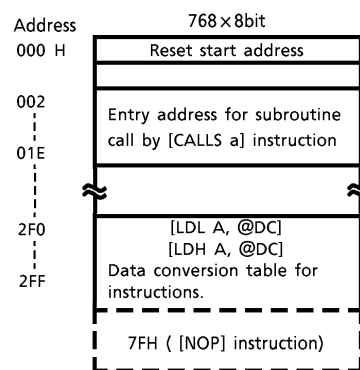


Figure 2.2 Program memory map



**2.9 Flags (FLAG)**

There are two types of flags: carry flag (CF) and status flag (SF). These are set and cleared according to conditions specified by instructions. The status flag is initialized to 1 at reset.

**2.10 Clock generator, Timing generator**

Figure 2.6 shows the clock generator and timing generator configuration.

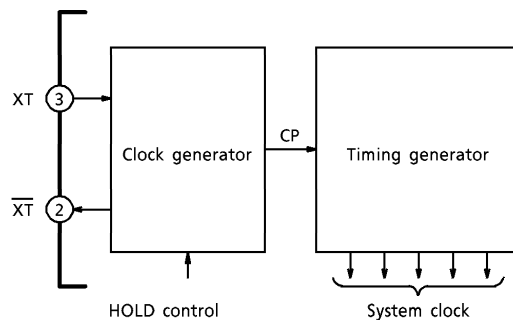


Figure 2.6 Clock generator and timing generator

**2.10.1 Clock generator**

The clock generator is a circuit which generates the fundamental clock pulse (CP) as the basis for the system clock supplied to the CPU. The fundamental clock is easily established by connecting the oscillator to the XT and XT pins. A clock can also be input from an external oscillator.

Clock input to the XT pin is used as the fundamental clock. The clock generator stops oscillation during hold mode.

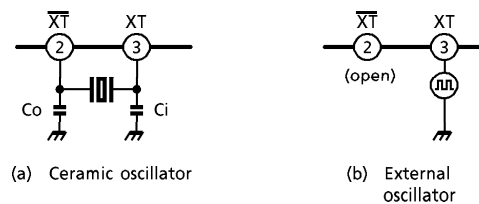


Figure 2.7 Typical oscillator connections

**2.10.2 Timing generator**

The timing generator is a circuit which uses the fundamental clock to generate various system clocks for the CPU and peripheral hardware.

2.10.3 Instruction cycle

Instructions and internal hardware operations are executed in sync with the fundamental clock. The minimum unit of instruction execution is called the instruction cycle. TC9028AP and TC9028AF has 1 and 2-cycle instructions. An instruction cycle consists of 5 states (S0-S4). Each state consists of 1 fundamental clock. Therefore, the instruction cycle time is  $5/f_c$  [s].

3. Peripheral hardware functions

3.1 Ports

The following functions are executed using I/O instructions (4 types): key scan, send signal output, send display output, internal circuit control.

This system features the 2 types of ports listed below. Addresses (00-05H) are allocated to these ports:

- ① I/O ports : key scan, send signal output, send display output
- ② Command register : internal circuit control

Ports are selected by specifying port addresses with I/O instructions. The port register controls input and output of programmable I/O ports.

3.1.1 Port register (PR)

The port register is a 4bit write-only register. It is used for selecting input or output mode for programmable I/O ports. Since an option is used to select input or output mode during hold, the port register cannot select the mode.

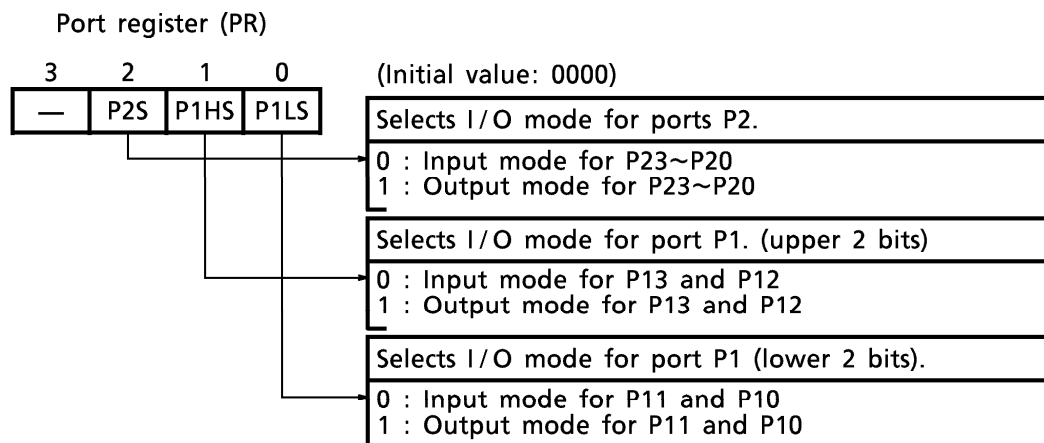


Figure 3.1 Programmable I/O port control using port register



3.1.2 I/O ports

TC9028AP and TC9028AF has 4 I/O ports with 15 pins.

- (1) Port P0: 4bit input
- (2) Ports P1, P2 : 4bit programmable input/output
- (3) Port P5: 3bit output (P52 and P53 are for large current output)

(1) Port P0 (P03~P00)

Port P0 is a 4bit input port. All its pins are equipped with hold mode cancellation function.

(2) Ports P1 (P13~P10), P2 (P23~P20)

Ports P1, P2 are 4bit programmable I/O ports with latches.

Input or output can be selected by program. (8 types)

Latches are initialized to 1 at reset.

Pins which can be switched using an option to input mode during hold mode are equipped with hold mode cancellation functions.

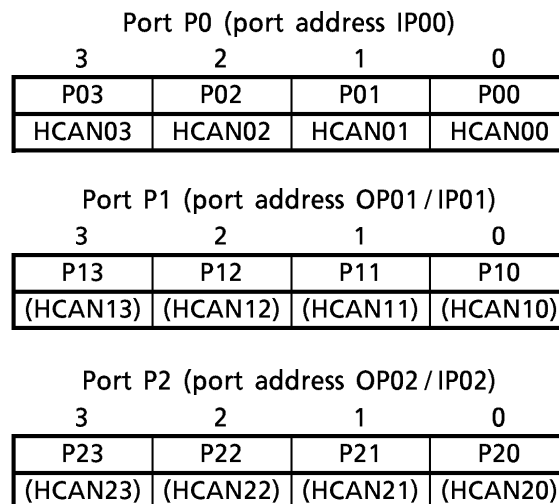


Figure 3.2 Ports P0, P1 and P2

(3) P5 (P53~P51) port

Port P5 is a 3bit output port with a latch.

P51 is for P-ch open-drain output. An option allows it to be used for push / pull output.

The latch is initialized to 0 at reset.

P52 is for large current output for driving the send display LED.

The output latch is initialized to 1 at reset.

P53 is for large current output for driving the infrared LED. Resetting the output latch to 1 outputs  $f_{OSC}/12$  (duty 1/3) or  $f_{OSC}/8$  (duty 1/2) sub-carrier frequency for modulation. An option allows selection of  $f_{OSC}/24$  (duty 1/3) or  $f_{OSC}/16$  (duty 1/2) sub-carrier frequency. Sub-carrier frequency (duty) is selected by the command register. The latch is initialized to 0 at reset.

The LSB (P50) of the port P5 is used for selecting the sub-carrier frequency (duty) output from P53 using the write-only command register.

The latch is initialized to 0 at reset.

Although port P5 is an output port, when an input instruction is executed, P5 can read timer/counter output (IT3~IT0).

Port P5, Command Register (port address OP05) and, Timer/Counter Output (port address IP05)

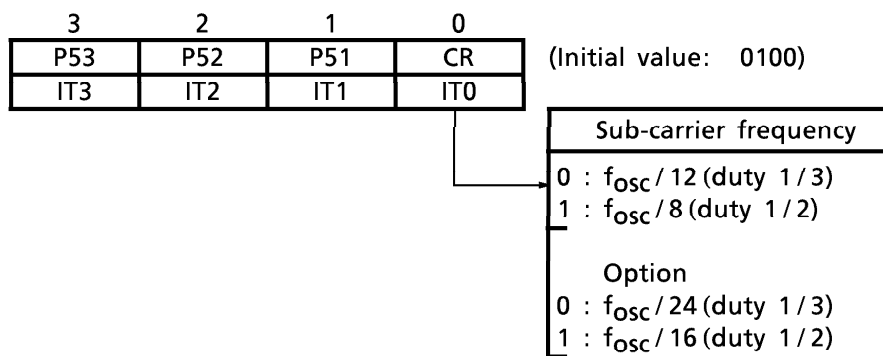


Figure 3.3 Port P5

### 3.2 Timer/counter

The timer/counter is a 17 step binary counter used to divide the fundamental clock. It outputs a pulse with a cycle selected from steps 10 through 15.

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The uses of the timer/counter are listed below. The timer/counter is cleared to 0 at reset, when a timer reset instruction (TMRST) is executed, and when hold mode is cancelled.

- ① Timer generating  $f_C/2^{10} \sim f_C/2^{15}$  [Hz] pulses
- ② Watchdog timer
- ③ Warming-up timer when hold mode is cancelled

3.2.1 Timer register (TR)

The timer register is a 4bit write-only register.  
 It selects the mode when the timer status is read.  
 The timer register is initialized to 0 at reset.

Timer register (TR)

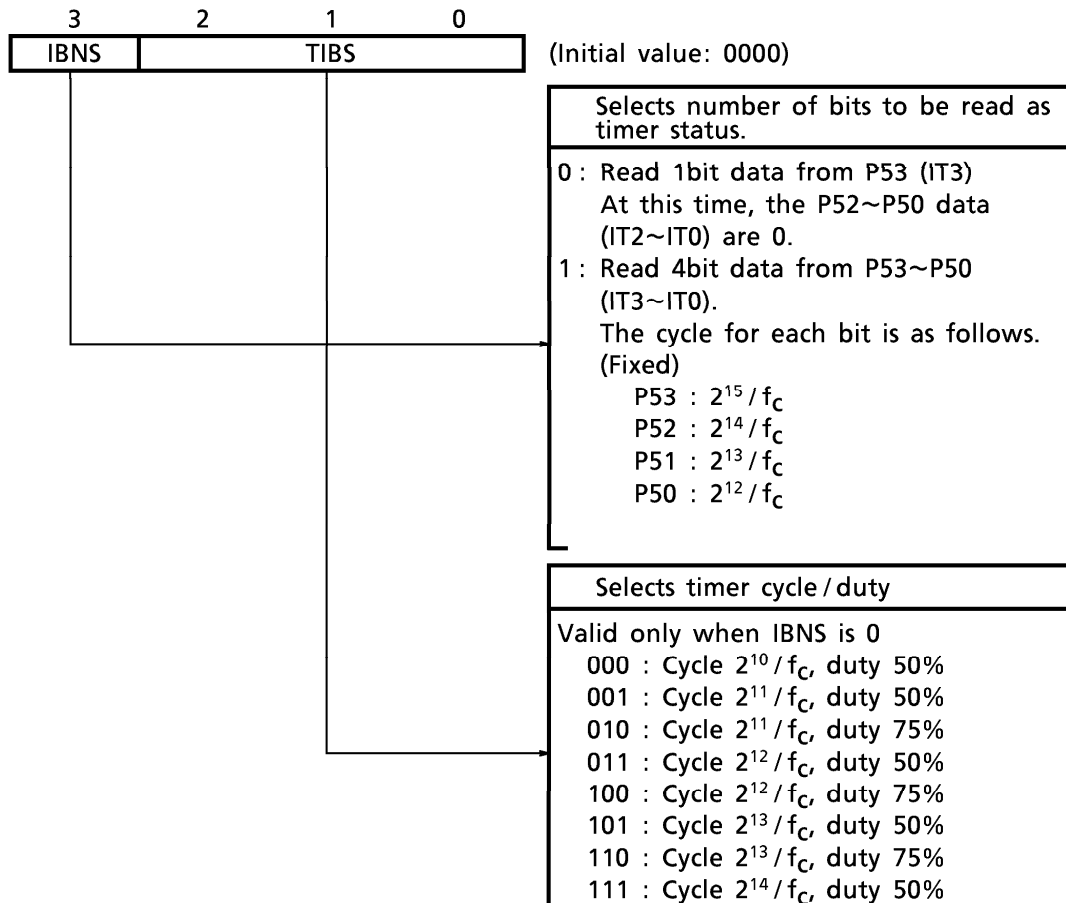


Figure 3.4 Timer/counter output mode control using timer register

3.2.2 Timer counter output (IT3~IT0)

The timer counter is cleared to 0 at reset. It is incremented, from 0, each time the fundamental clock is input. The timer counter output transfers the inverted value of the timer counter to the accumulator or data memory using port P5 input instructions [IN %IP05, A] and [IN %IP05, @LR]. Thus, 1 is read at reset. (Decrement)

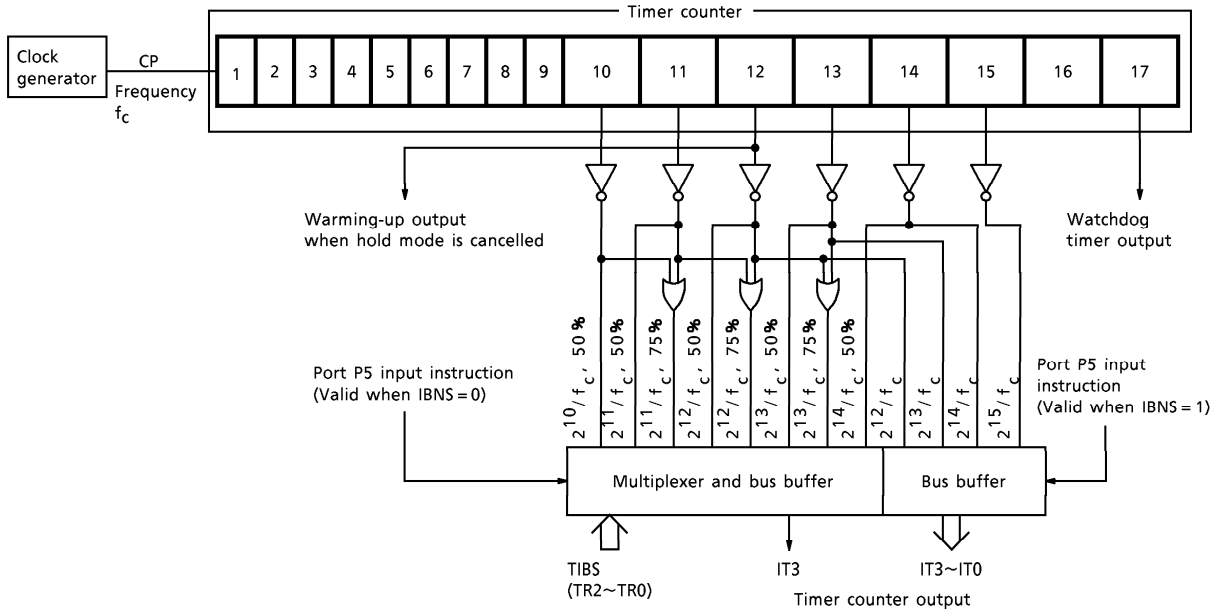


Figure 3.5 Timer counter configuration

3.2.3 Watchdog timer output

The watchdog timer output becomes active  $2^{16}/f_c$ (s) after the timer is reset. If the timer is not reset again before timer reset, TC9028AP and TC9028AF regards this as a CPU runaway and resets the CPU.

4. Low power consumption operation

TC9028AP and TC9028AF features a hold mode for low power consumption operation.

4.1 Hold mode

The hold function stops system operation and holds the internal states in effect immediately before stopping.

The hold function is controlled by the port hold mode cancellation function and by the hold instruction [HOLD]. The hold cancel function is valid with pins P00~P03, and with pins P10~P13, P20~P23 (HCAN pins) which are switched using and option to input mode during hold mode.

#### 4.1.1 Hold mode

Hold mode is activated by executing the hold instruction [HOLD]. Hold mode continues as long as the HCAN pins are at low level.

The following states are held during hold mode.

- ① Oscillation stops and all internal operations stop.
- ② The timer counter is cleared to 0.
- ③ Data memory, registers, and port latches hold the states immediately before entering hold mode. (Note that the status flag is set to 1.)
- ④ The program counter holds the 2 addresses after the hold instruction.  
(After hold mode is cancelled, execution resumes with the instruction following the hold instruction.)

#### 4.1.2 Hold mode cancellation

Hold mode is cancelled and normal operation resumes when high level is input to the HCAN pins during hold mode.

Hold mode is cancelled in the following sequence.

- ① Oscillation begins.
- ② Warming-up for the time required to stabilize oscillation. Internal operation remains stopped during warming-up.  
The warming-up time is  $2^{11} / f_C(s)$ .
- ③ After the warming-up time has elapsed, normal operation resumes from the instruction following the hold instruction.

(Note) The fundamental clock is divided by the interval timer. If the oscillation frequency fluctuates after hold mode is cancelled, the warming-up time is not exactly the same as the value given above. Thus, the warming-up time has allowance.

Hold mode is also cancelled by setting the RST pin to low level. In this case, the reset operation is performed immediately. Since normal operation begins at the same time the reset operation is cancelled, the RST pin must be kept at the low level for the warming-up time until oscillation becomes stable.

If input to the HCAN pin is at high level, executing the hold instruction does not enter hold mode but instead moves immediately to the cancellation sequence (warming-up).

The warming-up time in this case is an undefined value between  $0 \sim 2^{11} / f_C(s)$ .

Therefore, when the hold instruction is executed, input to the HCAN pin must be set to low level.

5. Reset

If the RST pin remains at low level for more than a minimum of 3 instruction cycles (15 fundamental clocks) when the power supply voltage is within the operating voltage range and oscillation is stable, the system is reset and the internal states are initialized.

When the RST pin is set to high level, the reset operation is cancelled and execution of the program at address 000H begins.

Table 5.1 Initialization of internal states by reset

INTERNAL HARDWARE	INITIAL VALUE	INTERNAL HARDWARE	INITIAL VALUE
Program Counter (PC)	000H	Output Latches (I/O ports)	See description of I/O circuits.
Status Flag (SF)	1		
Port Register (PR)	0000B		

Instruction list

FUNCTION	MNEMONIC	OBJECT CODE		OPERATION	FLAG		CYCLES	
		BINARY	HEXADECIMAL		CF	SF		
Transfer	LD A, @LR	0000	0110	06	Acc←RAM { LR }	—	1	1
	LD A, x	1001	0xxx	90 + x	Acc←RAM { x }	—	1	2
	LDL A, @DC	0110	0111	67	Acc←ROM { DC } L	—	1	2
	LDH A, @DC	0110	0110	66	Acc←ROM { DC } H	—	1	2
	ST A, @LR	0111	0110	76	RAM { LR } ←Acc	—	1	1
	ST #k, @LR	0011	kkkk	3k	RAM { LR } ←k	—	1	1
	ST A, x	1001	1xxx	98 + x	RAM { x } ←Acc	—	1	2
	LD A, #k	0001	kkkk	1k	Acc←k	—	1	1
	LD L, #k	0010	kkkk	2k	LR←k	—	1	1
	MOV L, A	0000	1111	0F	Acc←LR	—	1	1
	MOV A, L	0000	1100	0C	LR←Acc	—	1	1
	MOV D, A	0000	1110	0E	Acc←DC	—	1	1
	MOV A, D	0000	1101	0D	DC←Acc	—	1	1
	MOV A, P	0111	1110	7E	PR←Acc	—	1	1
MOV A, T	1000	1010	8A	TR←Acc	—	1	1	
Input/Output	IN %p, A	0110	0ppp	60 + p	Acc←PORT { p }	—	$\bar{Z}$	2
	IN %p, @LR	0110	1ppp	68 + p	RAM { LR } ←PORT { p }	—	$\bar{Z}$	2
	OUT A, %p	0111	0ppp	70 + p	PORT { p } ←Acc	—	1	2
	OUT @LR, %p	0111	1ppp	78 + p	PORT { p } ←RAM { LR }	—	1	2

FUNCTION	MNEMONIC	OBJECT CODE		OPERATION	FLAG		CYCLES	
		BINARY	HEXADECIMAL		CF	SF		
Operation (Arithmetic & Logical)	ADD A, @LR	0000	0011	03	$Acc \leftarrow Acc + RAM \{ LR \}$	—	$\bar{C}$	1
	ADDC A, @LR	0000	0100	04	$Acc \leftarrow Acc + RAM \{ LR \} + CF$	C	$\bar{C}$	1
	ADD A, #k	0100	kkkk	4k	$Acc \leftarrow Acc + k$	—	$\bar{C}$	1
	ADD L, #k	0101	kkkk	5k	$LR \leftarrow LR + k$	—	$\bar{C}$	2
	SUBRC A, @LR	0000	0101	05	$Acc \leftarrow RAM \{ LR \} - Acc - \bar{CF}$	C	C	1
	INC @LR	0000	1001	09	$RAM \{ LR \} \leftarrow RAM \{ LR \} + 1$	—	$\bar{C}$	1
	DEC @LR	0000	1000	08	$RAM \{ LR \} \leftarrow RAM \{ LR \} - 1$	—	C	1
	INC D	0000	1011	0B	$DC \leftarrow DC + 1$	—	$\bar{C}$	1
	DEC D	0000	1010	0A	$DC \leftarrow DC - 1$	—	C	1
	AND A, @LR	0000	0000	00	$Acc \leftarrow Acc \wedge RAM \{ LR \}$	—	$\bar{Z}$	1
	OR A, @LR	0000	0001	01	$Acc \leftarrow Acc \vee RAM \{ LR \}$	—	$\bar{Z}$	1
XOR A, @LR	0000	0010	02	$Acc \leftarrow Acc \nabla RAM \{ LR \}$	—	$\bar{Z}$	1	
Bit Manipulation	CLR @LR, b	1000	01bb	84 + b	$RAM \{ LR \} b \leftarrow 0$	—	1	2
	SET @LR, b	1000	00bb	80 + b	$RAM \{ LR \} b \leftarrow 1$	—	1	2
	TEST @LR, b	1000	11bb	8C + b	$SF \leftarrow RAM \{ LR \} b$	—	*	2
Flag Manipulation	CLR CF	1000	1011	8B	$CF \leftarrow 0$	0	1	2
	SET CF	1000	1001	89	$CF \leftarrow 1$	1	1	2
	TESTP CF	0111	0111	77	$SF \leftarrow CF$	—	*	1
Branch	BSS a	11dd	dddd	C0 + d	if SF = 1 then $PC \leftarrow a$ else null, $a = PC_{9..6} \cdot d$	—	1	2
	LD MBR, #k	1011	kkkk	Bk	$MBR \leftarrow k$	—	—	1
Subroutine	CALLS a	1010	nnnn	An	$STACK \leftarrow PC, PC \leftarrow a, a = 2n \ (n = 1 \sim 15)$	—	—	2
	RET	0110	1110	6E	$PC \leftarrow STACK$	—	—	2
CPU Control	HOLD	0000	0111	07	hold	—	1	1
	NOP	0111	1111	7F	no operation	—	—	1
Timer Counter Control	TMRST	1000	1000	88	reset timer counter	—	—	1

- (Note 1) C : Carry from the highest digit for addition and non-borrow to the highest digit for subtraction.  
 Z : Zero detection data are 1 when data transferred to the accumulator or RAM are 0000B.  
 \* : Value specified by operation is set.  
 — : No flag change.

(Note 2) The PC contains the address following the instruction being executed.

Instruction code map

Upper \ Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	AND A, @LR	OR A, @LR	XOR A, @LR	ADD A, @LR	ADDC A, @LR	SUBRC A, @LR	LD A, @LR	HOLD	DEC @LR	INC @LR	DEC D	INC D	MOV A, L	MOV A, D	MOV D, A	MOV L, A
1	LD A, #k															
2	LD L, #k															
3	ST #k, @LR															
4	ADD A, #k															
5	ADD L, #k															
6	IN %p, A						LDH A, @DC	LDL A, @DC	IN %p, @LR						RET	
7	OUT A, %p						ST A, @LR	TESTP CF	OUT @LR, %p						MOV A, P	NOP
8	SET @LR, b				CLR @HL, b				TMRST	SET CF	MOV A, T	CLR CF	TEST @LR, b			
9	LD A, x								ST A, x							
A	CALLS a															
B	LD MBR, #k															
C	BSS a															
D																
E																
F																

(Note 1) Blank code is undefined.

(Note 2)  1-Cycle instruction     2-Cycle instruction



**MAXIMUM RATINGS (Ta = 25°C)**

CHARACTERISTIC		SYMBOL	RATING	UNIT
Power Supply Voltage		V <sub>DD</sub>	- 0.3~5.0	V
Input Voltage		V <sub>IN</sub>	V <sub>SS</sub> - 0.3~V <sub>DD</sub> + 0.3	V
Output Current		I <sub>OUT</sub> (P53)	- 20	mA
Power Dissipation	TC9028AP	P <sub>D</sub>	350	mW
	TC9028AF		300	
Operating Temperature		T <sub>opr</sub>	- 20~75	°C
Storage Temperature		T <sub>stg</sub>	- 40~125	°C

**ELECTRICAL CHARACTERISTICS**

**RECOMMENDED OPERATING CONDITIONS**

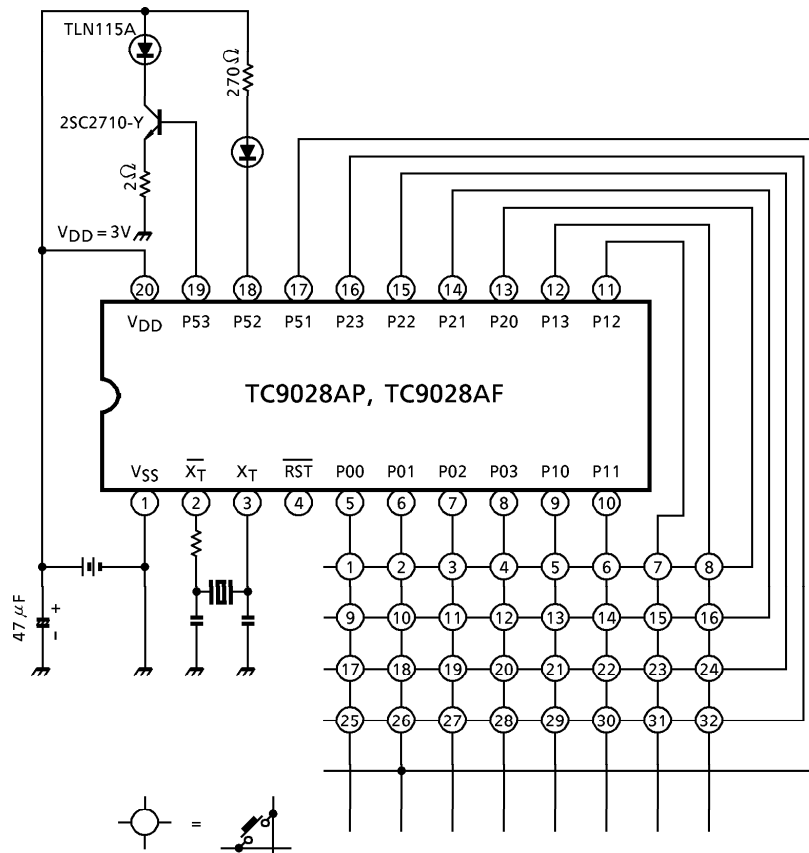
(In \*marked items, Ta = -20~75°C, unless otherwise specified, V<sub>CC</sub> = 3.0V, Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Power Supply Voltage *		V <sub>DD</sub>	—	—	2.0	—	4.0	V
Oscillation Frequency *		f <sub>osc</sub>	—	—	400	—	800	kHz
Input Voltage	"H" Level	V <sub>IH</sub>	—	Except Hysteresis Input	V <sub>DD</sub> × 0.7	—	V <sub>DD</sub>	V
		V <sub>IH</sub>	—	Hysteresis Input ( $\overline{RST}$ )	V <sub>DD</sub> × 0.8	—	V <sub>DD</sub>	
	"L" Level	V <sub>IL</sub>	—	Except Hysteresis Input	0	—	V <sub>DD</sub> × 0.3	V
		V <sub>IL</sub>	—	Hysteresis Input ( $\overline{RST}$ )	0	—	V <sub>DD</sub> × 0.2	

**DC CHARACTERISTICS (V<sub>DD</sub> = 3.0V, Ta = 25°C, unless otherwise specified)**

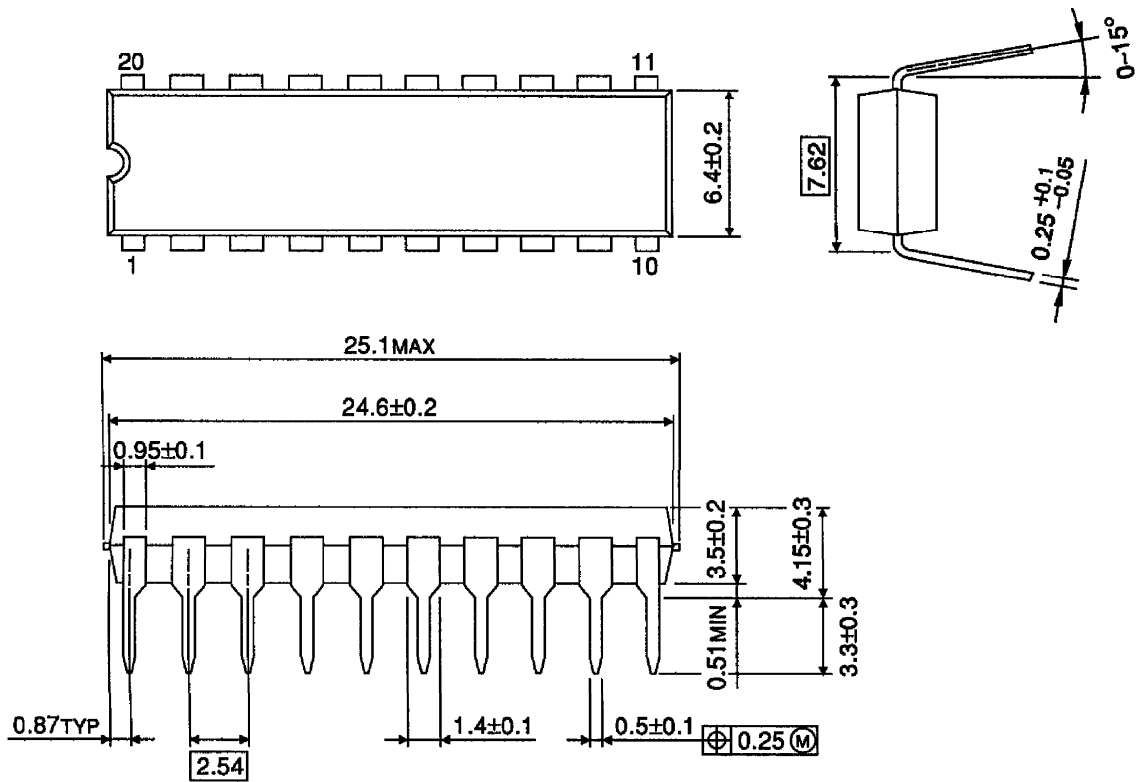
CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operation Power Supply Current		I <sub>DD</sub>	—	f <sub>c</sub> = 455kHz	—	—	1.0	mA
Static Dissipation Current		I <sub>QD</sub>	—	at Hold Function	—	—	1.0	μA
Pulldown Resistance		R <sub>D</sub>	—	(P0, P1, P2)	100	—	400	kΩ
Pullup Resistance		R <sub>U</sub>	—	( $\overline{RST}$ )	25	—	100	kΩ
Output Current	"H" Level	I <sub>OH</sub>	—	V <sub>OH</sub> (P52) = 2.6V	- 0.4	- 1.4	—	mA
	"L" Level	I <sub>OL</sub>	—	V <sub>OH</sub> (P53) = 1.5V	- 10	—	—	
Input Leak Current		I <sub>LI</sub>	—	V <sub>OL</sub> (P52) = 1.5V	5	—	—	μA
			—	V <sub>IN</sub> = V <sub>DD</sub> , V <sub>SS</sub>	- 1.0	—	1.0	μA

**APPLICATION CIRCUIT**



**OUTLINE DRAWING**  
DIP20-P-300-2.54A

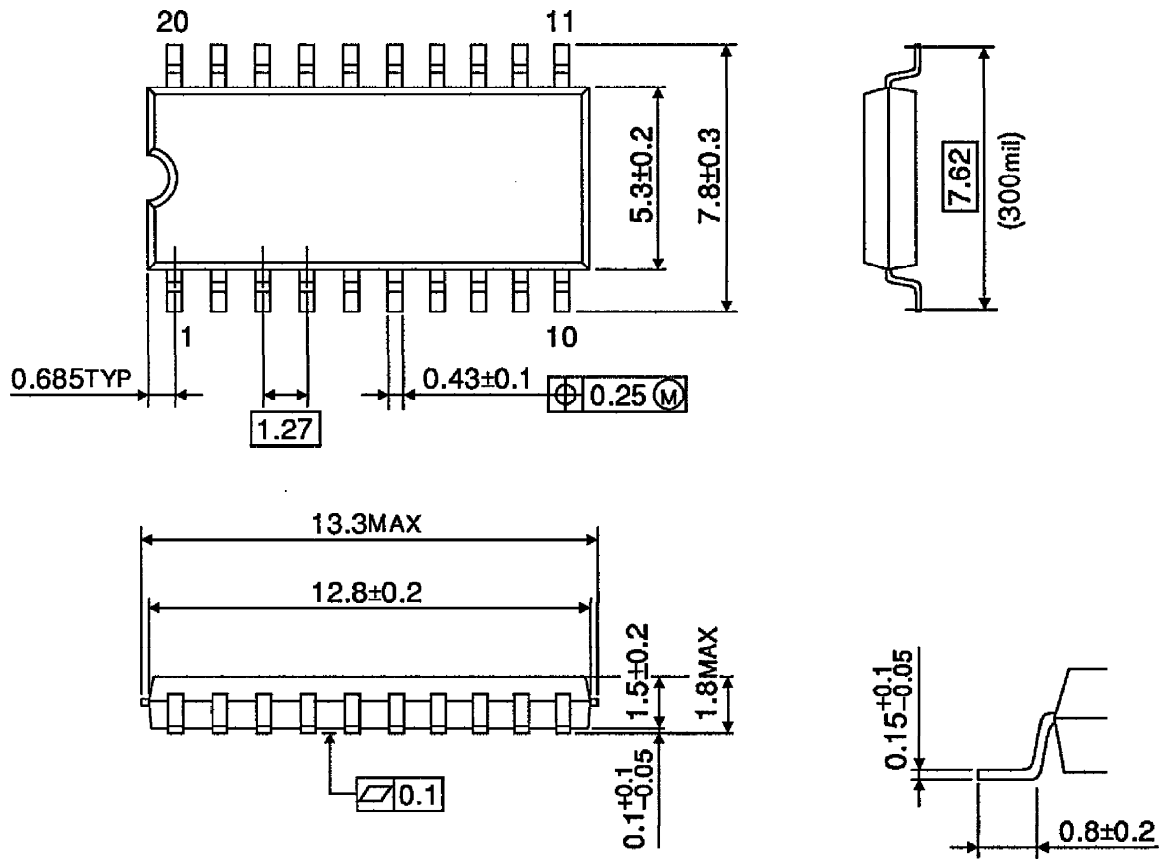
Unit : mm



Weight : 1.4g (Typ.)

**OUTLINE DRAWING**  
SOP20-P-300-1.27

Unit : mm



Weight : 0.48g (Typ.)