CMOS 4-BIT MICROCONTROLLER

TMP47CE820F

The 47CE820 is a high speed and high performance 4-bit single chip microcomputer based on the TLCS-470 CMOS series with E²PROM, LCD driver and high speed timer/counter.

PART No.	ROM	RAM	E² PROM	PACKAGE	PIGGYBACK
*TMP47CE820F	8192 x 8-bit	512 x 4-bit	64 x 8-bit	QFP80	*TMP47CE020G

* Under development

FEATURES

- ◆4-bit single chip microcomputer
- ◆Instruction exection time :
  1.3μs (at 6MHz), 244μs (at 32.8KHz)
- ◆92 basic instructions
- ◆Table look-up instructions
- ◆5-bit to 8-bit data conversion instruction
- ◆Subroutine nesting : 15 levels max.
- ◆6 interrupt sources (External :2, Internal : 4)
  All sources have independent latches each, and multiple interrupt control is available.
- ◆I/O port
  - Input 2 ports 5 pins
  - Output 2 ports 8 pins
  - I/O 6 ports 23 pins
- ◆Interval Timer
- ◆Two 12-bit Timer/Counters
  Timer, event counter, and pulse width measurement mode
- ◆Two 8-bit High-speed Timer/Counter
  Timer, event counter, frequency measurement, and pulse output mode
- ◆Watchdog Timer
- ◆Serial Interface with 8-bit buffer
  - Simultaneous transmission and reception capability
  - External/internal colck, leading/trailing edge shift, 4/8-bit mode
- ◆512-bit E²PROM
  - 1 byte rewrite and chip erase
  - Self timed rewrite cycle (With Timer)
  - Ready / Busy status monitor and Interrupt function
  - Data retention time : 10 Years (Min.)
  - Rewrite cycle : 1×10^4 (Min.)
- ◆High current outputs
  LED direct drive capability (typ.20mA x 8bits)
- ◆LCD driver
  - LCD direct drive is available (Max. 12-digit display at 1/4 duty LCD)
  - 1/4, 1/3 1/2 duties or static drive are programmably selectable.
- ◆Dual-clock operation
  High-speed/Low-power consumption operating mode
- ◆Hold function : Battery/Capacitor back-up
- ◆Emulator : BM47C820A

QFP80

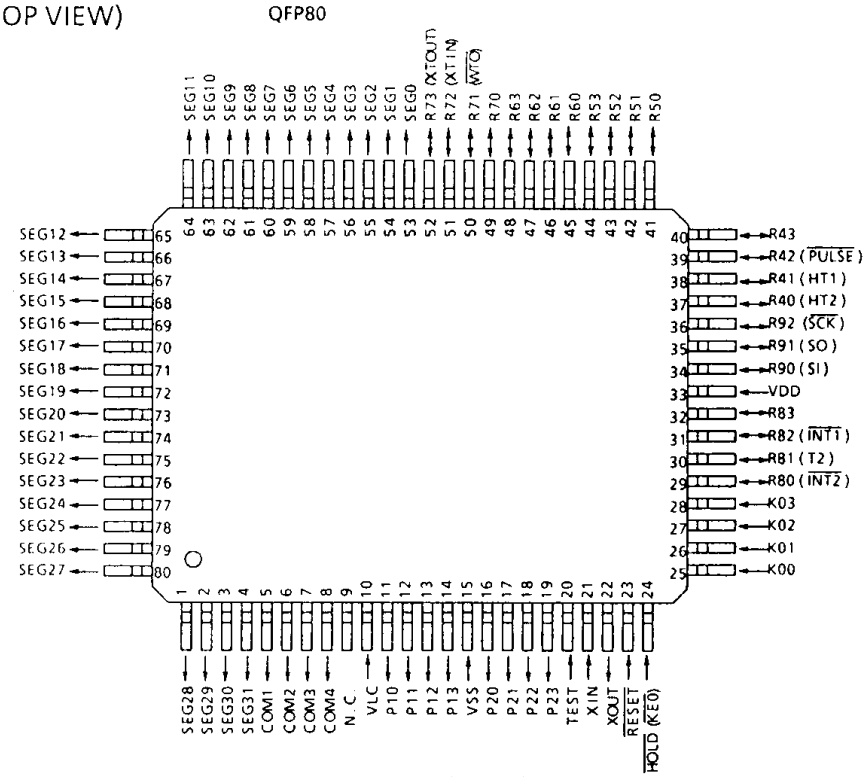
TMP47CE820F

QFC80

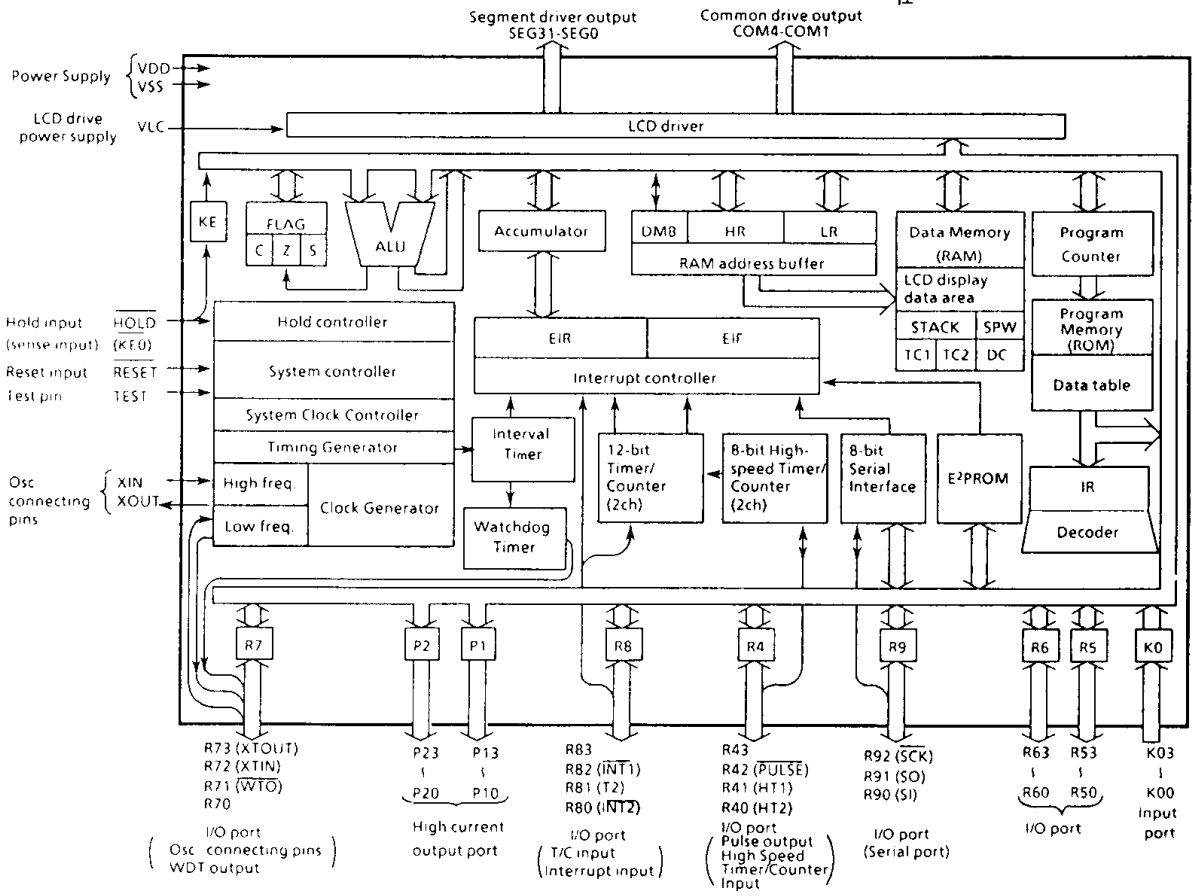
TMP47CE020G

PIN ASSIGNMENT (TOP VIEW)

QFP80



BLOCK DIAGRAM



OPERATIONAL DESCRIPTION

The 47CE820 contains an E²PROM in the 47C820.
The configuration and function of the 47CE820 are similar to the 47C820 except the E²PROM. The technical data sheets for the 47C820 should also be reffered to.

1. E²PROM

The 47CE820 contains 64 x 8-bit E²PROM (Electrically Erasable Programmable ROM).

1.1 Circuit configuration

The E²PROM circuit consists of the function blocks shown in Figure 1-1.

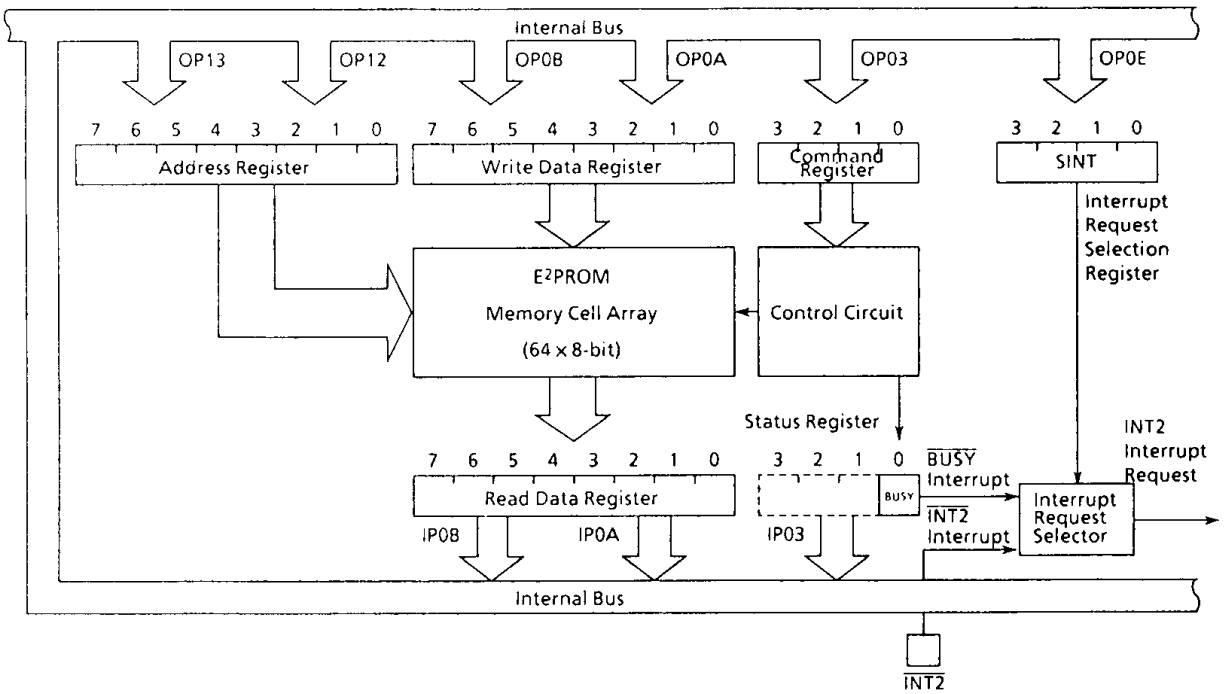


Figure 1-1. E²PROM

1.2 Control of E²PROM

E²PROM is controlled by 6 registers: the command register, address register, write data register, read data register, status register and interrupt request selection register.

(1) E²PROM command register

The E²PROM command register (OP03) selects the E²PROM operation mode. Operation starts at the point where the operation mode is set. When operation ends, the command register is automatically cleared to "0000_B".

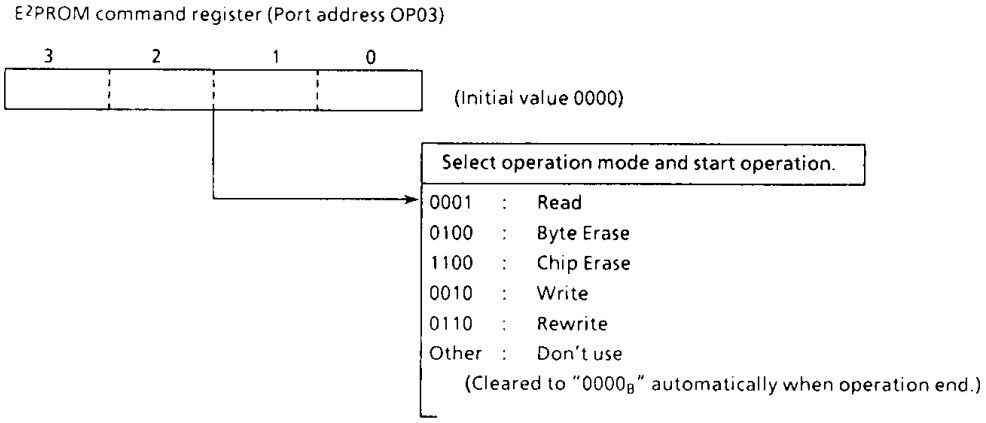


Figure 1-2. E²PROM command register

(2) E²PROM address register

The E²PROM address register is a 8-bit register which specifies the E²PROM address. The lower 4 bits are accessed as port address OP12 and the upper 4 bits are accessed as port address OP13.

The E²PROM address of the 47CE820 is 00_H to $3F_H$. Don't select 40_H to FF_H of the E²PROM address.

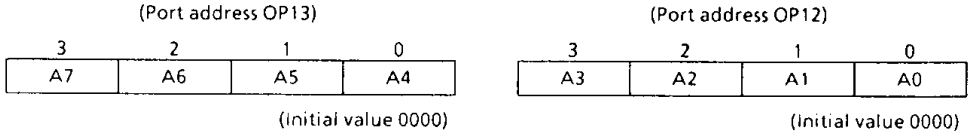


Figure 1-3. E²PROM address register

(3) E²PROM write data register

The E²PROM write data register is an 8-bit register used to store data to be written to the E²PROM. The lower 4 bits are accessed as port address OP0A and the upper 4 bits are accessed as port address OP0B.

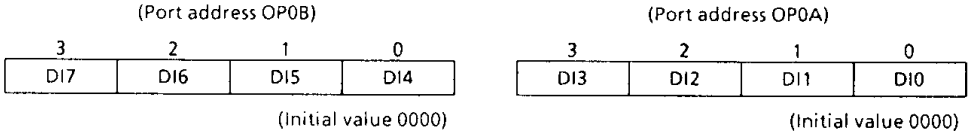


Figure 1-4. E²PROM write data register

(4) E²PROM read data register

The E²PROM read data register is an 8-bit register used to store data read from the E²PROM. The lower 4 bits are accessed as port address IP0A and the upper 4 bits are accessed as port address IP0B.

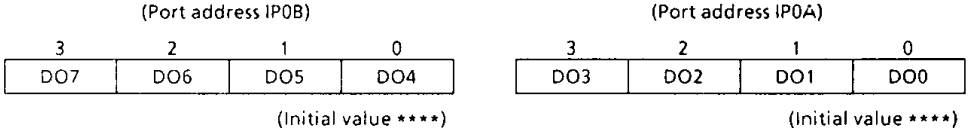


Figure 1-5. E²PROM read data register

(5) E²PROM status register

The operating status of an E²PROM can be monitored using the status register (IP03).

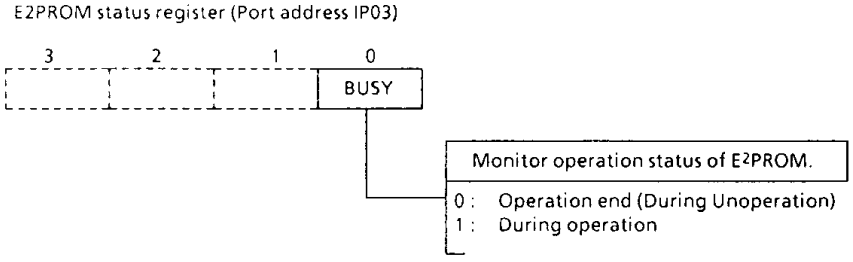


Figure 1-6. E²PROM status register

(6) Interrupt request selection register

The interrupt request selection register (OP0E) is a register used to select external interrupt (INT2) requests.

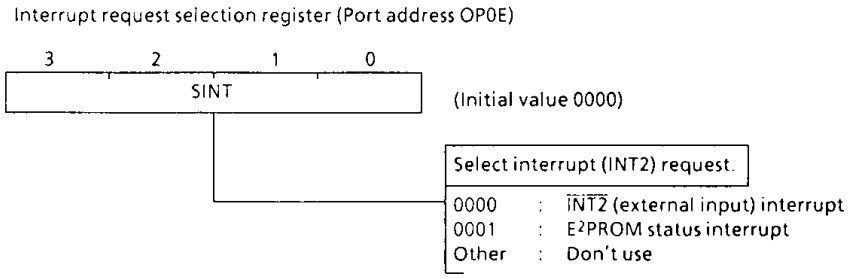


Figure 1-7. Interrupt request selection register

When SINT is "0", an interrupt is generated by an interrupt request from the $\overline{INT2}$ pin.
When SINT is "1", an interrupt is generated when E²PROM operation ends. (E²PROM status interrupt function)
SINT is switched when interrupt enable master F/F (EIF) or interrupt enable register (EIR) is "0" (inhibit).

1.3 Operation mode of E²PROM

E²PROM read operation is performed in real time, but it is necessary to wait during time set the built-in timer for erase or write operations. When the E²PROM is operating, the contents of the E²PROM command register, address register, write data register and interrupt request selection register cannot be changed. Thus, when changing the contents of these registers, it is necessary to either check that operation has ended using the E²PROM status register or the E²PROM status interrupt function.
The Erase, Write and Rewrite operations of the E²PROM can be executed during the normal mode.

(1) Read

When the E²PROM command register is set to the read mode, the data at the E²PROM specified by the address register are stored into the read data register.
The addresses must be loaded to the address register before read operation.

Example The contents at E²PROM address $2C_H$ are read, and are stored to location 30_H, 31_H in RAM.

```
LD    A, #0CH          ; Set address of E²PROM
OUT   A, %OP12
LD    A, #2H
OUT   A, %OP13
OUT   #0001B, %OP03H   ; Read operation
LD    HL, #30H         ; Store read data to RAM
IN    %IP0A, @HL
INC   L
IN    %IP0B, @HL
```

(2) Erase

Erasing clears the data in memory cells to "00_H".

① Byte Erase

When the E²PROM command register is set to the byte erase mode, the data at the E²PROM specified by the address register are erased.
The address must be loaded to the address register before byte erase operation.

Example The contents at location 1EH in E2PROM are erased.

```
LD    A, #0EH          ; Set address of E²PROM
OUT   A, %OP12
LD    A, #1H
OUT   A, %OP13
OUT   #0100B, %OP03    ; Start byte erase operation.
```

② Chip Erase

When the E²PROM command register is set to the chip erase mode, all data at all Addresses of the E²PROM are erased as one batch.

Example All data at all Addresses of E²PROM are erased as one batch.

```
OUT   #1100B, %OP03    ; Start chip erase operation.
```

(3) Write

When the E²PROM command register is set to the write mode, the contents of the write data register are written to the E²PROM specified by the address register. (The data at the E²PROM specified the address register must be erased biforehand.)

Before writing, it is necessary to load the address to the address register and the write data to the write data register.

Example "$5A_H$" is written at E²PROM address 32_H.

```
        LD    A, #2H            ; Set address of E²PROM
        OUT   A, %OP12
        LD    A, #3H
        OUT   A, %OP13
        OUT   #0AH, %OP0A       ; Set write data of E²PROM
        OUT   #5H, %OP0B
        OUT   #0100B, %OP03     ; Start byte erase operation
LOOP :  TESTP %IP03, 0          ; Monitor operation status of E²PROM
        B     LOOP                Start write operation
        OUT   #0010B, %OP03
```

(4) Rewrite

When the E²PROM command register is set to the rewrite mode, the data at the E²PROM specified by the address register are erased and the contents of the write data register is written.

Before rewriting, it is necessary to load the address to the address register and the write data to the write data register.

Example Rewriting the data at E²PROM address 32_H to "$5A_H$."

```
        LD    A, #2H            ; Set address of E²PROM
        OUT   A, %OP12
        LD    A, #3H
        OUT   A, %OP13
        OUT   #0AH, %OP0A       ; Set write data of E²PROM
        OUT   #5H, %OP0B
        OUT   #0110B, %OP03     ; Start rewrite operation
```

Port Address (**)	Port		Input/Output instruction						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A, %p OUT @HL, %p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p, b TESTP %p, b	SET @L CLR @L TEST @L
00_H	K0 input port	——	○	–	–	–	–	○	–
01	P1 output latch	P1 output port	○	○	○	○ (Note2)	○	○	–
02	P2 output latch	P2 output port	○	○	○	○	○	○	–
03	E²PROM status	E²PROM command	○	○	○	–	–	○	–
04	R4 input port	P4 output port	○	○	○	–	○	○	○
05	R5 input port	R5 output port	○	○	○	–	○	○	○
06	R6 input port	R6 output port	○	○	○	–	○	○	○
07	R7 input port	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	R9 input port	R9 output port	○	○	○	–	○	○	–
0A	E²PROM read data register	E²PROM write data register	○	○	○	–	–	○	–
0B	E²PROM read data register	E²PROM write data register	○	○	○	–	–	○	–
0C	HTC1 counter	HTC1 register	○	○	○	–	–	–	–
0D	HTC2 counter	HTC2 register	○	○	○	–	–	–	–
0E	SIO,colck generator and hold status	E²PROM interrupt request selection.	○	○	○	–	–	○	–
0F	Serial receive buffer	Serial transmit buffer	○	○	○	–	–	–	–
10_H	Undefined	Hold operating mode control	–	○	–	–	–	–	–
11	Undefined	——	–	–	–	–	–	–	–
12	Undefined	E²PROM address register	–	○	–	–	–	–	–
13	Undefined	E²PROM address register	–	○	–	–	–	–	–
14	Undefined	——	–	–	–	–	–	–	–
15	Undefined	Watchdog Timer control	–	○	–	–	–	–	–
16	Undefined	System clock control	–	○	–	–	–	–	–
17	Undefined	HTC1 control	–	○	–	–	–	–	–
18	Undefined	HTC2 control	–	○	–	–	–	–	–
19	Undefined	Interval timer interrpt control	–	○	–	–	–	–	–
1A	Undefined	LCD driver control 1	–	○	–	–	–	–	–
1B	Undefined	LCD driver control 2	–	○	–	–	–	–	–
1C	Undefined	Timer/Counter 1 control	–	○	–	–	–	–	–
1D	Undefined	Timer/Counter 1 control	–	○	–	–	–	–	–
1E	Undefined	Serial Interface control1	–	○	–	–	–	–	–
1F	Undefined	Serial Interface control2	–	○	–	–	–	–	–

Note 1 : "——" means the reserved state. Unavilable for the user programs.

Note 2 : The 5-bit to 8-bit data conversion instruction [OUTB @HL], automatic access to ports P1 and P2.

Table 1-1 Port Address Assignments and Available I/O Instructions

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATINGS	UNIT
Supply Voltage	V_{DD}		− 0.3 to 7	V
Supply Voltage (LCD drive)	V_{LC}		− 0.3 to V_{DD} + 0.3	V
Input Voltage	V_{IN}		− 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin	− 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Sink open drain pin	− 0.3 to 10	
Output Current (Per 1 pin)	I_{OUT1}	Ports P1, P2	15	mA
	I_{OUT2}	Ports R4 to R9	3.2	
Output Current (Total)	ΣI_{OUT1}	Ports P1, P2	60	mA
Power Dissipation [T_{opr} = 70°C]	PD		600	mW
Soldering Temperature (time)	T_{sld}		260 (10sec)	°C
Storage Temperature	T_{stg}		− 55 to 125	°C
Operating Temperature	T_{opr}		− 40 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = − 40 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		In the Normal mode	4.5	6.0	V
			In the SLOW mode	2.7		
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT		0.4	6.0	MHz
	fs	XTIN, XTOUT		30.0	34.0	KHz

Note. Input Voltage V_{IH3}, V_{IL3} : in the SLOW and HOLD mode.

D.C. CHARACTERISTICS (V_{SS} = 0V, T_{opr} = −40 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		−	0.7	−	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	−	−	±2	μA
	I_{IN2}	Open drain R port					
Input Low Current	I_{IL}	Push-pull R port	V_{DD} = 5.5V, V_{IN} = 0.4V	−	−	−2	mA
Input Registance	R_{IN1}	Port K0 with pull-up/pull-down		30	70	150	KΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leakage Current	I_{LO}	Open drain ports P, R	V_{DD} = 5.5V, V_{OUT} = 5.5V	−	−	2	μA
Output High Voltage	V_{OH}	Push-pull R port	V_{DD} = 4.5V, I_{OH} = −200μA	2.4	−	−	V
Output Low Voltage	V_{OL2}	Except XOUT XTOUT and ports P1, P2	V_{DD} = 4.5V, I_{OL} = 1.6mA	−	−	0.4	
Output Low Current	I_{OL1}	Ports P1, P2	V_{DD} = 4.5V, V_{OL} = 1.0V	−	10	−	mA
Segment Output Registance	R_{OS}	SEG pin	V_{DD} = 5V, V_{DD} − V_{LC} = 3V	−	20	−	KΩ
Common Output Registance	R_{OC}	COM pin					
Segment/Common Output Registance	$V_{O2/3}$	SEG / COM pin		3.8	4.0	4.2	V
	$V_{O1/2}$			3.3	3.5	3.7	
	$V_{O1/3}$			2.8	3.0	3.2	
Supply Current (in the Normal mode)	I_{DD}		Except E²PROM operating V_{DD} = 5.5V, fc = 4MHz	−	3	6	mA
	I_{DDE}		E²PROM operating V_{DD} = 5.5V, fc = 4MHz	−	7	15	
Supply Current (in the SLOW mode)	I_{DDS}		V_{DD} = 3.0V, fs = 32.768KHz	−	30	60	μA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5V	−	0.5	10	

Note 1. *Typ. values show those at T_{opr} = 25°C, V_{DD} = 5V.*

Note 2. *Input Current I_{IN1} ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.*

Note 3. *Output Resistance R_{OS}, R_{OC} ; Shows on-resistance at the level switching.*

Note 4. *$V_{O2/3}$; Shows 2/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.*
$V_{O1/2}$; Shows 1/2 level output voltage, when the 1/2 duty or static LCD is used.
$V_{O1/3}$; Shows 1/3 level output voltage, when the 1/4 or 1/3 duty LCD is used.

Note 5. *Supply Current I_{DD} ; V_{IN} = 5.3V/0.2V*
The K0 port is open when the input resistor is contained.
The voltage applied to the R port is within the valid range.

Note 6. *Supply Current I_{DDS} ; V_{IN} = 2.8V/0.2V. Only low frequency clock is only osillated (connecting XTIN, XTOUT).*

Note 7. *Supply Current I_{DDE} ; Supply Current for a read operation only is specified with I_{DD}.*

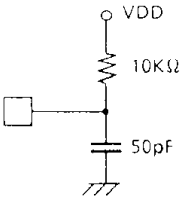
A.C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 40 to 70°C)

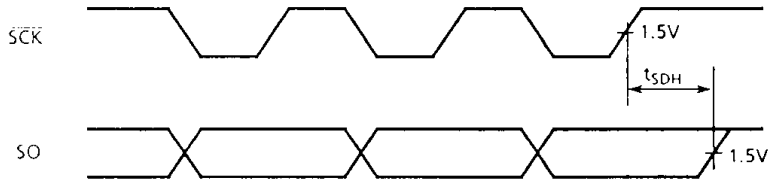
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}	in the Normal mode	1.9	–	20	μs
		in the SLOW mode	235	–	267	μs
High Level Clock Pulse Width	t_{WCH}	For external clock operation	80	–	–	ns
Low Level Clock Pulse Width	t_{WCL}					
Shift data Hold Time	t_{SDH}		$0.5t_{cy}$ – 300	–	–	ns
High Speed Timer/Counter input frequency	f_{HT}		–	–	fc	MHz
E²PROM Rewrite Cycle	N_{EW}		10^4	–	–	cycles
E²PROM Data Retention Time	t_{RET}		10	–	–	years

Note. Shift data Hold time :

External circuit for $\overline{SCK}$ pin and SO pin



Serial port (completion of transmission)



RECOMMENDED OSCILLATING CONDITIONS

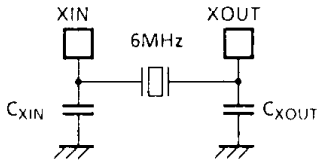
(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = – 40 to 70°C)

(1) 6MHz

Ceramic Resonator

CSA6.00MGU (MURATA) $C_{XIN} = C_{XOUT}$ = 30pF

KBR-6.00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30pF



(2) 4MHz

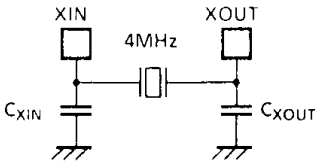
Ceramic Resonator

CSA4.00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 30pF

KBR-4.00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30pF

Crystal Oscillator

204B-6F 4.0000 (TOYOCOM) $C_{XIN} = C_{XOUT}$ = 20pF

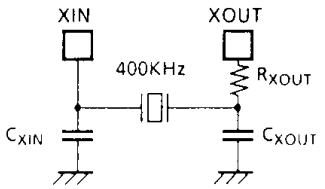


(3) 400KHz

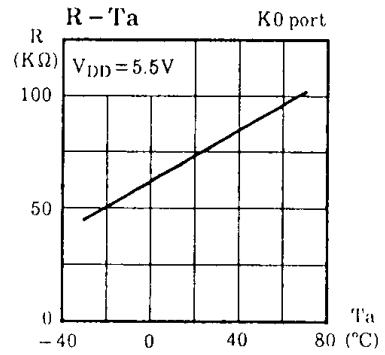
Ceramic Resonator

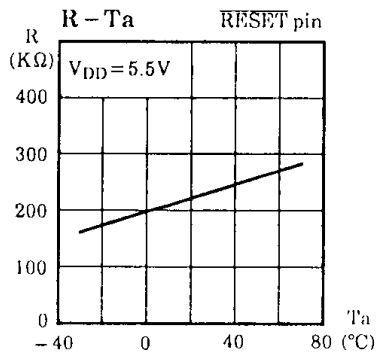
CSB400B (MURATA) $C_{XIN} = C_{XOUT}$ = 220pF, R_{XOUT} = 6.8KΩ

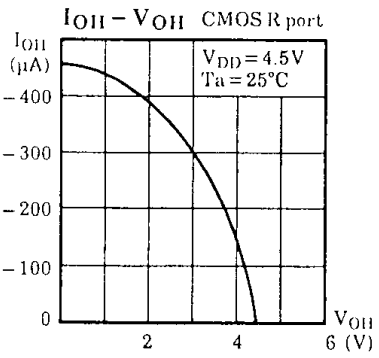
KBR-400B (KYOCERA) $C_{XIN} = C_{XOUT}$ = 100pF, R_{XOUT} = 10KΩ

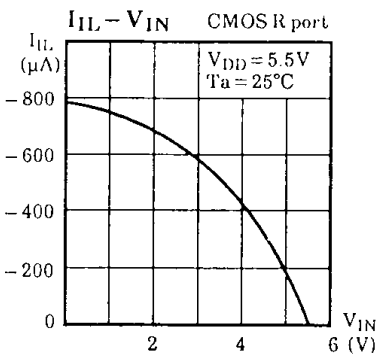


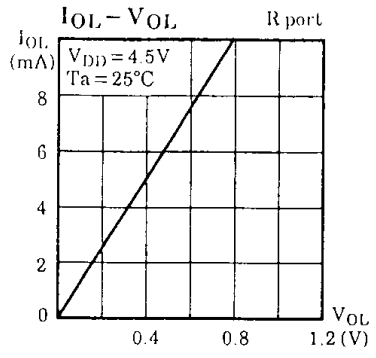
TYPICAL CHARACTERISTICS

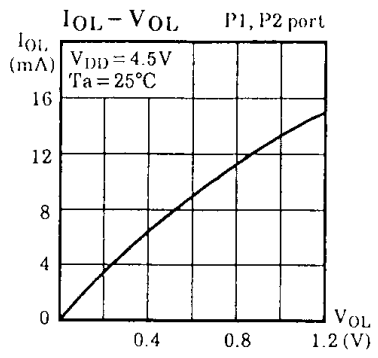


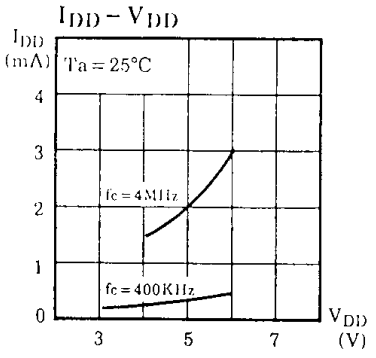


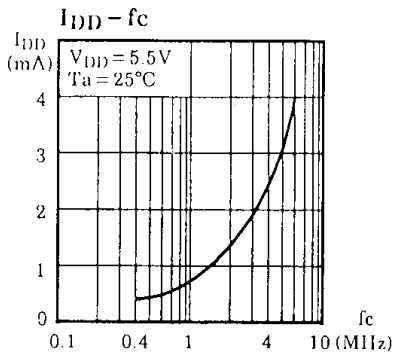












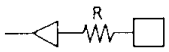
INPUT/OUTPUT CIRCUITRY

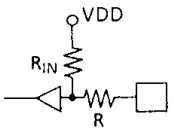
(1) Control pins

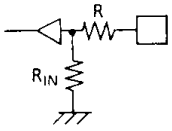
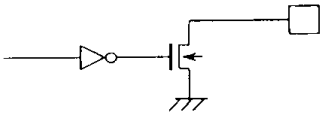
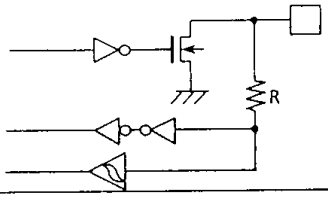
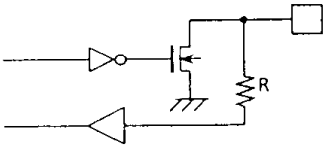
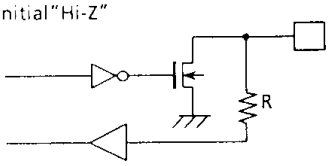
The input/output circuitries of the 47CE820 control pins are similar to those of the 47C660/860.

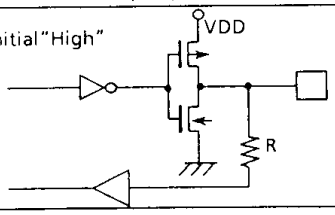
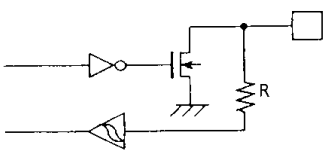
(2) I/O Ports

The input/output circuitries of the 47CE820 I/O ports are shown as belows, any one of the circuitries can be chosen by a code (GA to GF) as a mask option.

<table>
<tr><th>PORT</th><th>I/O</th><th>IINPUT/OUTPUT CIRCUITRY and CODE</th><th>REMARKS</th></tr>
<tr><td>K0</td><td>Input</td><td>GA, GD
 

GB, GE
 

GC, GF
 
</td><td>Pull-up/pull-down resistor
R_{IN} = 70KΩ (typ.)
R = 1KΩ (typ.)</td></tr>
<tr><td>P1
P2</td><td>Output</td><td>  </td><td>Sink open drain output
Initial "Hi-Z"
High current
I_{OL} = 10mA (typ.)</td></tr>
<tr><td>R40
R41</td><td>I/O</td><td> 
</td><td>Sink open darin output
Initial "Hi-Z"
(Hysteresis) = Input (HTC)
R = 1KΩ (typ.)</td></tr>
<tr><td>R42
R43
R7</td><td>I/O</td><td> 
</td><td>Sink open drain output
Initial "Hi-Z"
R = 1KΩ (typ.)</td></tr>
<tr><td>R6
R5</td><td>I/O</td><td>GA, GB, GC
Initial"Hi-Z"
 

GD, GE, GF
Initial"High"
 
</td><td>Sink open drain output
or
Push-pull output
R = 1KΩ (typ.)</td></tr>
<tr><td>R8
R9</td><td>I/O</td><td> 
</td><td>Sink open drain output
Initial "Hi-Z"
Hysteresis input
R = 1KΩ (typ.)</td></tr>
</table>