TOSHIBA MOS TYPE DEGITAL
INTEGRATED CIRCUIT
Silicon Monolithic N-Channel Silicon Gate MOS

TMP8259AP

PROGRAMMABLE INTERRUPT CONTROLLER

1. GENERAL DESCRIPTION

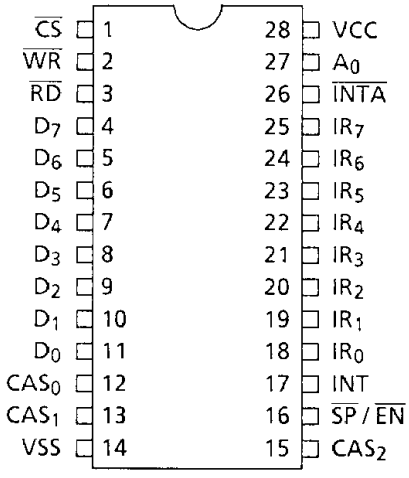
TMP8259AP is a programmable interrupt controller. It handles up to eight vectored priority interrupts for the MPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry.

FEATURES

- Eight Level Priority Controller.
- Expandable to 64 Level.
- Interrupt Modes, Interrupt Mask, Vectored Address Programmable.
- Single +5V Power Supply.
- Supports 8085A, 8086 Microcomputer Interrupt Sequence.

2. PIN CONNECTIONS (TOP VIEW)

TMP8259AP



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3. PIN NAMES AND PIN DESCRIPTION

Pin Name	Input / Output	Function
$\overline{CS}$	Input	Chip Select Input. A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication beween the MPU and the TMP8259AP. $\overline{INTA}$ functions are independent of $\overline{CS}$.
$\overline{WR}$	Input	Write Control Input. A low on this pin when $\overline{CS}$ is low enables the TMP8259AP to accept command words from MPU.
$\overline{RD}$	Input	Read Control Input. A low on this pin when $\overline{CS}$ is low enables the TMP8259AP to release status onto the data bus for the MPU.
D_0 to D_7	Input / Output	Bidirectional Data Bus. Command status and interrupt-vector information is transferred via this bus.
CAS_0 to CAS_2	Input / Output	Casecade Lines. The CAS lines from a private TMP8259AP bus to control a multiple TMP8259AP structure. These pins are outputs for a master TMP8259AP and inputs for a slave TMP8259AP.
$\overline{SP}$ / $\overline{EN}$	Input / Output	Slave Program / Enable buffer. This is a dual function pin. When in the buffered mode is can be used as on Output to control buffer transceivers ($\overline{EN}$). When not in the buffered mode it is used as an input to designate a master TMP8259AP ($\overline{SP} = 1$) or a slave ($\overline{SP} = 0$).
INT	Output	Interrupt Request Output. This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the MPU. It is connected to MPU's interrupt pin.
IR_0 to IR_7	Input	Interrupt Request Inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on a IR input (Level Triggered Mode.)
$\overline{INTA}$	Input	Interrupt Ackowledge INPUT. This pin is used to enable TMP8259AP interrupt-vector data onto the data bus by a sequence of interrupt ackowledged pulses issued by the MPU.
A_0	Input	A_0 address line. This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ pins. It is used by the TMP8259AP to decipher various command words the MPU writes and status the MPU wishes to read. It is typically connected to the MPU A_0 address line.
VCC		+ 5V Power Supply
VSS		Ground

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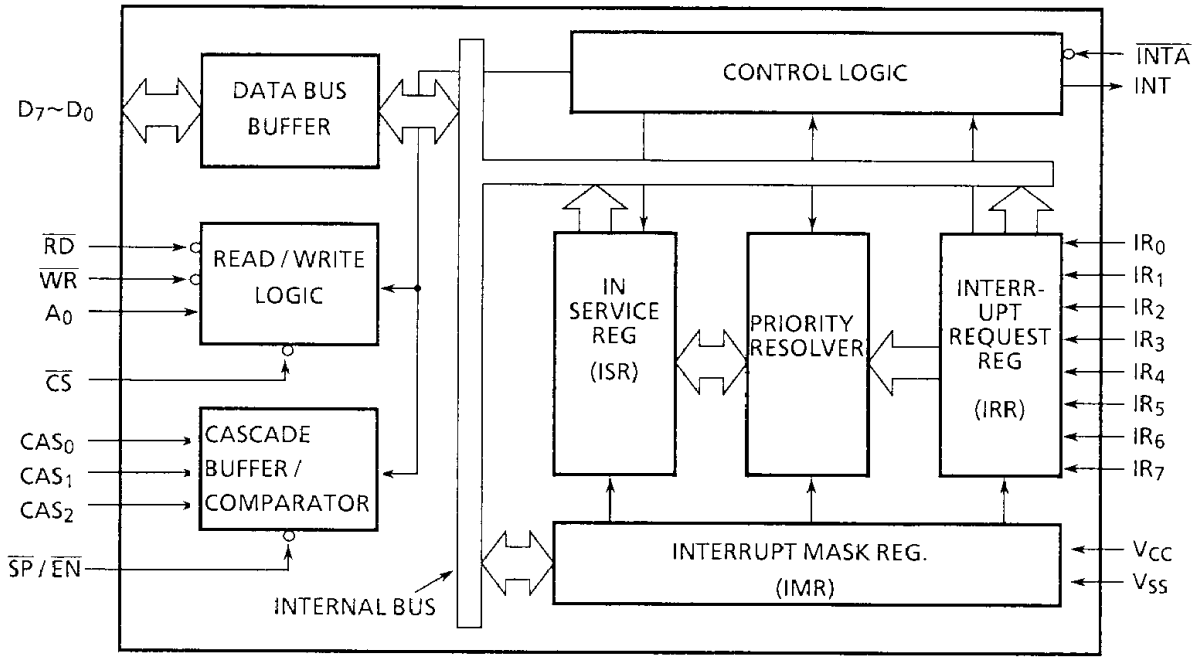
4. BLOCK DIAGRAM



5.1 ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING
VCC	VCC Supply Voltage (with respect to VSS (GND))	-0.5 to + 7V
VIN	Input Voltage	-0.5 to + 7V
PD	Power Dissipation	1W
Tsol	Soldering Temperature (Soldering Time 10 sec)	260℃
Tstg	Storage Temperature	-65℃ to + 150℃
Topr	Operating Temperature	0℃ to 70℃

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5.2 DC CHARACTERISTICS

Ta = 0 to + 70°C, VCC = 5V ± 10%, Vss (GND) = 0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
VIL	Input Low Voltage		-0.5	—	0.8	V
VIH	Input High Voltage		2.2	—	VCC + 0.5	V
VOL	Output Low Voltage	IOL = 2.2mA	—	—	0.45	V
VOH	Output High Voltage	IOH = -400μA	2.4	—	—	V
VOH (INT)	Output High Voltage (INT)	IOH = -100μA	3.5	—	—	V
		IOH = -400μA	2.4	—	—	V
IIL	Input Leak Current	0V ≦ VIN ≦ VCC	—	—	± 10	μA
IIOFL	Output Leak Current	0.45V ≦ VIN ≦ VCC	—	—	± 10	μA
ILIR	Input Current (IR)	VIN = 0V	—	—	-300	μA
		VIN = VCC	—	—	10	μA
ICC	Operating Supply Current		—	—	85	mA

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5.3 INPUT CAPACITANCE

Ta = 25°C, VCC = VSS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
CIN	INPUT CAPACITANCE	fC = 1 MHz Unmeasured pins, 0V	—	—	10	pF
CI / O	INPUT / OUTPUT CAPACITANCE		—	—	20	pF

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5.4 AC CHATACTERISTICS

Ta = 0°C to + 70°C, VCC = 5V ± 10%, VSS = 0V

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
TAHRL	A_0 / $\overline{CS}$ Setup Time ($\overline{RD}$)		0	—	—	ns
TRHAX	A_0 / $\overline{CS}$ Hold Time ($\overline{RD}$)		0	—	—	ns
TRLRH	$\overline{RD}$ Pulse Width		235	—	—	ns
TAHWL	A_0 / $\overline{CS}$ Setup Time ($\overline{WR}$)		0	—	—	ns
TWHAX	A_0 / $\overline{CS}$ Hold Time ($\overline{WR}$)		0	—	—	ns
TWLWH	$\overline{WR}$ Pulse Width		290	—	—	ns
TDVWH	D_0 toD_7 Setup Time ($\overline{WR}$)		240	—	—	ns
TWHDX	D_0 toD_7 Hold Time ($\overline{WR}$)		0	—	—	ns
TJLJH	Input IR Low Level Pulse width (Edge Trigger Mode)		100	—	—	ns
TCVIAL	Casecade Setup Time (Second or Third $\overline{INTA}$)		55	—	—	ns
TRHRL	$\overline{RD}$ to Next Command		160	—	—	ns
TWHWL	$\overline{WR}$ to Next Command		190	—	—	ns
*TCHCL	End of Command to next Command (Not Same)		500	—	—	ns
	End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence					
TRLDV	Valid Data Delay ($\overline{RD}$ / $\overline{INTA}$)	D_7 to D_0 CL = 100pF	—	—	200	ns
TRHDZ	Data Floating ($\overline{RD}$ / $\overline{INTA}$)		10	—	100	ns
TJHIH	Interrupt Output Delay (IR)	INT CL = 100pF	—	—	350	ns
TIALCV	Valid Cascade Delay ($\overline{INTA}$)		—	—	565	ns
TRLEL	Enable Active ($\overline{RD}$ / $\overline{INTA}$)	CAS_0 to $_2$ CL = 100pF	—	—	125	ns
TRHEH	Enable Inactive ($\overline{RD}$ / $\overline{INTA}$)		—	—	150	ns
TAHDV	Valid Data Delay (A_0 / $\overline{CS}$)		—	—	200	ns
TCVDV	Valid Data Delay (CAS_0 to CAS_2)		—	—	300	ns

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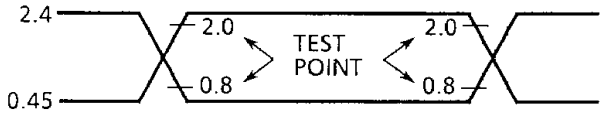
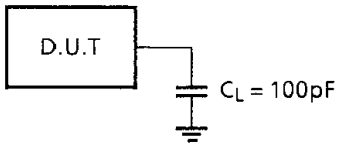
* Worst case timing for TCHCL in an actual microprocessor system is typically much greater than 500 ns (i.e. 8085A = 1.6μs, 8085A – 2 = 1μs, 8086 = 1μs, 8086 – 2 = 625μs)

AC CHARACTERISTICS TEST CONDITION

AC Testing I / O Waveform



AC Testing Load Circuit



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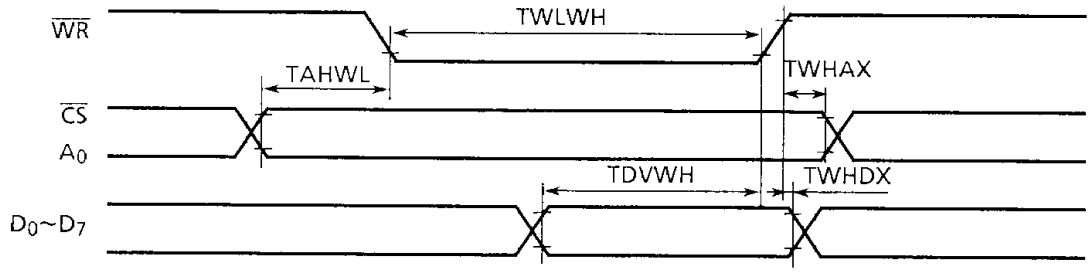
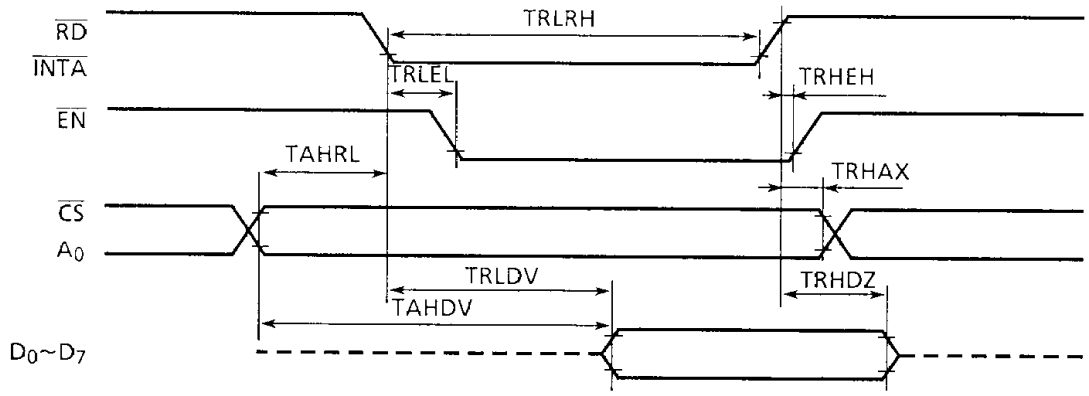
6. TIMING WAVEFORMS

WRITE OPERATION



READ AND INTA OPERATION



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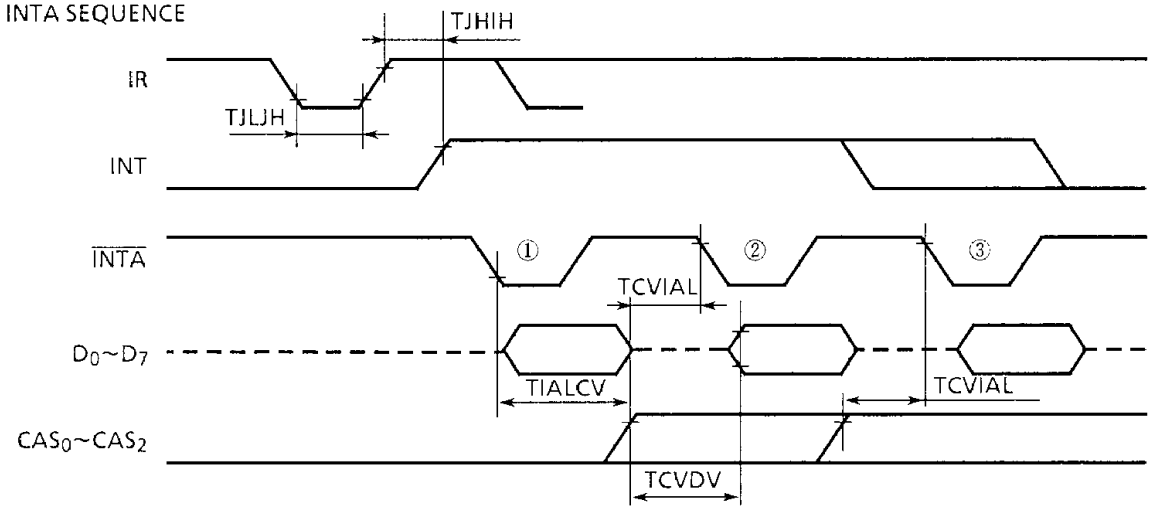
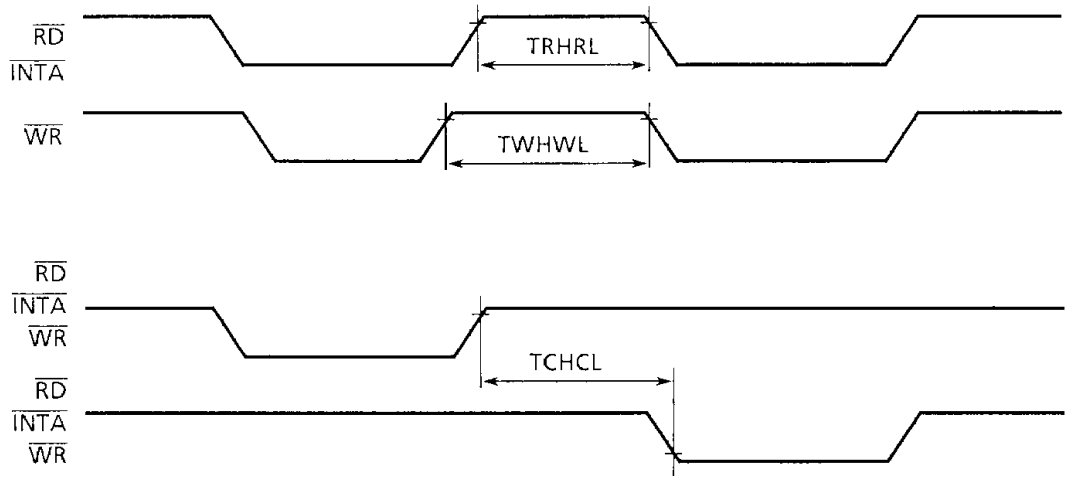
INTA SEQUENCE



OTHER TIMING



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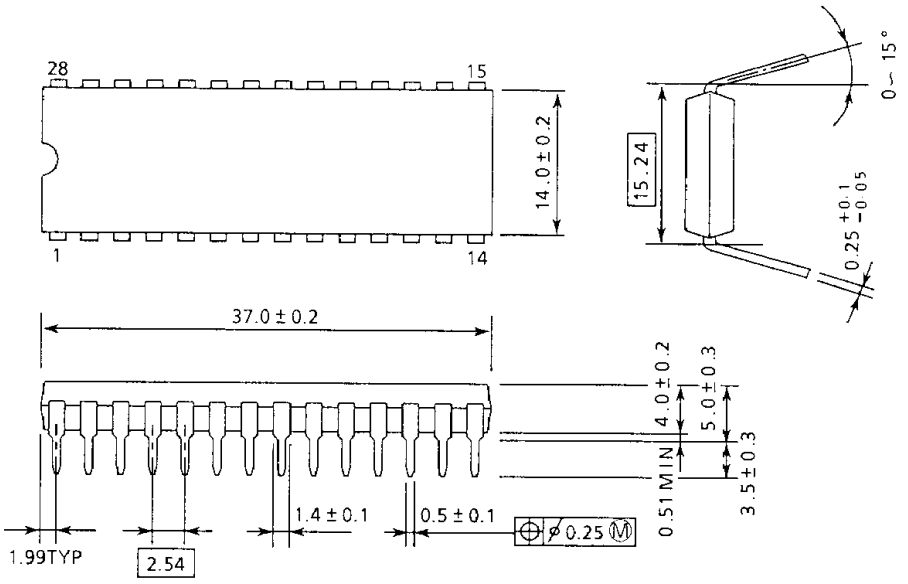
7. EXTERNAL DIMENSION VIEW

28 pins PRASTIC DIP

DIP28-P-600

Unit : mm



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Note : Each lead pitch is 2.54mm, and all the leads are located within ±0.25mm from their theoretical position with respect to No.1 and No.28 leads.