Turbo IC, Inc.

25C128/25C256

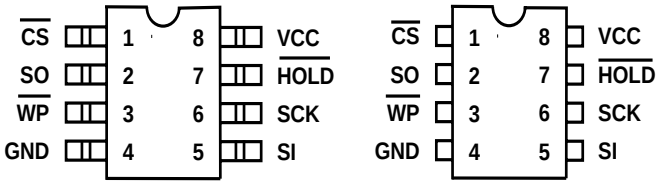
PRELIMINARY INFORMATION

CMOS SPI BUS
128K/256K ELECTRICALLY ERASABLE PROGRAMMABLE ROM
16K/32K X 8 BIT EEPROM

FEATURES :

- Extended Power Supply Voltage
  Single Vcc for Read and Programming
  (Vcc = 2.7V to 3.6 V) (Vcc = 4.5V to 5.5V)
- Low Power (Isb = 2µa @ 5.5 V)
- SPI (Serial Peripheral Interface) Bus
- Support Byte Write and Page Write (64 Bytes)
- Automatic 64 Byte Page write Operation (max. 10 ms)
  Internal Control Timer
  Internal Data Latches for 64 Bytes
- Hardware Data Protection by Write Protect Pin
- High Reliability CMOS Technology with EEPROM Cell
  Endurance : 100,000 Cycles
  Data Retention : 100 Years
- Support SPI Modes 0 (0,0) and 3 (1,1)
- 2.1 Mhz clock rate
- 8 pin JDEC 300 mil wide PDIP and 8 pin 150 mil wide SOIC

PIN DESCRIPTION



8 pin SOIC 8 pin PDIP

DESCRIPTION:

The Turbo IC 25C128/25C256 is a serial 128K/256K EEPROM fabricated with Turbo's proprietary, high reliability, high performance CMOS technology. It's 128K/256K of memory is organized as 16384/32768 x 8 bits. This device offers a flexible byte write and a faster 64-byte page write. It also offers significant advantages in low power and low VCC voltage applications.

The Turbo IC 25C128/25C256 is assembled in either a 8-pin PDIP or 8-pin SOIC package. Pin #1 is the Chip Select (CS). Pin #2 is the Serial Output (SO). Pin #3 is Write Protect (WP). Pin #4 is the ground (Vss). Pin #5 is the Serial Input (SI). Pin #6 is the serial clock (SCK). Pin #7 is the Hold Input (HOLD)., and Pin #8 is the power supply (Vcc) pin.

The Turbo IC 25C128/25C256 uses the Serial Peripheral Interface (SPI), allowing operation on a three-wire bus. The Turbo IC 25C128/25C256 has separate data input (SI) and data output (SO) pins. The serial clock (SCK) pin controls the data transfer. Access to the device is controlled through the chip select (CS) input.

The Turbo IC 25C128/25C256 provides the block write inhibit feature where the user has the option of inhibiting writes to 3 different sizes of the memory array. A write protect (WP) pin is provided to prevent inadvertent writes to the status register. The Turbo 25C128/25C256 can also be put on hold during any serial communication by asserting the hold (HOLD) pin.

PIN DESCRIPTION

CHIP SELECT (CS)
The CS input pin selects the Turbo IC 25C128/25C256. A high to low transition on CS selects the Turbo IC 25C128/25C256, and keeping CS low keeps the device activated. When CS is brought high, the Turbo IC 25C128/25C256 is de-selected and the serial output pin (SO) is at high impedance.

SERIAL DATA OUTPUT (SO)
The serial output pin is a push-pull serial data output. During read, the data is shifted out onto SO on the falling edge of the serial clock.

WRITE PROTECT (WP)
The WP input pin controls the status register write protect feature. For normal read and write operations, the WP pin is held high. When the WP pin is low and the WPEN bit in the status register is "1", all write operations to the status register are inhibited. The WP pin function is blocked when the WPEN bit is "0". This feature allows a user to install the Turbo IC 25C128/25C256 into a system with the WP pin tied to ground and still be able to program the status register. The WP pin function will then be enabled when the WPEN bit is set to "1".

SERIAL DATA INPUT (SI)
The SI input pin accepts all opcodes, addresses, and write data to be input into the Turbo IC 25C128/25C256. The data is latched on the rising edge of the serial clock.

SERIAL DATA CLOCK (SCK)
The SCK input pin controls the serial bus timing of the data transfer that occurs on the serial input pin and the serial output pin.

DATA TRANSFER PAUSE (HOLD)
The HOLD input pin pauses the data transfer, allowing the host to service higher-priority interrupts. Once the device is selected and serial communication between the controller and the device is under way, a high to low transition on HOLD while SCK is low freezes the serial communication. Transitions on the SI and SCK pins are ignored, and the SO pin is at high impedance. To resume the serial communication, HOLD is set high while SCK is low. The serial sequence restarts from where it had stopped with no loss of continuity. HOLD should always be high during normal operation.

DEVICE OPERATION

The Turbo IC 25C128/25C256 has an 8-bit instruction register and an 8-bit status register. The instruction register stores one of the operation codes defined in Table 1.

Table 1. Operation Codes

Instruction Name	Operation Code	Operation Description
WREN	00000110	Set Write Enable Latch
WRDI	00000100	Reset Write Enable Latch
RDSR	00000101	Read Status Register
WRSR	00000001	Write Status Register
READ	00000011	Read Data from Memory Array
WRITE	00000010	Write Data to Memory Array

In SPI bus convention, the master provides the serial clock and initiates the data transfer. The Turbo IC 25C128/25C256 are the slave devices in all applications. The master selects the Turbo IC 25C128/25C256 by pulling $\overline{CS}$ of the device low. Once the device is active, the master sends the operation code into the instruction register.

The write enable latch is cleared upon power up and at the end of the write cycle of a write instruction. Therefore, the WREN instruction precedes all write instructions because the write enable latch must be set before a write can be executed. The WRDI instruction is used to clear the write enable latch through software.

The status register gives the current operation status of the Turbo IC 25C128/25C256. The contents of the status register is given in Table 2.

Table 2 Status Register Contents

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN	X	X	X	BP1	BP0	WEN	BSY

Where, WPEN is the write protect enable bit. Setting WPEN to a "1" enables the hardware write protect, and a "0" disables the hardware write protect. This bit is non-volatile and is programmed by the WRSR instruction. This bit works in conjunction with the the Write Protect ($\overline{WP}$) pin to control the hardware write protect feature. Hardware write protection is enabled when the $\overline{WP}$ pin is low and the WPEN bit is "1". Hardware write protection is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is "0". When the hardware write protection is on, only the writes to the the non-volatile bits (WPEN, BP1, BP0) are disabled. It is noted that the write enable latch must also be set before the non-volatile bits can be programmed.

Bits[6:4] are "0" except when the internal write cycle is in progress. These bits are read-only. BP[1:0] are the block write protect bits. These bits specifies which blocks in the memory array are write protected, as indicated in Table 3. These bits are non-volatile and are programmed by the WRSR instruction.

WEN indicates the status of the write enable latch. A "1" means that the write enable latch is set. A "0" means that the write enable latch is cleared. This bit is read-only.

BSY indicates the status of the internal write cyle to the memory array. A "1" means that the write cycle is in progress. A "0" means the write cycle has finished and the device is ready for the next instruction. This bit is read-only.

Table 3 Block "Write Protect" Assignment

Status Register		Fraction of Array	Write Protected Memory Blocks	
BP1	**BP0**	**Write Protected**	**25C128**	**25C256**
0	0	0	None	None
0	1	1/4	3000-3FFF	6000-7FFF
1	0	1/2	2000-3FFF	4000-7FFF
1	1	All	0000-3FFF	0000-7FFF

The contents of the status register can be read by the RDSR instruction. The write protect enable bit, the block write protect bit, the write enable status, and the busy status of the Turbo IC 25C128/25C256 can be found through RDSR. Three bits of the status register can be altered by the WRSR instruction. The write protect enable bit can be set to enable the hardware write protect, and the block write protect bits can be set to control the number of blocks to be write protected, according to Table 3. When the status register is being programmed, the RDSR instruction can be used to check the status of the BSY bit. All the other bits will read back ones during an internal write cycle.

READ OPERATION

The data in the memory array of the Turbo IC 25C128/25C256 can be read as follows: The master pulls the $\overline{CS}$ pin of the Turbo IC 25C128/25C256 low, and issues a READ instruction to the SI pin, which is loaded into the instruction register. The two address bytes of the memory location to be read are sent next, which are loaded into the address counter. The two most significant bits of the address are don't cares for 25C128 while the first MSB of the address is don't care for the 25C256. The data byte in the memory is shifted out onto the SO pin on the falling edge of SCK. After the data byte is shifted out, the address counter is incremented by one. The next data byte is shifted out. The sequential read continues for as long as the master provides the clock and keeps $\overline{CS}$ low. When the address counter reaches the highest address, it rolls over to the zero address (0). The read is terminated by bringing $\overline{CS}$ high.

WRITE OPERATION

The write data can be written into the memory array of the selected Turbo IC 25C128/25C256 as follows: The master pulls the $\overline{CS}$ pin of the selected Turbo IC 25C128/25C256 low, and issues a WREN instruction to the SI pin, which is loaded into the instruction register. Then the master brings $\overline{CS}$ high to set the WREN latch. The master pulls the $\overline{CS}$ pin low, and issues the WRITE instruction to the SI pin, which is loaded into the instruction register. The two address bytes of the memory location to be written are sent next, which are loaded into the address counter. The first most significant bit of the address is a don't care for the 25C256 and the first two MSBs are don't cares for the 25C128. The data byte to be written is sent next. The data byte is stored in a data byte latch. The address counter is incremented by one after the data byte is shifted in. Up to 64 data bytes can be sent before a write cycle is necessary. To start the internal write cycle, the $\overline{CS}$ must be brought high after the least significant bit (D0) of the last data byte has been loaded. If $\overline{CS}$ is brought high at any other time, the write cycle will not start.

To check whether the write programming has finished, the master pulls $\overline{CS}$ low, and issues the RDSR instruction. The contents of the status register is shifted out onto the SO pin. The BSY bit can be checked. If BSY is "1", the write programming is still in progress. If BSY is "0", the write programming has finished. At the end of the write cycle, the WREN latch is automatically reset.

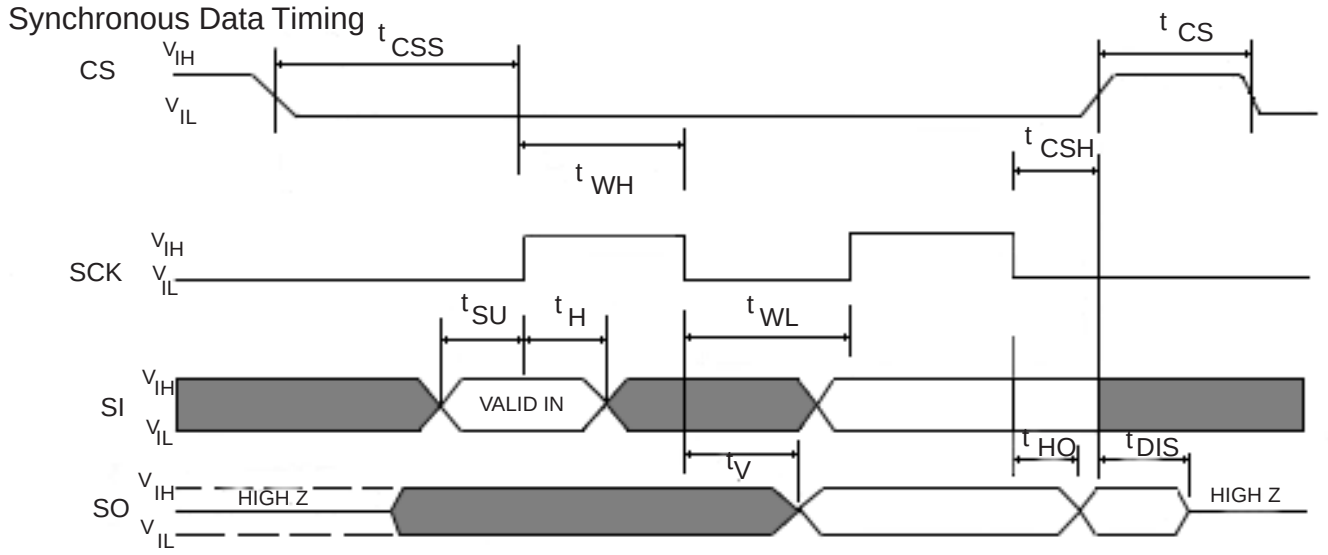
INQUIRY

Please Contact :

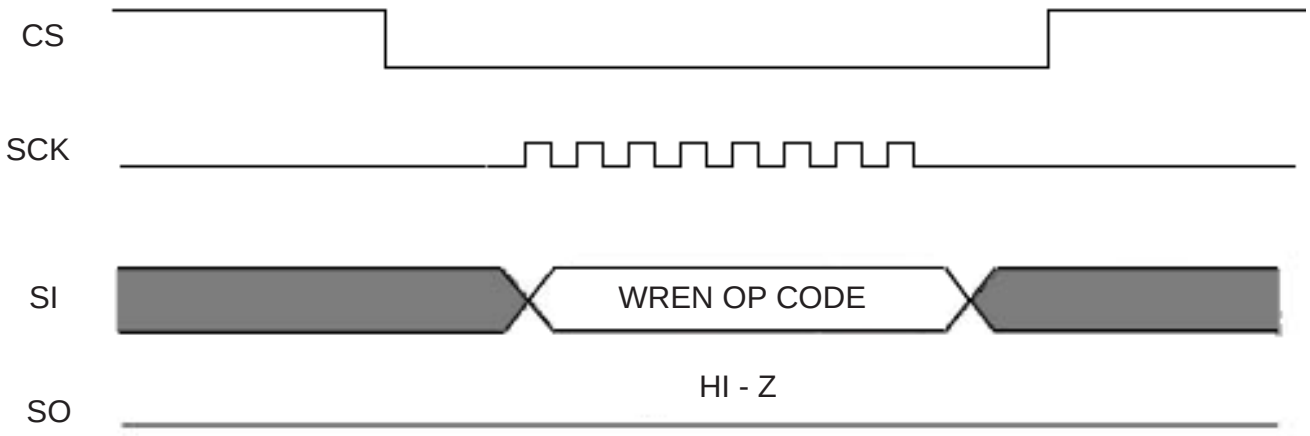
Turbo IC, Inc., U.S.A.
Phone : 408-324-0288
Fax : 408-324-0289

Timing Diagrams for Mode 1 (0,0)

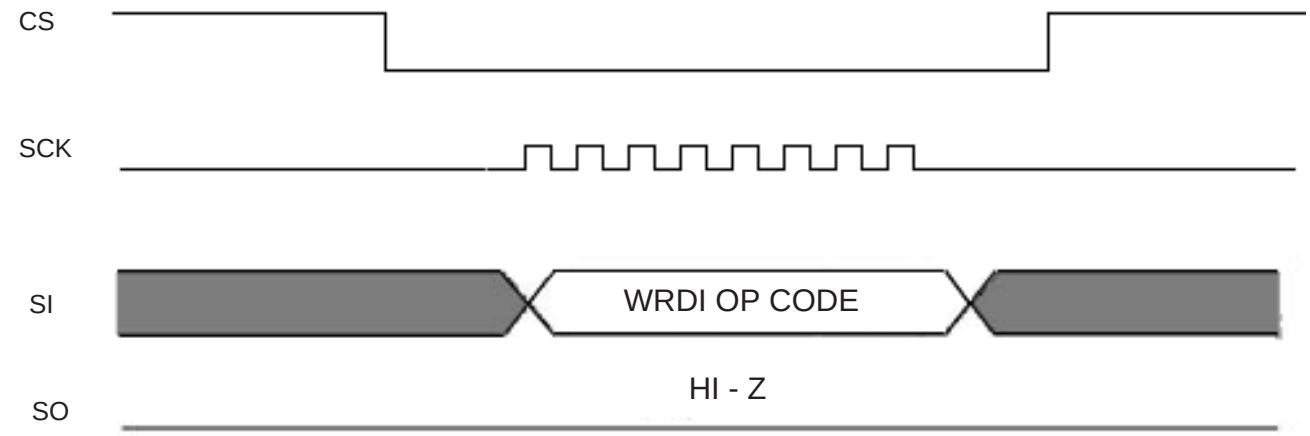
Synchronous Data Timing



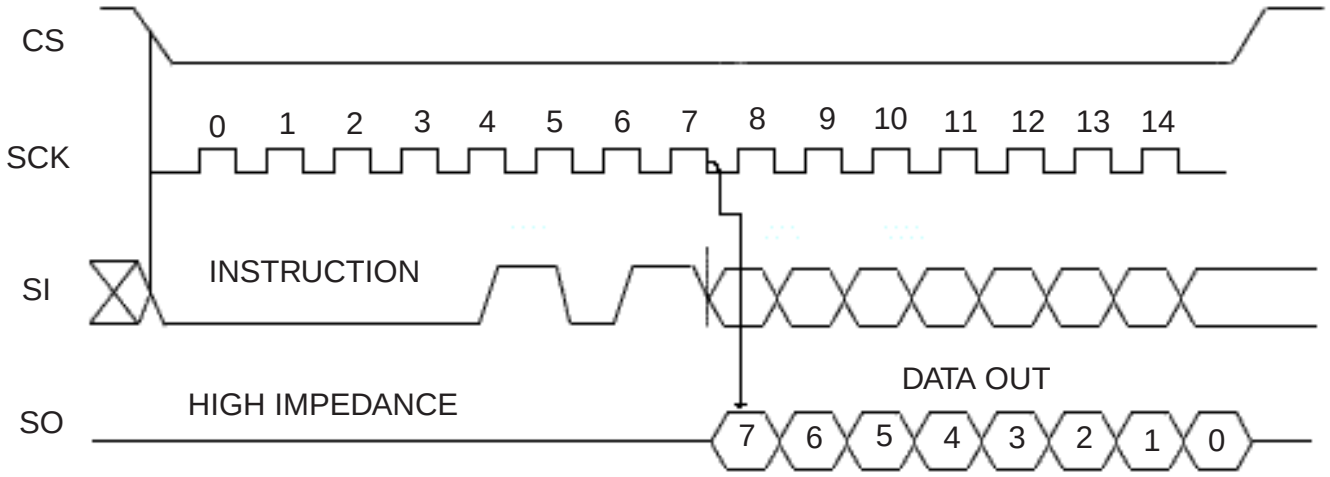
WREN Timing



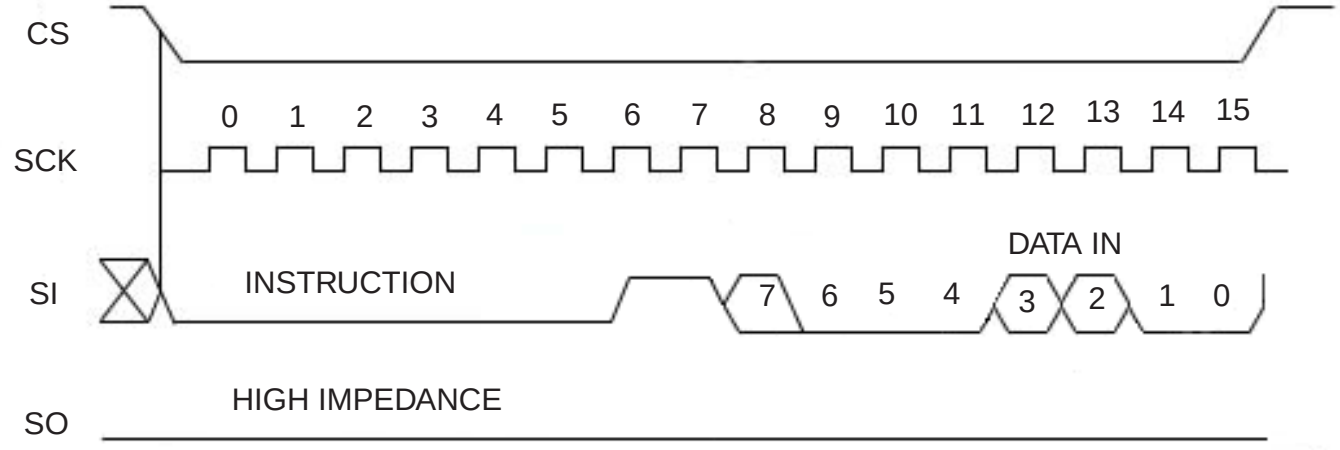
WRDI Timing



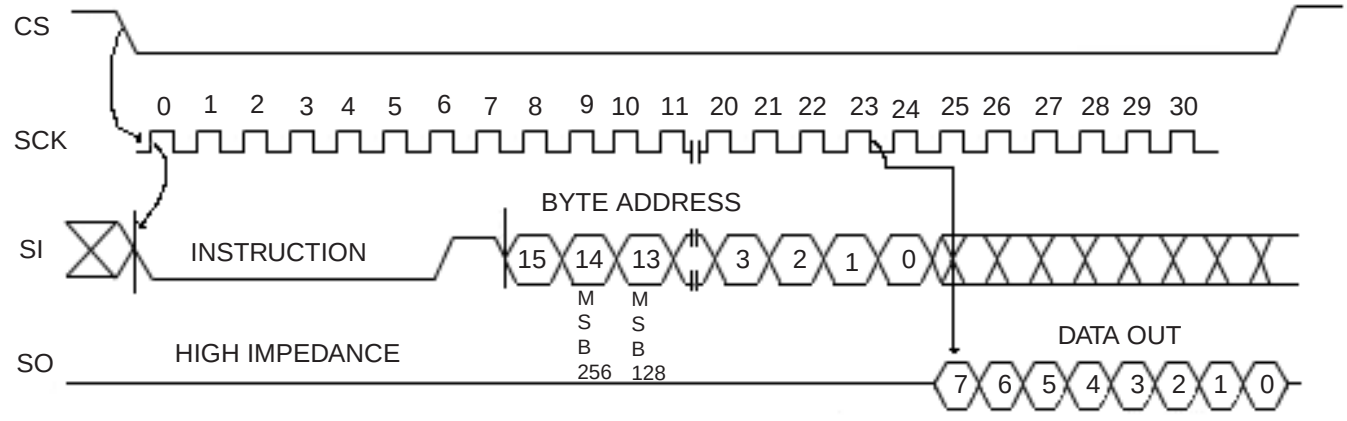
RDSR Timing



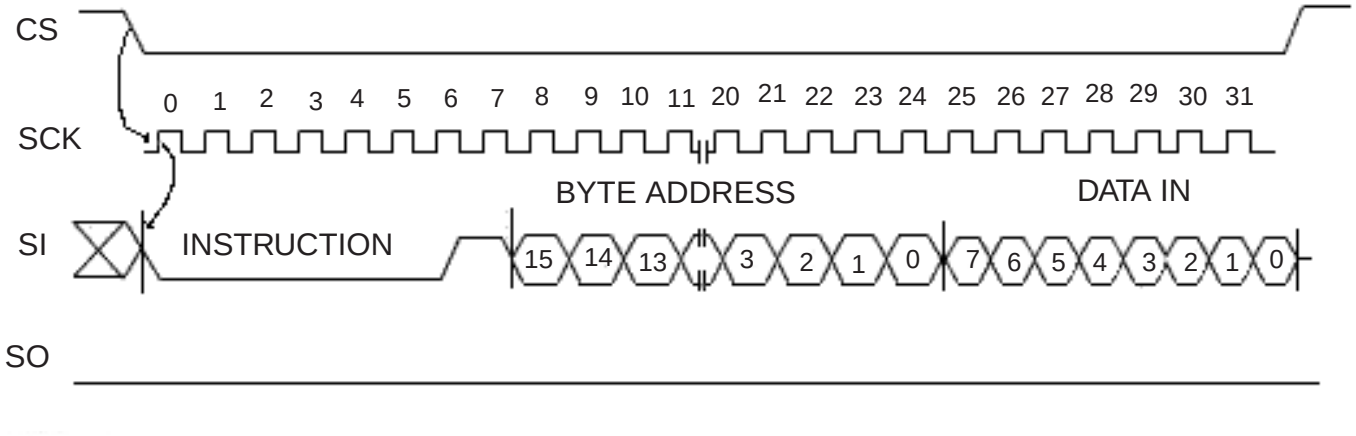
WRSR Timing



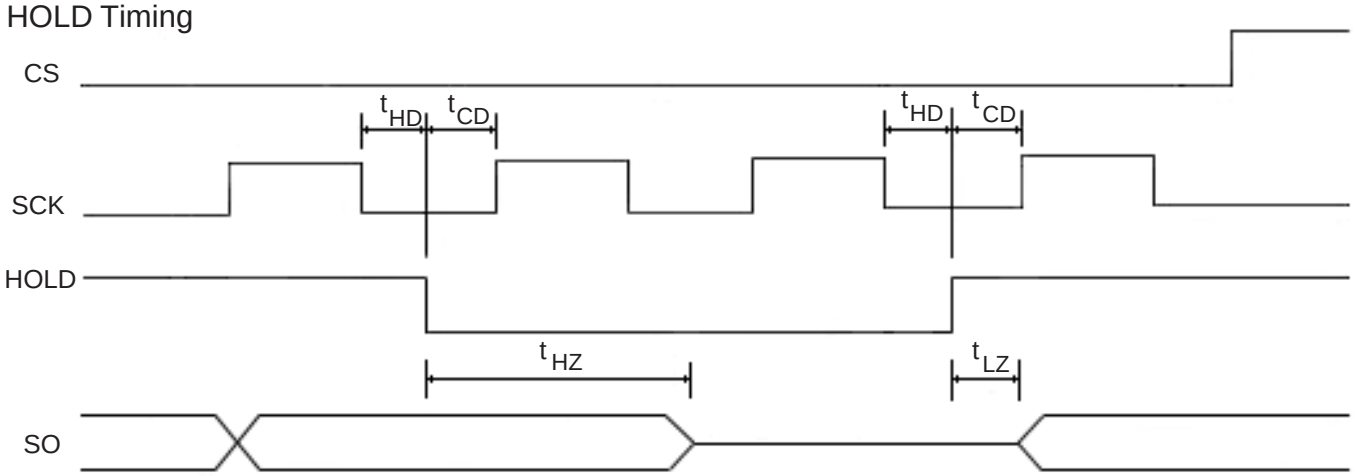
READ Timing



WRITE Timing



HOLD Timing



ABSOLUTE MANXIMUM RATINGS

TEMPERATURE
Storage: -65° C to 150° C
Under Bias: -55° C to 125° C

ALL INPUT OR OUTPUT VOLTAGES
with respect to Vss +6 V to -0.3 V

* "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature Range: Commercial: 0° C to 70° C
Industrial: -40° C to 85° C

Vcc Supply Voltage: 2.7 to 5.5 Volts
4.5 to 5.5 Volts

Endurance: 100,000 Cycles/Byte
Data Retention: 100 Years

D.C. CHARACTERISTICS

Symbol	Parameter	Condition	Min	Max	Units
Icc1	Active Vcc Current	VCC = 2.7 V at 1 Mhz SO= Open		3.0	mA
Icc2	Active Vcc Current	VCC = 5.0 V at 2 Mhz S0= Open		5.0	mA
Isb1	Standby Current	Vcc = 2.7 v		0.5	uA
Isb2	Standby Current	Vcc = 5.5 v		2.0	uA
Iil	Input Leakage Current	Vin=Vcc Max		3	uA
Iol	Output Leakage Current			3	uA
Vil	Input Low Voltage		-0.5	Vccx0.2	V
Vih	Input High Voltage		Vccx0.7	Vcc+0.5	V
Vol2	Output Low	Vcc=4.5v Iol=3.0 mA		0.4	V
Vol1	Output Low	Vcc=2.7v Iol=1.5 mA		0.3	V
Voh2	Output High	Vcc=4.5v Ioh=-1.6mA	Vcc-0.8		V
Voh1	Output High	Vcc=2.7v Iolh=-100uA	Vcc-0.8		V

A.C. TEST CONDITIONS

Output Load : 1 TTL Load and Cl=100 pF

A.C. CHARACTERISTICS

Symbol	Parameter	2.7 volt		5.5 volt		
		Min	Max	Min	Max	Units
fSCK	SCL Clock Frequency		1.0		2.1	MHz
TRi	Input Rise Time		2		2	us
tF1	Input Fall Time		2		2	us
tWH	SCK High Time	400		200		ns
tWL	SCK Low Time	400		200		ns
tCS	CS High Time	500		250		ns
tCSS	CS Setup Time	500		250		ns
tCSH	CS Hold Time	500		250		ns
tSU	Data-in Setup Time	50		50		ns
tH	Data-in Hold Time	50		50		ns
tHD	Hold Setup Time	200		100		ns
tCD	Hold Hold Time	200		100		ns
tV	Output Valid		400		200	ns
tHO	Output Hold Time					ns
tLZ	Hold to Output Low Z		100		100	ns
tHZ	Hold to Output High Z		100		100	ns
tDIS	Output Disable Time		250		250	ns
tWC	Write Cycle Time		10		10	ms

Part Numbers & Order Information

TU25C128/25C256PC-2.7

16K/32K X 8 Serial EEPROM	Package	Temperature	Operating Voltage
	P -PDIP	**C -Commercial**	blank 4.5 to 5.5 V
	S -SOIC	I -Industrial	**-2.7 2.7 to 5.5 V**