Turbo IC, Inc.

28C256A

HIGH SPEED CMOS
256K ELECTRICALLY ERASABLE PROGRAMMABLE ROM
32K X 8 BIT EEPROM

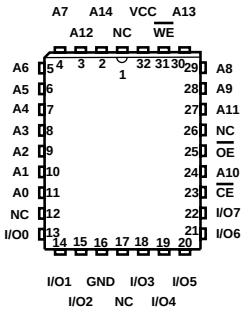
FEATURES:

- 120 ns Access Time
- Automatic Page Write Operation
  - Internal Control Timer
  - Internal Data and Address Latches for 64 Bytes
- Fast Write Cycle Times
  - Byte or Page Write Cycles: 10 ms
  - Time to Rewrite Complete Memory: 5 sec
  - Typical Byte Write Cycle Time: 160 µsec
- Software Data Protection
- Low Power Dissipation
  - 50 mA Active Current
  - 200 µA CMOS Standby Current
- Direct Microprocessor End of Write Detection
  - Data Polling
- High Reliability CMOS Technology with Self Redundant EEPROM Cell
  - Endurance: 100,000 Cycles
  - Data Retention: 10 Years
- TTL and CMOS Compatible Inputs and Outputs
- Single 5 V ± 10% Power Supply for Read and Programming Operations
- JEDEC Approved Byte-Write Pinout

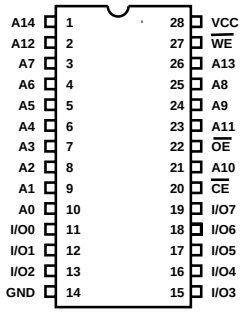
DESCRIPTION:

The Turbo IC 28C256A is a 32K X 8 EEPROM fabricated with Turbo's proprietary, high reliability, high performance CMOS technology. The 256K bits of memory are organized as 32K by 8 bits. The device offers access time of 120 ns with power dissipation below 250 mW.

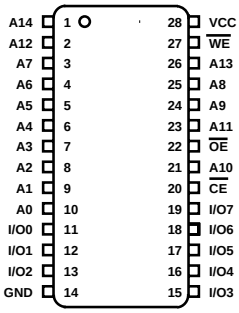
The 28C256A has a 64-bytes page write operation, enabling the entire memory to be typically written in less than 5.0 seconds. During a write cycle, the address and 1 to 64 bytes of data are internally latched, freeing the address and data bus for other microprocessor operations. The programming process is automatically controlled by the device using an internal control timer. Data polling on one or all I/O can be used to detect the end of a programming cycle. In addition, the 28C256A includes an user-optional software data write mode offering additional protection against unwanted (false) write. The device utilizes an error protected self redundant cell for extended data retention and endurance.



32 pins PLCC



28 pins PDIP



28 pins SOIC (SOG)

28 pins TSOP

PIN DESCRIPTION

ADDRESSES (A0 - A14)
The Addresses are used to select an 8 bits memory location during a write or read operation.

OUTPUT ENABLE ($\overline{OE}$)
The Output Enable input activates the output buffers during the read operations.

CHIP ENABLES ($\overline{CE}$)
The Chip Enable input must be low to enable all read/write operation on the device. By setting $\overline{CE}$ high, the device is disabled and the power consumption is extremely low with the standby current below 200 µA.

WRITE ENABLE ($\overline{WE}$)
The Write Enable input initiates the writing of data into the memory.

DATA INPUT/OUTPUT (I/O0-I/O7)
Data Input/Output pins are used to read data out of the memory or to write Data into the memory.

DEVICE OPERATION

READ:

The 28C256A is accessed like a static RAM. Read operations are initiated by both $\overline{CE}$ and $\overline{OE}$ going low and terminated by either $\overline{CE}$ or $\overline{OE}$ returning high. The outputs are at the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ returns high. The two line control architecture gives designers flexibility in preventing bus contention.

WRITE:

A write cycle is initiated when $\overline{CE}$ and $\overline{WE}$ are low and $\overline{OE}$ is high. The address is latched internally on the falling edge of $\overline{CE}$ or $\overline{WE}$ whichever occurs last. The data is latched by the rising edge of $\overline{CE}$ or $\overline{WE}$ whichever occurs first. Once a byte write cycle has been started, the internal timer automatically generates the write sequence to the completion of the write operation.

PAGE WRITE OPERATION:

The page write operation of 28C256A allows one to 64 bytes of data to be serially loaded into the device and then simultaneously written into memory during the internally generated write cycle. After the first byte has been loaded, successive bytes of data may be loaded until the full page of 64 bytes is loaded. Each new byte to be written must be loaded within 200 µs of the previously loaded byte. The page address defined by the addresses A6-A14 is latched by the first $\overline{CE}$ or $\overline{WE}$ falling edge which initiates a writing cycle and they will stay latched until the completion of the page write. Any changes in the page addresses during the load-write cycle will not affect the initially latched page addresses. Addresses A0 - A5 are used to define which bytes will be loaded and written within the 64 bytes page. The bytes may be loaded in any order that is convenient to the user. The content of a loaded byte may be altered at any time during the loading cycle if the maximum allowed byte-load time (200 µs) is not exceeded. Only loaded bytes within the page will be written; no rewriting will occur to the non-selected bytes in the page.

DATA POLLING:

The 28C256A features $\overline{DATA}$ POLLING to indicate the completion of a write cycle to the host system. During a byte or page write cycle, an attempted read of the last byte loaded into the page will result in the complement of the loaded byte on all outputs I/O0 - I/O7 (i.e. loaded data 01010110, read data 10101001). Data Polling feature may be used by an attempted read on one or more outputs (whatever is convenient for the system developer). Once the write cycle has been completed, true data is valid on all outputs and the next cycle may be started.

DATA PROTECTION:

The 28C256A has three hardware features to protect the written content of the memory against inadvertent writes :

a.) Vcc threshold detector: If Vcc is below 2.5 V, the write capabilities of the chip is inhibited for whatever input conditions.

b.) Noise protection: A $\overline{WE}$, $\overline{OE}$, or $\overline{CE}$ pulse less than 10 ns in width is not able to initiate a write cycle.

c.) Write inhibit: Holding $\overline{OE}$ at low, or $\overline{CE}$ at high, or $\overline{WE}$ at high inhibits the write cycle.

SOFTWARE WRITE PROTECTION:

The 28C256A offers a software controlled data write protection feature. The device is delivered to the user with the software data write protection DISABLED; i.e. the device will go to the data write operation as long as Vcc exceeds 2.5 V and $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ inputs are set at write mode levels. The 28C256A can be automatically protected against an accidental write operation during power-up or power-down without any external circuitry by enabling the software data write protection features. This features is enabled after the first write cycle which includes the software algorithm. After this operation is done, the data write function of the device may be performed only if every page write cycle is preceded by the software algorithm. The device will maintain its software protect feature for the rest of its life unless that the software algorithm for disabling the protection is implemented.

SOFTWARE ALGORITHM:

The 28C256A has an internal register for the software algorithm which enables the memory to provide the user with additional features:

a.) Software Write Protect Enable

A sequence of three dummy data writes to the memory will activate internal EEPROM fuses during the first page write cycle. These EEPROM fuses will reject any write attempts of new pages of data unless the three dummy data writes are repeated at the beginning of any page writes. The timing for the dummy data and addresses must be the same as for a normal write operation. A violation of the three steps write protect sequence in data or address timing and content will abort the procedure and reset the device to the starting point condition.

Note: After the three dummy data writes, at least one page load/ write cycle must be performed. If no additional page data is added to the three dummy data writes, the software write protect will not be enabled until the next write, which will not be protected. Table 1 shows the required procedure for enabling the software write protect:

Step	Mode	Address A14-A0	Data I/O 7-0
1	Page Write	5555 Hex	AA Hex
2	Page Write	2AAA Hex	55 Hex
3	Page Write	5555 Hex	A0 Hex
4-67	Page Write	Address	Data

b.) Software Write Protect Disable

The software algorithm of 28C256A includes a six steps sequence of dummy data writing to disable the software write protect feature described in a.). The six steps write sequence shown in Table 2 must be performed at the beginning of a page write cycle. A violation of the six steps write sequence in data or address timing and content will abort the procedure and reset the chip to the starting point condition. After a page write cycle including the six steps write sequence has been performed, the 28C256A does not require the use of three dummy data writes described in a.) for the following page write cycle. The device is at the software write protect disabled state.

Note: After the six dummy data writes, at least one page load/ write cycle must be performed. If no additional page data is added to the six dummy data writes, the software write protect disable will not be activated. Table 2 shows the required procedure for disabling the software write protect:

Step	Mode	Address A14-A0	Data I/O 7-0
1	Page Write	5555 Hex	AA Hex
2	Page Write	2AAA Hex	55 Hex
3	Page Write	5555 Hex	80 Hex
4	Page Write	5555 Hex	AA Hex
5	Page Write	2AAA Hex	55 Hex
6	Page Write	5555 Hex	20 Hex
7-70	Page Write	Address	Data

c.) Software Chip Clear

The software algorithm of 28C256A includes a sequence of six steps dummy data writing to perform a chip clear operation. Table 3 shows the six steps write sequence to perform the software chip clear operation:

Step	Mode	Address A14-A0	Data I/O 7-0
1	Page Write	5555 Hex	AA Hex
2	Page Write	2AAA Hex	55 Hex
3	Page Write	5555 Hex	80 Hex
4	Page Write	5555 Hex	AA Hex
5	Page Write	2AAA Hex	55 Hex
6	Page Write	5555 Hex	10 Hex

At the end of the six steps write sequence shown in Table 3, the device automatically activates its internal timer to control the chip

erase cycle; typically takes 20 msec. After a software chip clear operation has been completed, all 256K bit locations of memory show high level at read operation mode.

d.) Software Autoclear Disable Mode

This software algorithm disables the internal automatic clear before write cycle. Table 4 shows the six steps needed to perform the autoclear disable mode:

Step	Mode	Address A14-A0	Data I/O 7-0
1	Page Write	5555 Hex	AA Hex
2	Page Write	2AAA Hex	55 Hex
3	Page Write	5555 Hex	80 Hex
4	Page Write	5555 Hex	AA Hex
5	Page Write	2AAA Hex	55 Hex
6	Page Write	5555 Hex	40 Hex
7-70	Page Write	Address	Data

Page write operation using the software autoclear disable mode will reduce programming time to typically 5 msec. The page write using software autoclear disable mode is usually used after a chip clear or a software chip clear operation. At the end of the six steps sequence, the autoclear before write is disabled and will stay that way unless a power-down occurs or the software autoclear enable procedure is initiated.

e.) Software Autoclear Enable Mode

Automatic page clear before page write can be restored to 28C256A either by Vcc power-down or by software autoclear enable mode. Table 5 shows the six steps page write procedure needed to enable software autoclear mode:

Step	Mode	Address A14-A0	Data I/O 7-0
1	Page Write	5555 Hex	AA Hex
2	Page Write	2AAA Hex	55 Hex
3	Page Write	5555 Hex	80 Hex
4	Page Write	5555 Hex	AA Hex
5	Page Write	2AAA Hex	55 Hex
6	Page Write	5555 Hex	50 Hex
7-70	Page Write	Address	Data

D.C. CHARACTERISTICS

(C) = COMMERCIAL
(I) = INDUSTRIAL
(M) = MILITARY

Symbol	Parameter	Condition	Min	Max	Units	
Icc	Active Vcc Current	$\overline{CE}$=$\overline{OE}$=Vil; All I/O Open, Min Read or Write Cycle Time		50	(C)	mA
				70	(I)	mA
				90	(M)	mA
Isb1	CMOS Standby Current	$\overline{CE}$=Vcc-0.3 V to Vcc+1 V		200	(C)	µA
				300	(I&M)	µA
Isb2	TTL Standby Current	$\overline{CE}$=Vih, $\overline{OE}$=Vil, All I/O Open, Other Inputs=Vcc Max Vin=Vcc Max		3		mA
Iil	Input Leakage Current			1		µA
Iol	Output Leakage Current			10		µA
Vil	Input Low Voltage		-0.1	-0.8		V
Vih	Input High Voltage		2	Vcc+0.3		V
Vol	Output Low Voltage	Iol=2.1 mA		0.45		V
Voh	Output High Voltage	Ioh=-0.45 mA	2.4			V

ABSOLUTE MAXIMUM STRESS RANGES *

TEMPERATURE

Storage:	-65° C to 150° C
Under Bias:	-55° C to 125° C

ALL INPUT OR OUTPUT VOLTAGES

with respect to Vss	+6 V to -0.3 V

"Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature Range:	Commercial:	0° C to 70° C
	Industrial:	-40° C to 85° C
	Military:	-55° C to 125° C
Vcc Supply Voltage:	5 V ± 10%	
Endurance:	100,000 Cycles/Byte (Typical)	
Data Retention:	10 Years	

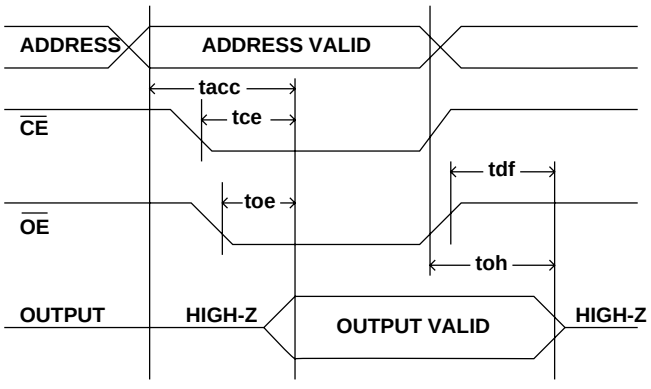
A.C. CHARACTERISTICS - READ OPERATION

		28C256A-1		28C256A-2		28C256A-3		28C256A-4		
Symbol	Parameters	Min	Max	Min	Max	Min	Max	Min	Max	Unit
tacc	Address to Output Delay		120		150		200		250	ns
tce	$\overline{CE}$ to Output Delay		120		150		200		250	ns
toe	$\overline{OE}$ to Output		70		90		110		150	ns
tdf	$\overline{OE}$ to Output In High Z	0	40	0	60	0	90	0	90	ns
toh	Output Hold from Address Changes, Chip Enable or Output Enable Whichever Occurs First	0		0		0		0		ns

A.C. TEST CONDITIONS

Output Load : 1 TTL Load and Cl=100 pF
Input Rise and Fall Times : < 10 ns
Input Pulse Level : 0 V to 3 V
Timing Measurement Reference Level : 1.5 V

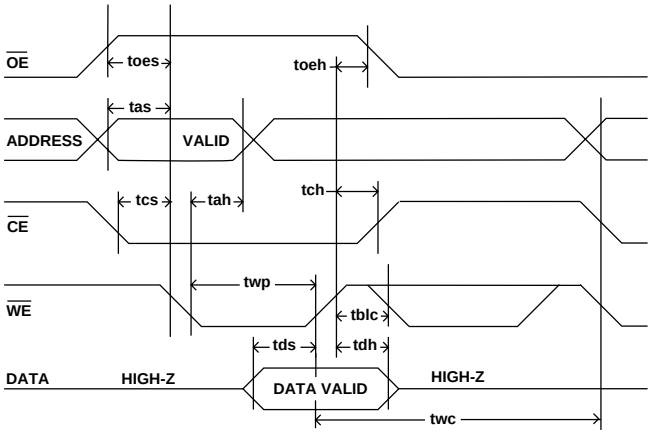
A.C. Read Wave Forms



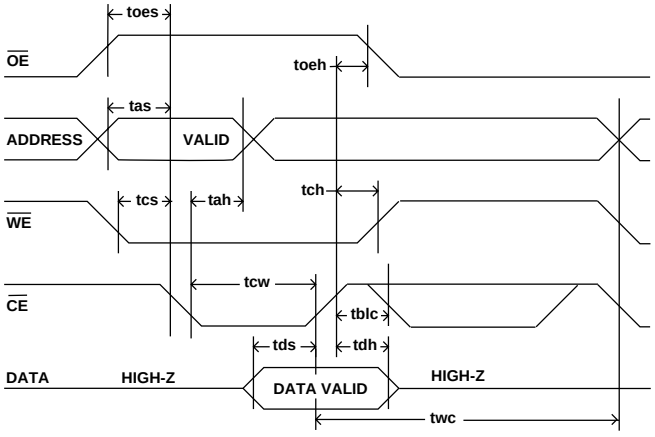
A.C. WRITE CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
tas	Address Set-up Time	20		ns
tah	Address Hold Time	100		ns
tcs	Write Set-up Time	0		ns
tch	Write Hold Time	0		ns
tcw	$\overline{CE}$ Pulse Width	150		ns
twp	$\overline{WE}$ Pulse Width	150		ns
toes	$\overline{OE}$ Set-up Time	20		ns
toeh	$\overline{OE}$ Hold Time	20		ns
tds	Data Set-up Time	50		ns
tdh	Data Hold Time	0		ns
tdh	Data Hold (28C256A-4 ONLY)	10		ns
tblc	Byte Load Cycle	0.2	200	µs
tlp	Last Byte Loaded to Data Polling Output		500	µs
twc	Write Cycle Time		10	ms
twc	Write Cycle Time (IND & MIL)		15	ms

A.C. Write Characteristics $\overline{WE}$-Controlled



A.C. Write Characteristics $\overline{CE}$-Controlled



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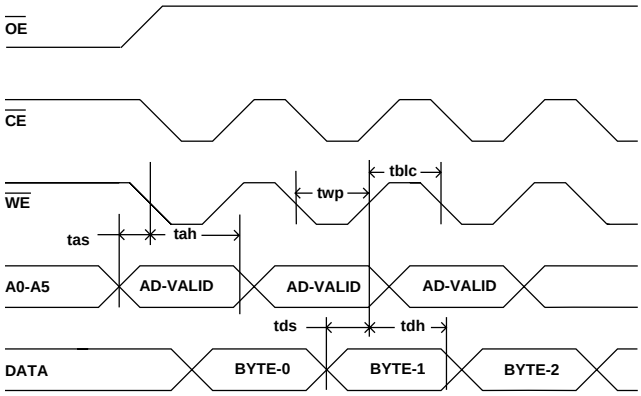
PAGE MODE WRITE CHARACTERISTICS

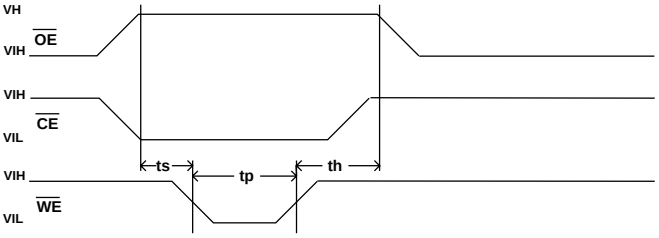
Symbol	Parameter	Min	Max	Unit
twc	Write Cycle Time		10	ms
tas	Address Set-up Time	20		ns
tah	Address Hold Time	100		ns
tds	Data Set-up Time	50		ns
tdh	Data Hold Time	0		ns
twp	Write Pulse Width	150		ns
tblc	Byte Load Cycle Time	0.2	200	µs

Page Mode Write Wave Form



Chip Clear Wave Form

The content of the 28C256A may be altered to HIGH by the use of the Chip Clear operation. By setting $\overline{CE}$ to low, $\overline{OE}$ to 12 volts, and $\overline{WE}$ to low, the entire memory can be cleared (written HIGH) within 20 ms. The Chip Clear operation is a latch operation mode. After the Chip Clear starts, the internal chip timer takes over and completes the clear without $\overline{CE}$, $\overline{OE}$ and $\overline{WE}$ being held active.



ts= 20 ns
tp= 200 ns
th= 20 ns
VH=12.0 V±0.5V

Part Numbers & Order Information

28C256APC-2

32K x 8 EEPROM

Package	Temperature	Speed
J -PLCC	**C -Commercial**	-1 120 ns
P -PDIP	I -Industrial	**-2 150 ns**
S -SOIC	M -Military	-3 200 ns
T -TSOP		-4 250 ns