Turbo IC, Inc.

93C66/93C56/93C46

PRODUCT INTRODUCTION

CMOS MICROWIRE BUS
4K/2K/1K ELECTRICALLY ERASABLE PROGRAMMABLE ROM
512/256/128 X 8/16 BIT EEPROM

FEATURES :

- Power Supply Voltage
  - Single Vcc for Read and Programming
  - (Vcc = 2.7 V to 5.5 V)
- Industry Standard Microwire Bus
- Byte (x8) or Word (x16) - Dual Organization
- Programming Instructions For
  - Byte/Word
  - Memory Array
- Self Timed Programming Cycle
  - (includes Auto - Erase)
  - 10 ms Typical Programming Time
- Signals Ready/Busy During Programming
- Sequential Read Function
- High Reliability CMOS Technology with EEPROM Cell
  - Endurance : 1,000,000 Cycles
  - Data Retention : 100 Years

DESCRIPTION:

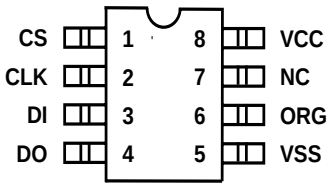
The Turbo IC 93C66/93C56/93C46 is a serial 4K/2K/1K EEPROM fabricated with Turbo's proprietary, high reliability, high performance CMOS technology. It's 4K/2K/1K of memory is organized as 512/256/128 x 8/16 bits, depending on the byte/word organization. The memory can be accessed using the MicroWire bus protocol through the Serial Data Input (DI) and the Serial Data Output (DO) pins.

The Turbo IC 93C66/93C56/93C46 is assembled in either a 8-pin PDIP or 8-pin SOIC package. Pin #1 is the Chip Select (CS) for the device. Pin #2 is the Clock (CLK) for the device. Pin #3 is the Data Input (DI) of the device. Pin #4 is the Data Output (DO) of the device. Pin #5 is the ground (Vss). Pin #6 is the Organizational Select (ORG) that allows the user to select between 8 bit or 16 bit organizational structure. Pin #7 is not connected. Pin #8 is the power supply (Vcc) pin.

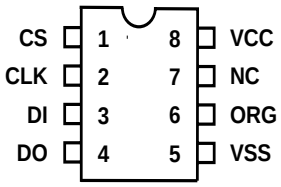
The Turbo IC 93C66/93C56/93C46 memory itself is accessed using a set of instructions that consists of the opcode, address, and the data. These instructions include Byte/Word Read, Byte/Word Write, Byte/Word Erase, and an Erase or Write All instruction. In the Byte/Word Read instruction, the instruction loads the address of the first byte/word to be read to an internal address pointer. The data at this address is then serially clocked out and the address pointer incremented. If the Chip Select (CS) pin is held High, a stream of data can be read.

Since the Turbo IC 93C66/93C56/93C46 device is self-timed, the clock pin is not required to be connected nor is it required that the pulse be stopped after the start of the Write cycle. Furthermore, programming the device does not need an erase before the Write cycle. After the start of the programming, a Busy/Ready signal is available on the Data Output (DO) pin when Chip Select (CS) is High.

PIN DESCRIPTION



8 pin SOIC



8 pin PDIP

PIN DESCRIPTION

CHIP SELECT (CS)
The chip select allows the programming of the device through an encoded opcode, address, and data.

CLOCK (CLK)
This pin is the pin that drives the sampling of input or streaming of output during programming.

ORGANIZATION SELECT (ORG)
This pin allows the user to select between 8-bit and 16-bit modes.

DATA INPUT (DI)
This pin is used in the input of the instruction, ie. the start bit, opcode, address, and data during programming.

DATA OUTPUT
This pin is used to check the device' s status during programming as well as to output the data from memory during a READ or READ ALL instruction.

Memory Organization:
The Turbo IC 93C66/93C56/93C46 device is organized as either bytes or words. If the ORG input is left unconnected or connected to VCC, the organization of words is selected. On the other hand, if the ORG input is connected to VSS (or ground), the organization of bytes is selected. Because setting the ORG input to a value between VCC and VSS causes a higher standby current, the ORG input should be set to either VCC or VSS to minimize power.

DEVICE OPERATION:

Instructions:
The Turbo IC 93C66/93C56/93C46 device has seven instructions, made active by the rising edge of the Chip Select (CS) input. The device then awaits a start bit, a '1' bit on the Data Input (DI) with a rising clock edge, to begin programming. After the start bit, a 2 - bit opcode is used to define the instruction for the device. A bit string dependent on the organization of bytes/words is then entered to tell the device which address to access.

Read:
The Read instruction (READ) outputs data on the Data Output (DO) pin. Upon decoding the instruction, the device will then decode the address and data from the memory at that address is then transferred into into an output shift register. A dummy bit, '0', is then output with the 8 bit byte or 16 bit word, depending on the organization used. The device will then automatically increment address with each rising clock edge as long as the Chip Select (CS) pin is kept High. With each clock cycle, another byte/word is output; however, no dummy bit will exist between this byte/word output.

Erase/Write Enable and Disable
The Erase/Write Enable instruction (EWEN) allows Erase/Write instructions to be executed. The Erase/Write Disable instruction (EWDS) prohibits Erase/Write instructions to be executed and the programming cycle to be disabled. When the device is first powered on, the device will be in Erase/Write Disable Instruction (EWDS) mode.

The device will remain in this mode until an Erase/Write Enable instruction (EWEN) is executed. Once the EWEN instruction is executed, it will remain in this mode until either a Erase/Write Disable instruction (EWDS) is executed or the VCC falls below the power-on reset Threshold voltage.

Erase
The Erase instruction (ERASE) programs the byte or word addressed to '1'. A falling edge of the Chip Select input (CS) will start a self-timed erase cycle. If the Chip Select input(CS) is driven High after the t_{SLSH} delay and the device is still in the erase mode in the programming cycle, data on the DI pin is ignored and the Busy signal will be returned. On the other hand, once the Erase cycle is completed and CS is driven high, the Ready signal will be given.

Write
The Write instruction (WRITE) opcode is followed by the address and the 8/16 data bits to be written to memory. The rising clock edge is when the data input is sampled. *Once the last data bit is sampled, the Chip Select (CS) pin must be driven Low to start the self-timed programming cycle.* Otherwise, the addressed location will not be programmed.

If the Chip Select input(CS) is driven High after the t_{SLSH} delay and the device is in write mode in the programming cycle, data on the DI pin is ignored and the Busy signal is returned. On the other hand, once the Write cycle is completed and CS is driven high, the Ready signal will be given.
Since the programming cycle is self-timed, the external clock signal may be disconnected or left running after the start of the write cycle. The instruction itself also has an automatic Erase cycle that executes prior to writing the data. This precludes the need to execute an Erase instruction before a Write instruction.

Note: The write cycle time t_{WC} is the time from a valid stop condition of a write sequence to the end of the internal clear / write cycle.

TABLE 1: Instruction Set for 93C46

Instr.	Description	Start Bit	Op-Code	x8 ORG Address (ORG =0)	Data	Req. Clock Cycles	x16 ORG Address (ORG=1)	Data	Req. Clock Cycles
READ	Read data from Memory	1	10	A6-A0	Q7-Q0		A5-A0	Q15-Q0	
WRITE	Write data	1	01	A6-A0	D7-D0	18	A5-A0	D15-D0	25
EWEN	Erase/Write Enable	1	00	11X XXXX		10	11 XXXX		9
EWDS	Erase/Write Disable	1	00	00X XXXX		10	00 XXXX		9
ERASE	Erase Byte or Word	1	11	A6-A0		10	A5-A0		9
ERAL	Erase All Memory	1	00	10X XXXX		10	10 XXXX		9
WRAL	Write Data to All Memory	1	00	01X XXXX	D7-D0	18	01 XXXX	D15-D0	25

TABLE 2: Instruction Set for 93C66 and 93C56

Instr.	Description	Start Bit	Op-Code	x8 ORG Address (ORG =0)	Data	Req. Clock Cycles	x16 ORG Address (ORG=1)	Data	Req. Clock Cycles
READ	Read data from Memory	1	10	A8-A0	Q7-Q0		A7-A0	Q15-Q0	
WRITE	Write data	1	01	A8-A0	D7-D0	20	A7-A0	D15-D0	27
EWEN	Erase/Write Enable	1	00	1 1XXX XXXX		12	11XX XXXX		11
EWDS	Erase/Write Disable	1	00	0 0XXX XXXX		12	00XX XXXX		11
ERASE	Erase Byte or Word	1	11	A8-A0		12	A7-A0		11
ERAL	Erase All Memory	1	00	1 0XXXX XXXX		12	10 XXXX		11
WRAL	Write Data to All Memory	1	00	0 1XXXX XXXX	D7-D0	20	01XX XXXX	D15-D0	27

Erase All:
The Erase All instruction (ERAL) sets all memory bits to '1'. A dummy address is used during the address assignment and the Erase is performed the same way as the Erase instruction.

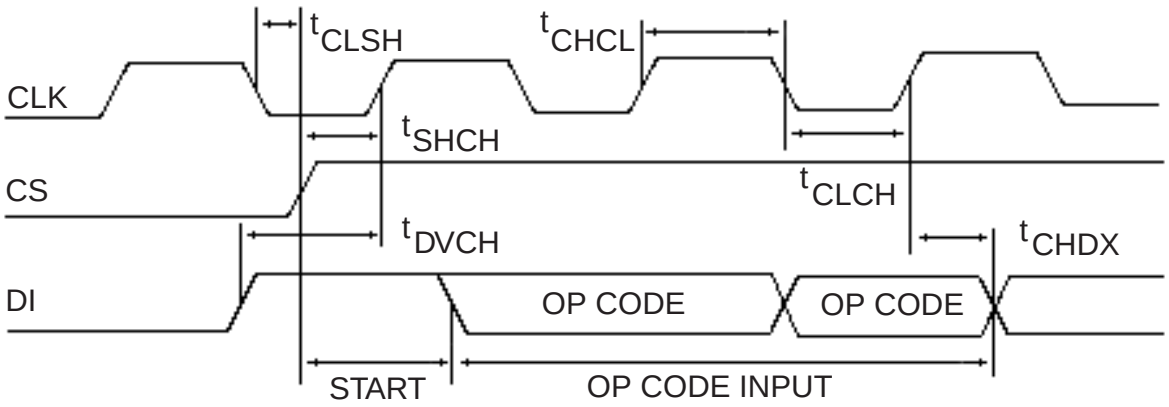
If the CS input is driven High after the t_{SLSH} delay and the Erase All operation is not complete, the device will ignore any data on the bus and return a Busy signal. On the other hand, if the CS input is driven High after the t_{SLSH} delay and the Erase All operation is complete, the device will return the Ready signal.

Write All:
The Write All instruction (WRAL) sets all memory bytes/words to the input data. Again, a dummy address is used during the address assignment.

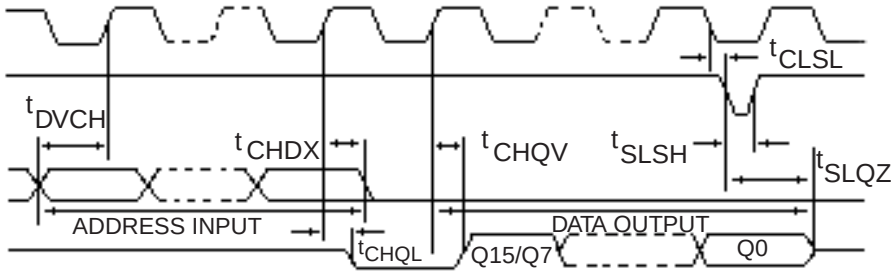
If the CS pin is driven High after the t_{SLSH} delay and the Write All operation is not complete, the device will ignore any data on the bus and return a Busy signal. On the other hand, the CS pin is driven High after the t_{SLSH} delay and the Write All operation is complete, the device will return the Ready signal.

READY/BUSY Status:
During each programming cycle, the status of the device is indicated by the Ready/Busy status of the memory if the Chip Select (CS) pin is driven High. This status is available for inspection on the Data Output (DO) pin until a new start bit is decoded or the Chip Select (CS) is driven low.

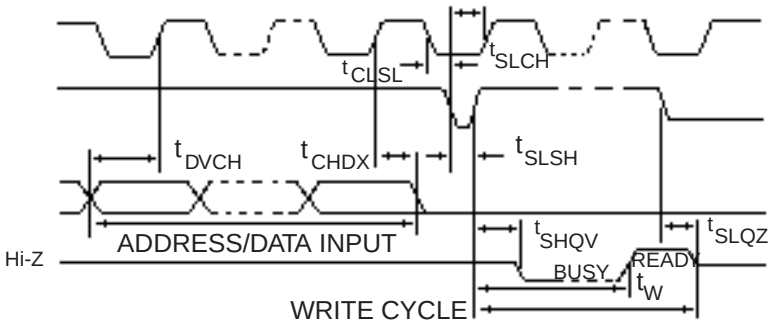
Synchronous Timing, Start and Opcode Inputs



Synchronous Read Timing



Synchronous Write Timing



ABSOLUTE MAXIMUM RATINGS

TEMPERATURE
Storage: -65° C to 150° C
Under Bias: -55° C to 125° C

ALL INPUT OR OUTPUT VOLTAGES
with respect to Vss +6 V to -0.3 V

* "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature Range:	Commercial:	0° C to 70° C
	Industrial:	-40° C to 85° C
	Military:	-55° C to 125° C
Vcc Supply Voltage:	4.5 to 5.5 Volts	
Endurance:	1,000,000 Cycles/Byte	
Data Retention:	100 Years	

D.C. CHARACTERISTICS

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Leakage Current	0V < V_{IN} < VCC		2.5	uA
I_{LO}	Active Vcc Current	0V < V_{OUT} < VCC, DO in Hi-Z		2.5	uA
I_{CC}	Supply Current (TTL inputs)	Vcc = 4.5 v, CS = V_{IH} , f= 1 Mhz		2.0	mA
	Supply Current (CMOS inputs)	Vcc = 5.5 v, CS = V_{IH}, f= 1 Mhz		2.0	mA
I_{CC1}	Supply Current (Standby)	Vcc = 5.5 v, CS = VSS, CLK = VSS, ORG = VSS or VCC		50	uA
V_{il}	Input Low Voltage		-0.3	0.8	V
V_{ih}	Input High Voltage		2	Vcc+1	V
V_{ol}	Output Low Voltage	Vcc=4.5v Iol=2.1 mA		0.4	V
V_{oh}	Output High Voltage	Vcc= 4.5v, Ioh=-400uA	2.4		V

A.C. CHARACTERISTICS

Symbol	Parameter	5.5 volt		
		Min	**Max**	**Units**
t_{SHCH}	Chip Select High to Clock High	50		ns
t_{CLSH}	Clock Low to Chip Select High	100		ns
t_{DVCH}	Input Valid to Clock High	100		ns
t_{CHDX}	Clock High to Input Transition	100		ns
t_{CHQL}	Clock High to Output Low		500	ns
t_{CHQV}	Clock High to Output Valid		500	ns
t_{CLSL}	Clock Low to Chip Select Low	0		ns
t_{SLCH}	Chip Select Low to Clock High	250		ns
t_{SLSH}	Chip Select Low to Chip Select High (1)	250		ns
t_{SHQV}	Chip Select High to Output Valid		500	ns
t_{SLQZ}	Chip Select Low to Output Hi-Z		200	ns
t_{CHCL}	Clock High to Clock Low (2)	250		ns
t_{CLCH}	Clock Low to Clock High (2)	250		ns
t_{W}	Erase/Write Cycle time		10	ms
f_{C}	Clock Frequency	0	1	Mhz

Note 1. Chip Select (CS) must be brought low for a minimum of 250ns (t_{SLSH}) between consecutive instruction cycles.
Note 2. Clock frequency specifications calls for a minimum clock period of 1us, therefore t_{CHCL} + t_{CLCH} >= 1us.

Part Numbers & Order Information

TU93C66/93C56/93C46PC

512 Serial EEPROM	**X 8/16**	**256** Serial EEPROM	**X 8/16**	**128** Serial EEPROM	**X 8/16**	Package	Temperature
						P -PDIP	**C -Commercial**
						S -SOIC	I -Industrial