Turbo IC, Inc.

29C8192

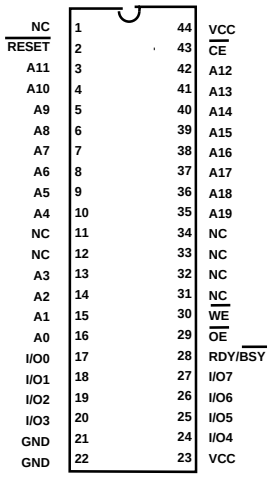
ADVANCE INFORMATION

HIGH SPEED CMOS
8 Megabit PROGRAMMABLE and ERASABLE ROM
1024K X 8 BIT FLASH PEROM

FEATURES:

- Single Supply Voltage for Read and Program Operations
  Vcc = 1.8V to 3.6V
- Fast Read Access Time
  - 150ns for Vcc = 2.7V to 3.6V
  - 200ns for Vcc = 1.8V to 3.6V
- Sector Program Operation
  - Single Cycle Reprogram (Erase & Program)
  - 256 Sectors (4096 bytes/sector)
  - Internal Address and Data Latches for 4096 Bytes
- Automatic Sector Programming Operation
  - Internal Control Timer
- Fast Program Times
  - Sector Program (Erase & Write) Cycles : 40 ms Typical
  - Total Time to Reprogram the Entire Memory (256 sectors) : 10 s Typical
  - Typical Byte Program Cycle Time: 10 µs
- JEDEC Standard Software Data Protection
- Low Power Dissipation
  - 15 mA Active Current
  - 20 µA CMOS Standby Current
- Direct Microprocessor End of Program Detection
  - Data Polling
- High Reliability CMOS Technology
  - Endurance: 100,000 Cycles
  - Data Retention: 10 years
- JEDEC Approved Byte Pinout

PIN CONFIGURATION:



44 pins SOIC

DESCRIPTION:

The Turbo IC 29C8192 is a 1024K x 8 Flash programmable and erasable read only memory (PEROM) fabricated with Turbo IC's proprietary, high reliability, high performance CMOS technology. Its 8192K bits of memory are organized as 1024K by 8 bits. The device offers access time of 250 ns with power dissipation below 50 mW.

The 29C8192 has a 4096 bytes sector program operation enabling the entire memory to be programmed typically in less than 10 seconds. During a program operation, the address and a complete sector (4096 bytes) of data are internally latched, freeing the address and data bus for other microprocessor operations. The programming process is automatically controlled by the device using an internal control timer. Data polling on I/O7 or a Toggle bit can be used to detect the end of a programming cycle. In addition, the 29C8192 includes an user-optional software data write mode offering additional protection against unwanted (false) write.

The 29C8192 does not require a separate high voltage to program the device. The 1.8V to 3.6Vsource is all that is required.

PIN DESCRIPTION

ADDRESSES (A0 - A19)
The Addresses are used to select an 8 bits memory location during a program or read operation.

CHIP ENABLE ($\overline{CE}$)
The Chip Enable input must be low to enable all read/program operations on the device. By setting $\overline{CE}$ high, the device is disabled and the power consumption is extremely low with the standby current below 10 µA.

OUTPUT ENABLE ($\overline{OE}$)
The Output Enable input activates the output buffers during the read operations.

WRITE ENABLE ($\overline{WE}$)
The Write Enable input initiates the programming of data into the memory.

DEVICE OPERATION

READ

The 29C8192 is accessed like a static RAM. Read operations are initiated by both $\overline{CE}$ and $\overline{OE}$ on low and terminated by either $\overline{CE}$ or $\overline{OE}$ returning high. The outputs are at the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ returns high. The two line control architecture gives designers flexibility in preventing bus contention.

PROGRAM

A program cycle is initiated when $\overline{CE}$ and $\overline{WE}$ are low and $\overline{OE}$ is high. The address is latched internally on the falling edge of the $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs first. Once a programming cycle has been started, the internal timer automatically generates the program sequence to the completion of the program operation.

SECTOR PROGRAM OPERATION

The device is reprogrammed on a sector basis. When a byte of data within a sector is to be changed, data for the entire sector must be loaded into the device. Any byte that is not loaded during the programming of its sector will be erased to read FFh. The programming operation of the 29C8192 allows 4096 bytes of data to be serially loaded into the device and then simultaneously written into memory during the internally generated program cycle. After the first byte has been loaded, successive bytes of data must be loaded until the full sector of 4096 bytes is loaded. Each new byte to be written must be loaded within 300 µs of the previously loaded byte. The sector address defined by the addresses A0 - A7 is latched by the first $\overline{CE}$ or $\overline{WE}$ falling edge which initiates a program cycle and they stay latched until the completion of the program cycle. Any changes in the sector addresses during the load-program cycle will not affect the initially latched sector address. Addresses A8 - A19 are used to define which bytes will be loaded within the 4096 bytes sector. The bytes may be loaded in any order that is convenient to the user. All the 4096 bytes of the page are serially loaded and are programmed in a single 40 ms program cycle

$\overline{DATA}$ POLLING

The 29C8192 features $\overline{DATA}$ Polling to indicate the completion of a program cycle to the host system. During a program cycle, an attempted read of the last byte loaded into the page will result in the complement of the loaded byte on I/O7, i.e., loaded 0 would be read 1. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may be started. $\overline{DATA}$ Polling may begin at any time during the programming cycle.

DATA INPUT/OUTPUT (I/O0-I/O7)
Data Input/Output pins are used to read data out of the memory or to program Data into the memory.

$\overline{RESET}$
The $\overline{RESET}$ = HIGH puts the device in standard operating mode. The $\overline{RESET}$ = LOW interrupts any interval activity in the device and puts it I/O in high impedance condition. If the $\overline{RESET}$ pin makes a high to low transition during a program cycle, the program operation is interrupted by the $\overline{RESET}$ signal and it will have to be repeated in a new programming cycle after $\overline{RESET}$ pin goes HIGH. After exercising a $\overline{RESET}$ function ($\overline{RESET}$ = LOW) and returning to normal standard operation ($\overline{RESET}$ = HIGH) the device returns to a standby or read mode according to the status of $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ pins.

RDY/$\overline{BUSY}$
The RDY/$\overline{BUSY}$ pin is an open drain output giving the user the opportunity to have a single RDY/$\overline{BUSY}$ by more than one component during a program cycle the RDY/$\overline{BUSY}$ pin is actively pulled low. When the program cycle is finished, the RDY/$\overline{BUSY}$ pin becomes high impedance and can be pulled HIGH by an external resistance connected between the VCC and RDY/$\overline{BUSY}$ pins.

TOGGLE BIT
In addition to $\overline{DATA}$ Polling the 29C8192 provides another method for determining the end of a programming or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

CHIP CLEAR

The content of the entire memory array of the 29C8192 may be altered to HIGH by the use of the CHIP CLEAR operation. By setting $\overline{CE}$ to low, $\overline{OE}$ to 12 Volts, and $\overline{WE}$ to low, the entire memory array can be cleared (written HIGH) within 20 ms. The CHIP CLEAR operation is a latch operation mode. After $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ get the CHIP CLEAR process started, the internal chip timer takes over the CHIP CLEAR operation and $\overline{CE}$, $\overline{OE}$, or $\overline{WE}$ becomes free to be used by the system for other purposes.

HARDWARE DATA PROTECTION

The 29C8192 has three hardware features to protect the written content of the memory against inadvertent programming:

a) Vcc threshold detector - If Vcc is below 1.8 V the program capabilities of the chip is inhibited for whatever input conditions.
b) Noise protection - A $\overline{WE}$, $\overline{OE}$, or $\overline{CE}$ pulse of less than 10 ns in width is not able to initiate a program cycle.
c) Write inhibit - Holding $\overline{OE}$ at low, or $\overline{CE}$ at high, or $\overline{WE}$ at high inhibits the program cycle.

SOFTWARE DATA PROTECTION

The 29C8192 offers a software controlled data program protection feature. The device is delivered to the user with the software data protection DISABLED, i.e., the device will go to the program operation as long as Vcc exceeds 1.8 V and $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ inputs are set at program mode levels. The 29C8192 can be automatically protected against an accidental write operation during power-up or power-down without any external circuitry by enabling the software data protection feature. This feature is enable after the first program cycle which includes the software algorithm. After this operation is done the program function of the device may be performed only if every program cycle is preceded by the software algorithm. The device will maintain its software protect feature for the rest of its life, unless the software algorithm for disabling the protection is implemented.

SOFTWARE ALGORITHM

The 29C8192 has an internal register for the software algorithm which enables the memory to provide the user with additional features:

a) Software Data Protect Enable

A sequence of the three dummy data writes to the memory will activate internal EEPROM fuses during the first page write cycle. These EEPROM fuses will reject any write attempts of new pages of data, unless the three dummy data writes are repeated at the beginning of any page writes.

The timing for the dummy data and addresses must be the same as for a normal program operation. A violation of the three steps program protect sequence in data or address timing and content will abort the procedure and reset the device to the starting point condition.

Note: Software data protect enable procedure must be performed as part of a standard program cycle. If no additional page data is added to the three dummy data writes, the software data protect enable procedure will be aborted. The data protect state will be activated at the end of the program cycle. 4096 bytes of data must be loaded during a Software Data Protection Enable cycle.

Table 1 shows the required procedure for enabling the software data protect:

TABLE 1

STEP	MODE	ADD.A14-A0	DATA I/O 7-0
1	Page Write	5555 Hex	AA Hex
2	Page Write	2AAA Hex	55 Hex
3	Page Write	5555 Hex	A0 Hex
4-131	Page Write	Address	Sector Data (4096 Bytes)

b) Software Data Protect Disable

The software algorithm of 29C8192 includes a six step sequence dummy data programming sequence to disable the software data protect feature described in a). The six step sequence shown in Table 2 must be performed at the beginning of a program cycle. A violation of the six step program sequence in data or address timing and content will abort the procedure and reset the chip to the starting point condition. After a software data protect disable cycle including the six step sequence has been performed, the 29C8192 does not require the use of three dummy loads described in a) for the following program cycle. The device is at the software data protect disabled state.

Note: When six step sequence of software data protect disable procedure is performed, if no additional bytes of data is added after the six-step write sequence, the software data protect disable procedure will be aborted. The data protect state will be deactivated at the end of the program period. 4096 bytes of data must be loaded during a Software Data Protection disable cycle.

Table 2 shows the required procedure for disabling the software data protect:

TABLE 2

STEP	MODE	ADD.A14-A0	DATA I/O 7-0
1	Page Write	5555 Hex	AA Hex
2	Page Write	2AAA Hex	55 Hex
3	Page Write	5555 Hex	80 Hex
4	Page Write	5555 Hex	AA Hex
5	Page Write	2AAA Hex	55 Hex
6	Page Write	5555 Hex	20 Hex
7-134	Page Write	Address	Sector Data (4096 Bytes)

C) Software Chip Clear

The software algorithm of 29C8192 includes a sequence of six step dummy data writing to perform a chip clear operation. Table 3 shows the six step write sequence to perform the software chip clear operation:

TABLE 3

STEP	MODE	ADD.A14-A0	DATA I/O 7-0
1	Page Write	5555 Hex	AA Hex
2	Page Write	2AAA Hex	55 Hex
3	Page Write	5555 Hex	80 Hex
4	Page Write	5555 Hex	AA Hex
5	Page Write	2AAA Hex	55 Hex
6	Page Write	5555 Hex	10 Hex

At the end of the six step program sequence shown in Table 3, the device automatically activates its internal timer to control the chip erase cycle; typically takes 20 msec. After a software chip clear operation has been completed, all 8192K bit locations of memory show high level at read operation mode.

d) Software Autoclear Disable Mode

This software algorithm disables the internal automatic clear before a program cycle. Table 4 shows the six steps needed to perform the autoclear disable mode.

TABLE 4

STEP	MODE	ADD.A14-A0	DATA I/O 7-0
1	Page Write	5555 Hex	AA Hex
2	Page Write	2AAA Hex	55 Hex
3	Page Write	5555 Hex	80 Hex
4	Page Write	5555 Hex	AA Hex
5	Page Write	2AAA Hex	55 Hex
6	Page Write	5555 Hex	40 Hex
7-134	Page Write	Address	Sector Data (4096 Bytes)

Program operation using the software autoclear disable mode will reduce programming time to typically 8 µs per byte. The program cycle using software autoclear disable mode is usually used after a chip clear or a software chip clear operation. At the end of the six step sequence, the autoclear before program is disabled and will stay that way unless a power-down occurs or the software autoclear enable procedure is initiated.

e) Software Autoclear Enable Mode

Automatic page clear before page program can be restored to 29C8192 either by Vcc power-down or by software autoclear enable mode. Table 5 shows the six step page procedure needed to enable software autoclear mode:

TABLE 5

STEP	MODE	ADD.A14-A0	DATA I/O 7-0
1	Page Write	5555 Hex	AA Hex
2	Page Write	2AAA Hex	55 Hex
3	Page Write	5555 Hex	80 Hex
4	Page Write	5555 Hex	AA Hex
5	Page Write	2AAA Hex	55 Hex
6	Page Write	5555 Hex	50 Hex
7-134	Page Write	Address	Sector Data (4096 Bytes)

ABSOLUTE MAXIMUM STRESS RANGES *

TEMPERATURE

Storage: -65° C to 150° C
Under Bias: -55° C to 125° C

ALL INPUT OR OUTPUT VOLTAGES

with respect to Vss +6 V to -0.3 V

* "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature Range:	Commercial:	0° C to 70° C
	Industrial:	-40° C to 85° C
	Military:	-55° C to 125° C
Vcc Supply Voltage:	1.8V to 3.6V	
Endurance:	10,000 Cycles/Byte (Typical)	
Data Retention:	10 Years	

A.C. CHARACTERISTICS - READ OPERATION

Symbol	Parameters	29C8192-1 Min	29C8192-1 Max	29C8192-2 Min	29C8192-2 Max	29C8192-3 Min	29C8192-3 Max	Unit
tacc	Address to Output Delay		250		350		400	ns
tce	$\overline{CE}$ to Output Delay		250		350		400	ns
toe	$\overline{OE}$ to Output		120		130		140	ns
tdf	$\overline{OE}$ to Output In High Z	0	100	0	110	0	120	ns
toh	Output Hold from Address Changes, Chip Enable or Output Enable Whichever Occurs First	0		0		0		ns

D.C. CHARACTERISTICS

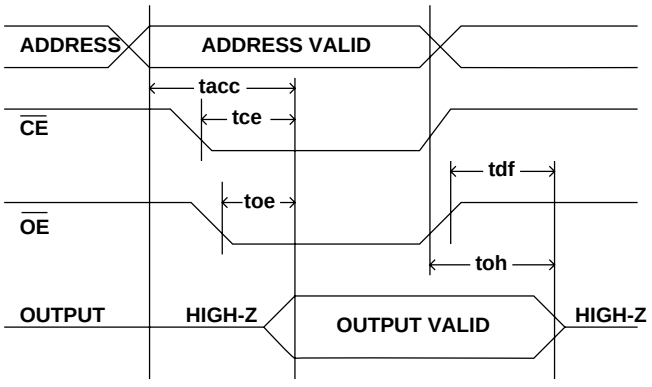
(C) = COMMERCIAL
(I) = INDUSTRIAL
(M) = MILITARY

Symbol	Parameter	Condition	Min	Max	Units
Vcc	Power Supply			1.8 3.6	V
Icc	Active Vcc Current	$\overline{CE}$=$\overline{OE}$=Vil; All I/O Open, Min Read or Write Cycle Time		15 (C) 17 (I) 20 (M)	mA mA mA
Isb1	CMOS Standby Current	CE=Vcc-0.3 V to Vcc+1 V		20 (C) 50 (I&M)	µA µA
Isb2	TTL Standby Current	$\overline{CE}$=Vih, $\overline{OE}$=Vil, All I/O Open, Other Inputs=Vcc Max		1	mA
Iil	Input Leakage Current	Vin=Vcc Max		1	µA
Iol	Output Leakage Current			1	µA
Vil	Input Low Voltage			0.6	V
Vih	Input High Voltage			1.8	V
Vol	Output Low Voltage	Iol=1.6 mA Vcc = 3V		0.45	V
Voh	Output High Voltage	Ioh = -100 uA Vcc = 3V	2.4		V

A.C. TEST CONDITIONS

Output Load : 1 TTL Load and Cl=100 pF
Input Rise and Fall Times : < 10 ns
Input Pulse Level : 0.45 V to 2.4V

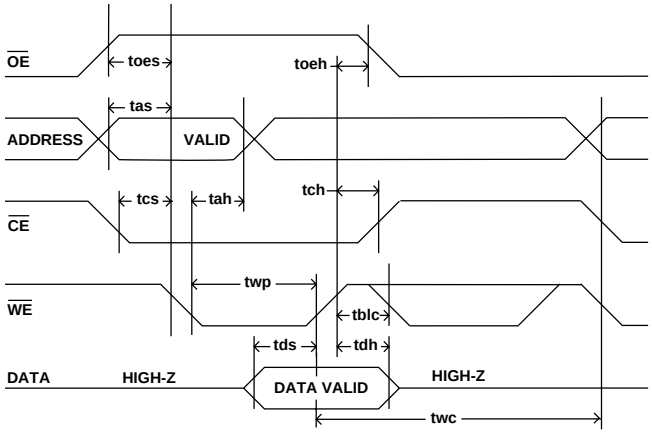
A.C. Read Wave Forms



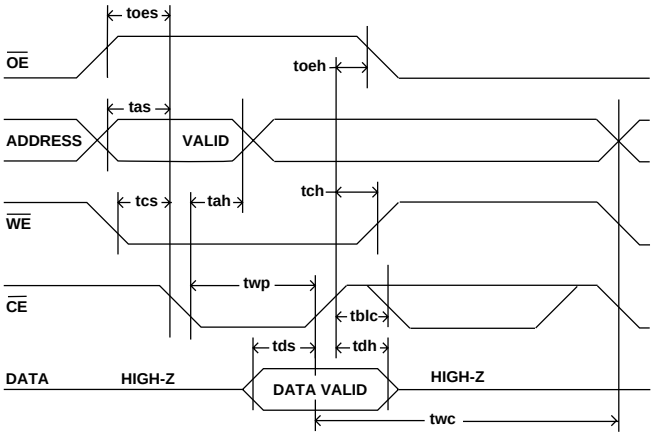
A.C. WRITE CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
tas	Address Set-up Time	20		ns
tah	Address Hold Time	100		ns
tcs	Write Set-up Time	0		ns
tch	Write Hold Time	0		ns
tcw	$\overline{CE}$ Pulse Width	200		ns
twp	$\overline{WE}$ Pulse Width	200		ns
toes	$\overline{OE}$ Set-up Time	20		ns
toeh	$\overline{OE}$ Hold Time	20		ns
tds	Data Set-up Time	100		ns
tdh	Data Hold Time	10		ns
tblc	Byte Load Cycle	0.2	300	µs
tlp	Last Byte Loaded to Data Polling Output		500	µs
twc	Write Cycle Time		40	ms

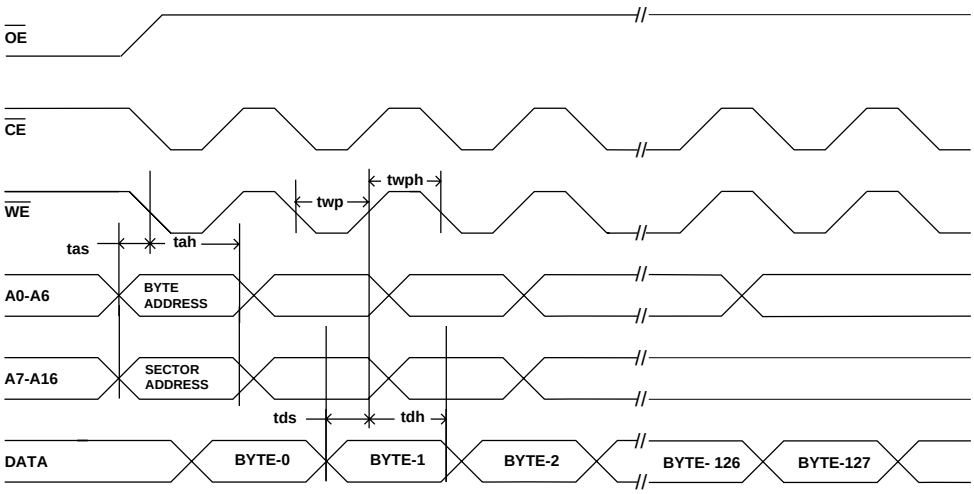
A.C. Write Wave Forms $\overline{WE}$-Controlled



A.C. Write Wave Forms $\overline{CE}$-Controlled



Sector Mode Write Wave Forms (1,2,3)



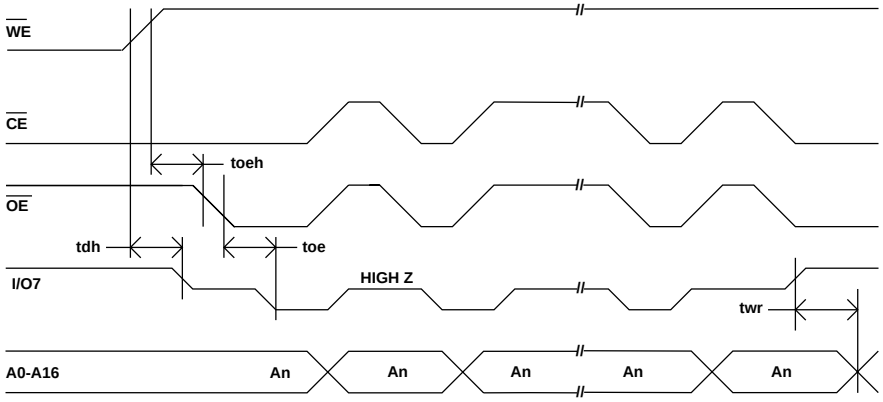
Note: 1. Addresses A0 to A7 define the 256 sectors and are latched by the first high to low transition of $\overline{WE}$ or $\overline{CE}$ of the first loading cycle.
2. $\overline{OE}$ must be high when $\overline{WE}$ and $\overline{CE}$ are both low.
3. All bytes that are not loaded within the sector being programmed will be erased to FF.

$\overline{\text{DATA}}$ Polling Characteristics

Symbol	Parameter	Min	Max	Unit
tdh	Data Hold Time	10		ns
toeh	$\overline{\text{OE}}$ Hold Time	10		ns
toe	$\overline{\text{OE}}$ to Output Delay (1)			ns
twr	Write Recovery Time	0		ns

Note: 1. See toe Specification in AC Characteristics - Read Operation

$\overline{\text{DATA}}$ Polling Wave Forms

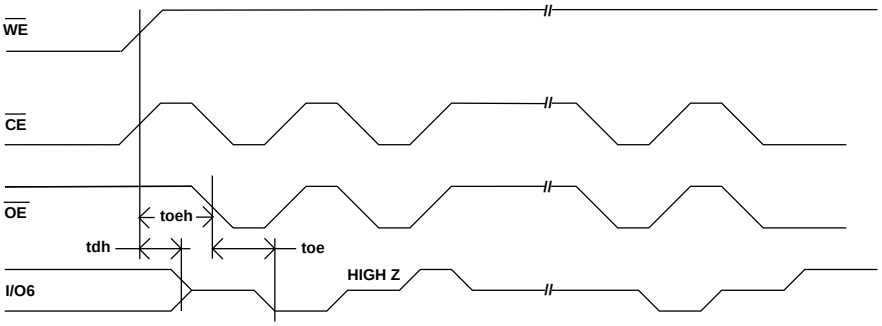


Toggle Bit Characteristics

Symbol	Parameter	Min	Max	Unit
tdh	Data Hold Time	10		ns
toeh	$\overline{\text{OE}}$ Hold Time	10		ns
toe	$\overline{\text{OE}}$ to Output Delay (1)			ns
toeh	OE High Pulse	150		ns

Note: 1. See toe Specification in AC Characteristics - Read Operation

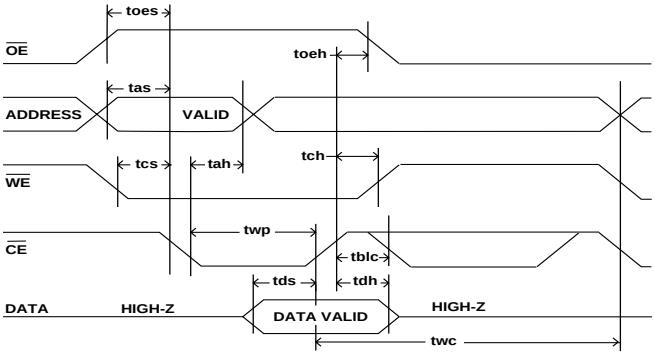
Toggle Bit Wave Forms (1,2,3)



Note:
1. Toggling either $\overline{\text{OE}}$ or $\overline{\text{CE}}$ or both will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Chip Clear Wave Form

The content of the 29C8192 may be altered to HIGH by the use of the Chip Clear operation. By setting $\overline{CE}$ to low, $\overline{OE}$ to 12 volts, and $\overline{WE}$ to low, the entire memory can be cleared (written HIGH) within 20 ms. The Chip Clear operation is a latch operation mode. After the Chip Clear starts, the internal chip timer takes over and completes the clear without $\overline{CE}$, $\overline{OE}$ and $\overline{WE}$ being held active.



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