T R I Q U I N T   *S E M I C O N D U C T O R , I N C .*

TQS

TQ6124

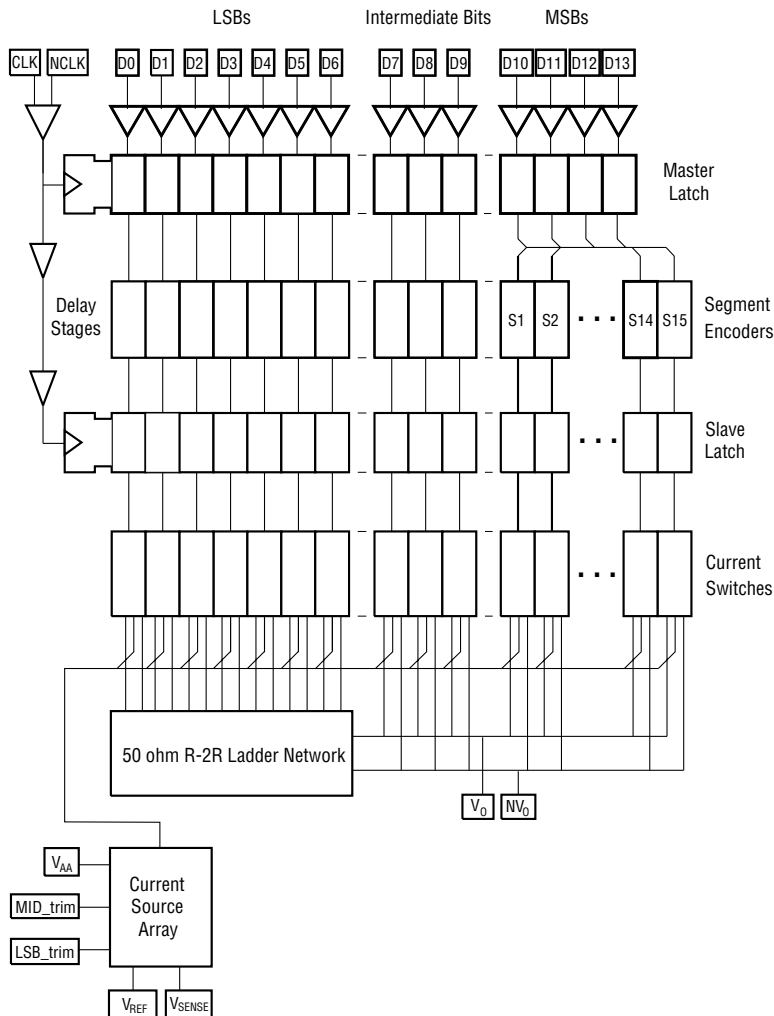## 1 Gigasample/sec, 14-bit Digital-to-Analog Convertor

The TQ6124 is a 14-bit monolithic digital-to-analog converter. The TQ6124 achieves conversion accuracy by using a segmented architecture, precision current sources, and on-chip nichrome resistors. The only external components required are an external reference and loop control amplifier.

The TQ6124 is ideally suited for applications in direct digital synthesis, pixel generation for high-resolution monitors, broadband video generation, and high-speed arbitrary waveform generators.

Figure 1. TQ6124 Block Diagram

Features

- 1Gs/s aggregate bandwidth
- 14-bit resolution
- RF front end
- ECL-compatible inputs
- 0.026% DC differential non-linearity
- 0.035% DC integral non-linearity
- SFDR: 52 dBc @ F_{OUT} = 75 MHz
  48 dBc @ F_{OUT} = 148 MHz
  45 dBc @ F_{OUT} = 199 MHz
- 1.4 W power dissipation
- 44-pin ceramic QFP package or die only

Applications

- Direct Digital Synthesis
- Pixel generation for workstations and high-end monitors
- Direct-generation of broadband video for cable TV
- High-speed arbitrary waveform generators

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Functional Description

The TQ6124 registers incoming bits in a master latch array. The value of the four most-significant bits is encoded into an n-of-15 thermometer code while the ten low-order bits pass though an equalizing delay stage. All 25 bits are re-registered in a 25-wide slave latch array which drives a set of 25 differential pair switches. These switches steer the corresponding segment and bit currents into the true (V_0) and complementary (NV_0) outputs. This architecture minimizes glitch impulses by eliminating large mid-scale current transitions.

The most-significant bits generate the segment currents, which are of equal weight at $^1/_{16}$ of the full-scale output (I_{FS}). The ten lower-order bits are divided into two subgroups. The three intermediate bits steer binary-weighted currents of magnitude $I_{FS}/32$, $I_{FS}/64$ and $I_{FS}/128$ to the outputs. The seven least-significant bits steer identical $I_{FS}/128$ currents into a differential R-2R ladder to generate effective bit currents of $I_{FS}/256$ to $I_{FS}/16384$. The DAC output is the sum of the outputs of the segments and the low-order bits.

Clock and data inputs are ECL-compatible. The outputs are designed to operate into a 50Ω load, with internal reverse termination to ground being provided by the R-2R network.

External compensation is utilized to minimize the effects of device mismatch. An external op amp senses the sum of the segment, the intermediate bit, and the LSB currents.

Figure 2. TQ6124 Currents

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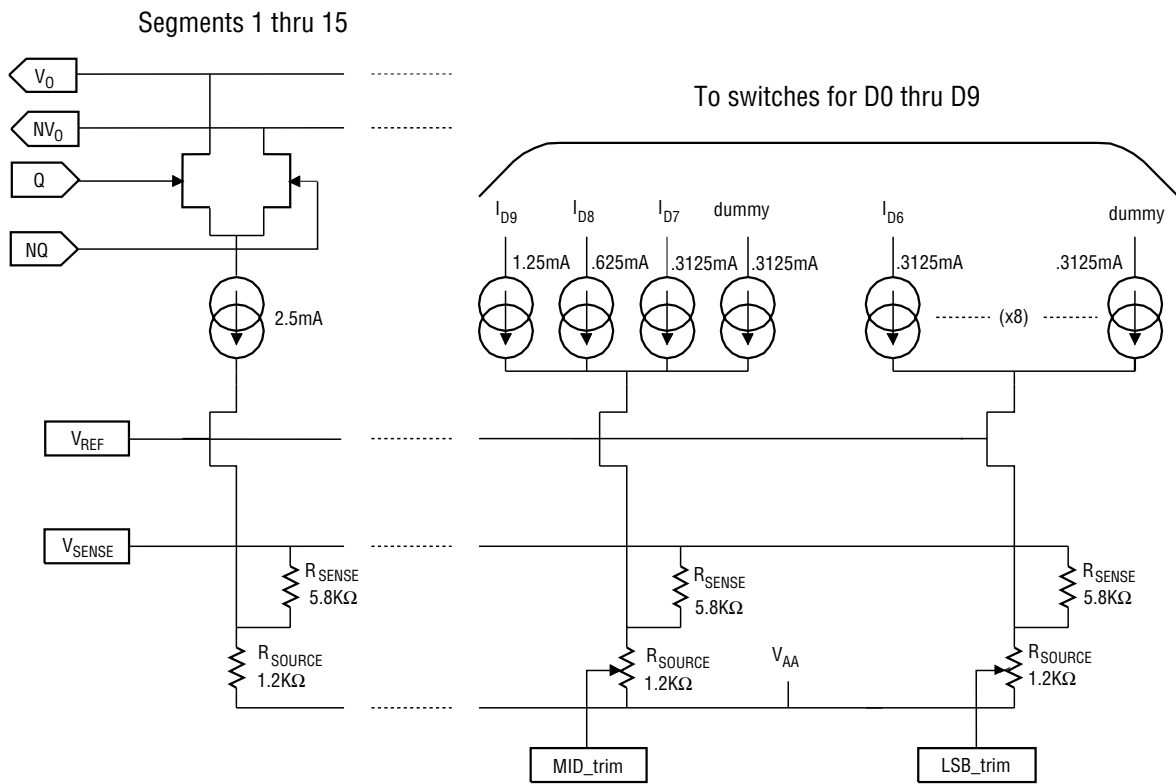
Electrical Specifications

Table 1. Recommended Operating Conditions

Symbol	Parameter	Min.	Nom.	Max.	Unit
V_{SS}	Negative Power Supply	−5.25	−5.0	−4.75	V
V_{AA}	Analog Power Supply	−15.5	−12	−11.5	V
T_C	Case Temperature	−20		85	°C

Table 2. DC Operating Characteristics

Unless otherwise specified, measured over Recommended Operating Conditions with balanced 50Ω loads, V_{FS} = 1.0 V.

Symbol	Parameter	Condition	Min.	Nom.	Max.	Unit
I_{AA}	V_{AA} Supply Current			−75	−90	mA
I_{SS}	V_{SS} Supply Current			−285	−450	mA
V_{REF}	Reference Voltage		V_{AA} + 2.5	V_{AA} + 3.0	V_{AA} + 3.75	V
I_{REF}	Reference input current		−25		25	mA
V_{IH}	ECL Input High Voltage	V_{EREF} = −1.3 V	−1.1		−0.6	V
V_{IL}	ECL Input Low Voltage	V_{EREF} = −1.3 V	−2.5		−1.5	V
I_I	ECL Input Current		−25		25	mA
V_{EREF}	ECL Reference Voltage	V_{SS} = −5.0 V		−1.34		V
R_{EREF}	ECL Reference Resistance			400		ohms
DNL	Differential non-linearity	(Note 2)	−0.05	0.026	0.05	%F.S.
INL	Integral non-linearity	(Note 2)	−0.05	0.035	0.05	%F.S.
	Full-scale symmetry	(Note 1)	−8	2	8	mV
V_{FS}	Full-scale output voltage	R_L = 50 ohms		−1.0	−1.125	V
R_{OUT}	V_O, NV_O, output resistance		44	50.9	57	ohms
	R_{OUT} Matching		−2.5	0.15	2.5	%
V_O, NV_O	Output Voltage		−1.125		0	V
V_{ZS}	Zero Scale Voltage		−50	−40	0	mV
V_{SENSE}	Sense output voltage		V_{AA} + 2.5		V_{AA} + 3.75	V
θ_{JC}	Thermal Impedance			15		°C/W

Notes: 1. Full-scale symmetry is a measure of the balance between V_O and NV_O. For a full-scale output transition, the change in V_O will match the change in NV_O to within the specified amount. Any imbalance in the output loads will affect symmetry.

2. Linearity can interpreted as 10 bits at $1/2$ LSB or as 11 bits at 1 LSB. The device is monotonic to 10 bits. Linearity is tested with the Mid_trim set for optimal DNL, with the LSB_trim pin open.

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Table 3. AC Operating Characteristics

Unless otherwise noted, measured over DC operating characteristics with balanced 50Ω loads,
V_{FS} = 0.8V, V_{IN} = 0.8V_{P-P}, input rise and fall times ≤ 300 ps.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{CLK}	Clock Frequency		50		1000	MHz
t_R, t_F	At full scale	10% to 90%			350	ps
t_{DS}	Data Setup Time		200			ps
t_{DH}	Data Hold Time		300			ps
t_{CLKHI}	Clock High Time		400			ps
t_{CLKLO}	Clock Low Time		400			ps
SFDR*	Spurious free dynamic range	F_{OUT} = 75 MHz	45	52		dBc
		F_{OUT} = 148 MHz	45	52		dBc
		F_{OUT} = 199 MHz	45	49		dBc

Note: SFDR testing performed at F_{CLK} = 600 MHz only.

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{SS}	Digital Supply	−7.0		V
V_{AA}	Analog Supply	−16.0		V
V_O, NV_O	Analog Output Voltage	−2.0	2.0	V
V_I	Digital Input Voltage	V_{SS} − 0.5	+0.5	V
I_I	Digital Input Current	−1.0	+1.0	mA
V_{REF}	Reference Voltage	V_{AA}-2	0	V
I_{REF}	Reference Current	−1	1	mA
	Power Dissipation		5	W
T_{STG}	Storage Temperature	−65	150	°C
T_J	Operating Junction Temperature		150	°C

Note: Absolute Maximum Ratings are those beyond which the integrity of the device cannot be guaranteed.
If the device is subjected to the limits in the absolute maximum ratings, its reliability may be impaired.
The Electrical Specifications tables provide conditions for actual device operation.

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AC Timing

The low-going transition of CLK latches the data. Production SFDR testing is performed with the clock transitioning in the center of the data eye. The timing of the clock transition with respect to the data can improve SFDR performance. Systems working to optimize SFDR can 'tune' this phase relationship to optimize the desired characteristic.

Figure 3. AC Timing Relationships
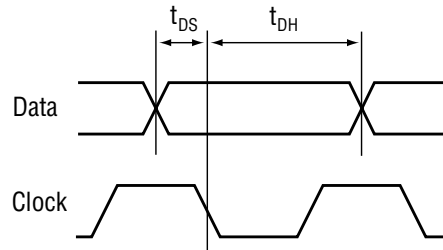
Operating Notes

Current Source Control Loop

The full scale output voltage is set through the use of an external op amp, as shown in Figure 4. Nominal full scale output voltage can be achieved by using a voltage source. With this, control voltages on the op amp of around $V_{AA}+3V$ can be set. Adjusting the full scale output voltage can be achieved by toggling the inputs over full scale while adjusting the control voltage to achieve the desired level.
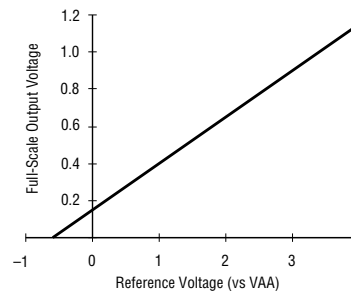
Figure 4. Adjusting the Full-Scale Output Voltage
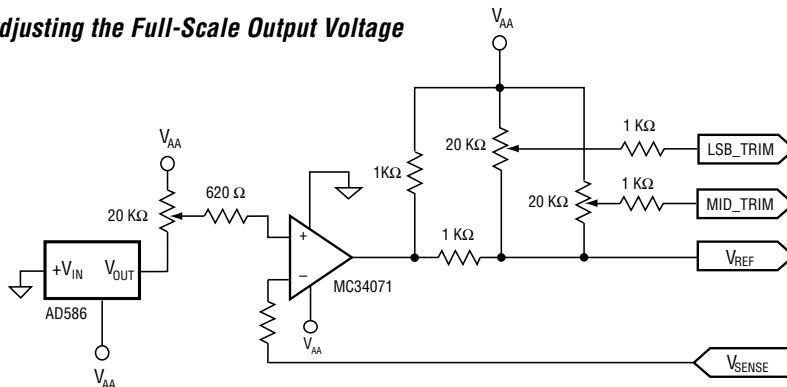
V_{REF} Adjustment Range

The output full scale voltage range can be set through the V_{REF} input. Figure 5 shows the approximate relationship between V_{REF} and V_{FS}.

Figure 5. Full-Scale Output Voltage vs. V_{REF}

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Operating Notes (continued)

Power Supplies

Optimized performance depends on clean supplies. Utilize very low impedance negative supplies that are decoupled over a wide frequency range. The analog and digital grounds should be isolated at the chip, connecting to a single point ground on the circuit board.

ECL Reference

The single-ended data inputs switch against an internal reference of -1.3V (nominal). Variations among input buffers, or in V_{TT}, may benefit from adjustments in the reference. The ECL reference pin may be driven externally. Its equivalent load is 400 ohms to –1.3V (nominal).

Trim Adjustments

The external trim adjustments for the midrange bits and the LSBs is optional. Trimming is performed by monitoring the attribute of greatest concern (INL, DNL, Spurious levels) while minimizing the unwanted effects. Trim inputs should be left open if not used.
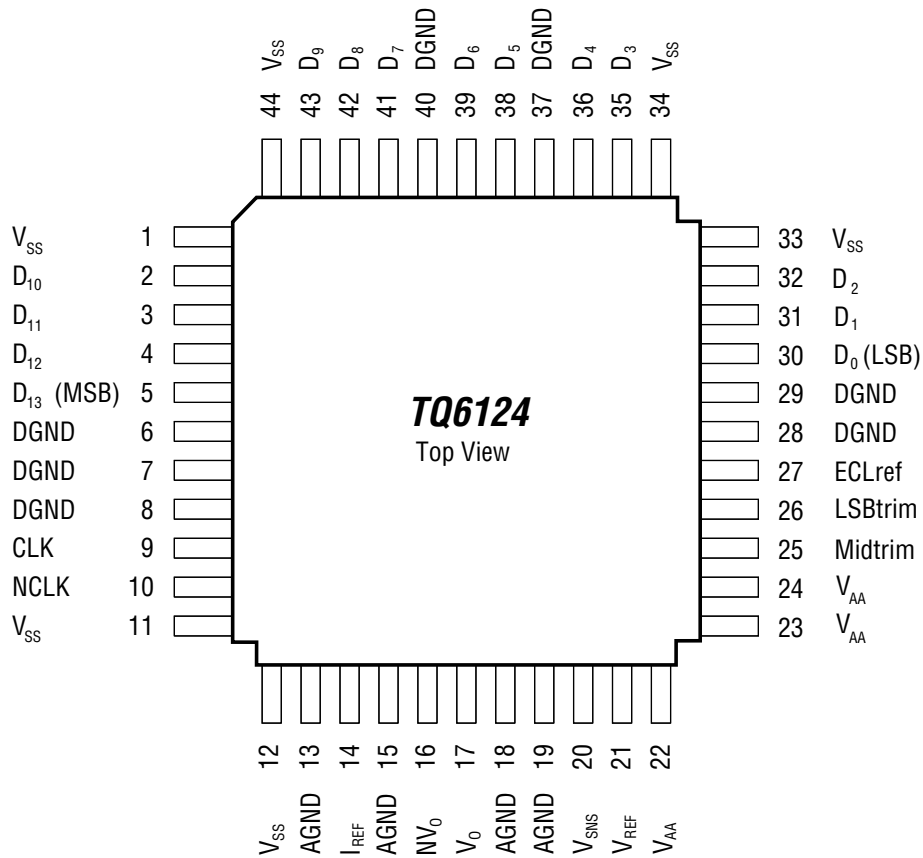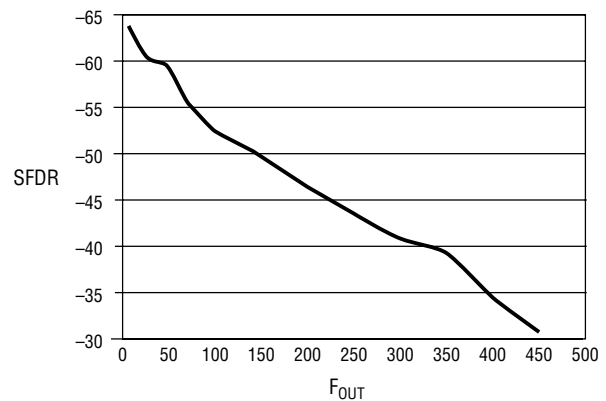
Signals

Figure 6. TQ6124 Pinout

*For additional information and latest specifications, see our website: **www.triquint.com***

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Table 5. Signal-Pin Descriptions

Signal	Pin(s)	Description
DGND	6, 7, 8, 28, 29, 37, 40	Ground connection for digital circuitry.
AGND	13, 15, 18, 19	Ground connection for analog circuitry.
D_0 thru D_{13}	30, 31, 32, 35, 36, 38, 39, 41, 42, 43, 2, 3, 4, 5	Data inputs. D_0 is the least significant bit. ECL levels.
V_0, NV_0	17, 16	True and complementary analog outputs.
CLK, NCLK	9, 10	True and complementary clock inputs. ECL levels.
I_{REF}	14	Connect to AGND. Source of dummy currents in the switch array.
V_{SENSE}	20	Sense Output.
V_{REF}	21	Reference Input.
V_{SS}	1, 11, 12, 33, 34, 44	Digital negative power supply.
V_{AA}	22, 23, 24	Analog negative power supply.
Mid_trim	25	Trim terminal for mid range bits.
LSB_trim	26	Trim terminal for LSB range bits.
ECLref	27	Optional ECL reference level adjustment. Thevinin equivalent is 1.3V nominally into 400 ohms. Equivalent voltage tracks with digital supply.

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Typical Performance Data

The graph in Figure 7 shows representative performance data of spurious free dynamic range (SFDR) vs. output frequency performance measured from TQ6124 devices.

Data was collected at room temperature; note, however, that SFDR is not strongly dependendent on temperature. Optimum performance is obtained by utilizing as high a clock rate as practical.
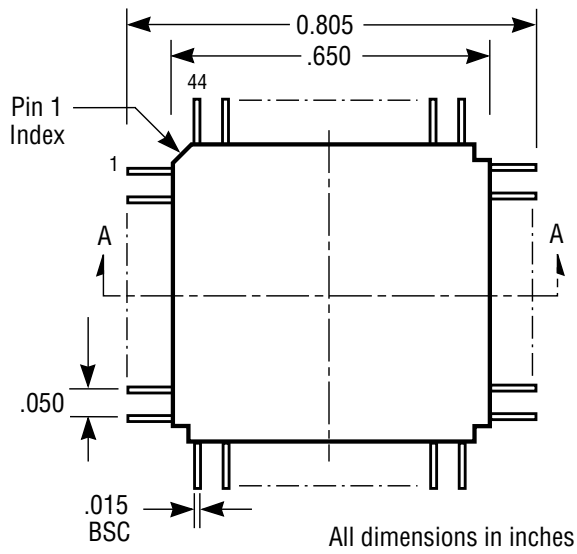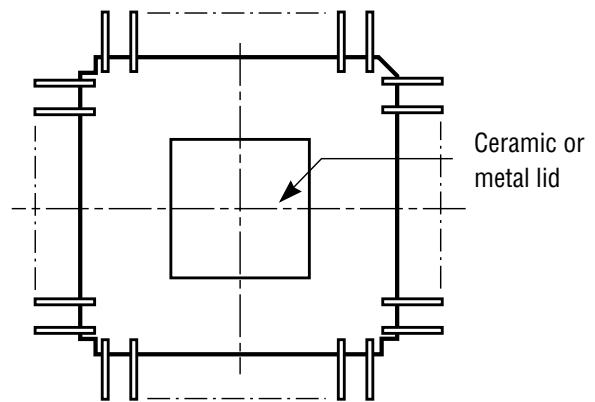
Figure 7. SFDR vs. Output Frequency

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Packaging

Figure 8. 44-pin QFP Package Dimensions

Top View

BottomView

0.805

.650

44

Pin 1
Index

1

A

A

.050

.015
BSC

All dimensions in inches

Ceramic or
metal lid

Section A-A

Device

.125

Seating plane

.035 typ.

.065

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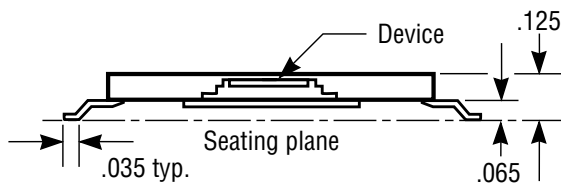
Ordering Information

TQ6124-CM   *1 GS/s 14-bit DAC in 44-pin ceramic QFP*
TQ6124-CD   *1 GS/s 14-bit DAC — die only*
ETF6124   *Engineering Test Fixture with TQ6124 device*

Additional Information

For latest specifications, additional product information,
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Web: www.triquint.com   **Tel: (503) 615-9000**
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