

The TQ8015 is a non-blocking 16 x 16 digital crosspoint switch capable of data rates greater than 1.25 Gigabits per second per port. Utilizing a fully differential internal data path and ECL I/O, the TQ8015 offers a high data rate with exceptional signal fidelity. The symmetrical switching and noise rejection characteristics inherent in differential logic result in low jitter and signal skew. The TQ8015 is ideally suited for digital video, data communications and telecommunication switching applications.

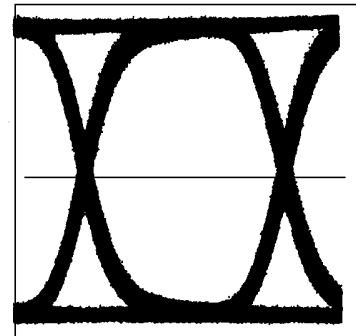
The non-blocking architecture uses 16 fully independent 16:1 multiplexers (see diagram on page 2), allowing each output port to be independently programmed to any input port. The switch is configured by sequentially loading each multiplexer's 4-bit program latch (OA0:3) with the desired input port address (IA0:3) and enabling the LOAD pin. When complete, the CONFIGURE pin is strobed and all new configurations are simultaneously transferred into the switch multiplexers. Data integrity is maintained on all unchanged data paths.

Electrical Characteristics

| | Min | Max | Units |
|---------------------------------|------|------|--------------|
| Data Rate/Port | 1.25 | | Gb/s |
| Jitter | | 150 | ps peak-peak |
| Channel Propagation Delay | | 2000 | ps |
| Ch-to-Ch Propagation Delay Skew | | 500 | ps |

TQ8015

**1.25 Gigabit/sec
16x16 Digital ECL
Crosspoint Switch**



Typical output waveform with all channels driven

Features

- >20 Gb/s aggregate BW
- 1.25 Gb/s/port NRZ data rate
- Non-blocking architecture
- 500 ps delay match
- Differential ECL-level data I/O; CMOS-level control inputs
- Low jitter and signal skew
- Fully differential data path
- Double buffered configuration latches
- 132-pin MQFP package

Applications

- Telecom/Datacom Switching*
- Hubs and Routers*
- Video Switching*

SWITCHING PRODUCTS

TQ8015

Figure 1. TQ8015 architecture.

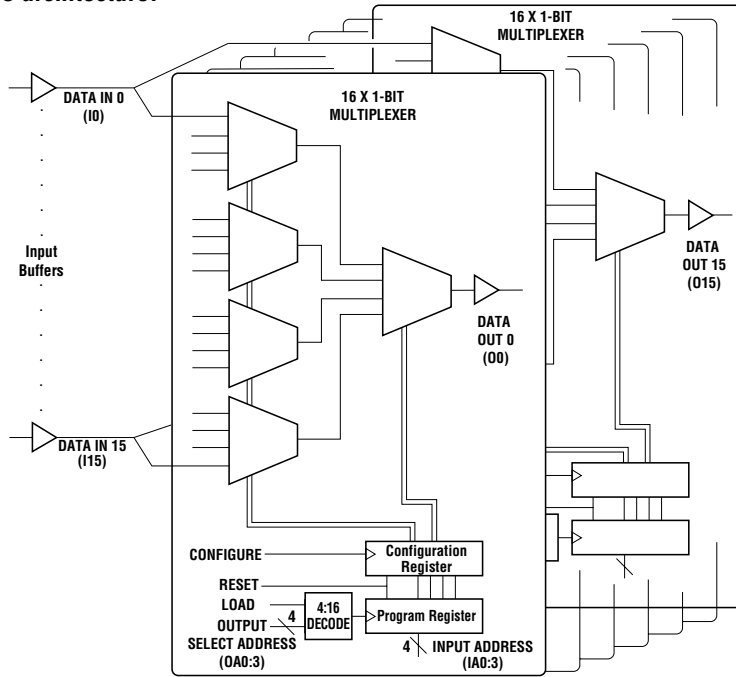


Table 1. Absolute Maximum Ratings⁵

| Symbol | Parameter | Absolute Max. Rating | Notes |
|-------------------|--|----------------------------------|-------|
| T _{STOR} | Storage Temperature | -65° C to +150° C | |
| T _{CH} | Junction (Channel) Temperature | -65° C to +150° C | 1 |
| T _C | Case Temperature Under Bias | -65° C to +125° C | 2 |
| V _{CC} | Supply Voltage | 0 V to +7 V | 3 |
| V _{EE} | Supply Voltage | -7 V to 0 V | 3 |
| V _{TT} | Load Termination Supply Voltage | V _{EE} to 0 V | 4 |
| V _{IN} | Voltage Applied to Any ECL Input; Continuous | V _{EE} -0.5 V to +0.5 V | |
| I _{IN} | Current Into Any ECL Input; Continuous | -1.0 mA to +1.0 mA | |
| V _{IN} | Voltage Applied to Any CMOS Input; Continuous | -0.5 V to V _{CC} +0.5 V | |
| I _{IN} | Current Into Any CMOS Input; Continuous | -1.0 mA to +1.0 mA | |
| V _{OUT} | Voltage Applied to Any ECL Output | V _{EE} -0.5 V to +0.5 V | 4 |
| I _{OUT} | Current From Any ECL Output; Continuous | -40 mA | |
| P _D | Power Dissipation per Output P _{OUT} = (GND - V _{OUT}) x I _{OUT} | 50 mW | |

- Notes:
1. For die applications.
 2. T_C is measured at case top.
 3. All voltages specified with respect to GND, defined as 0V.
 4. Subject to I_{OUT} and power dissipation limitations.
 5. Absolute maximum ratings, as detailed in this table, are the ratings beyond which the device's performance may be impaired and/or permanent damage to the device may occur.

Table 2. Recommended Operating Conditions³

| Symbol | Parameter | Min | Typ | Max | Units | Notes |
|---------------|-------------------------------------|------|------|------|----------|-------|
| T_C | Case Operating Temperature | 0 | | 85 | °C | 1 |
| V_{CC} | Supply Voltage | 4.5 | | 5.5 | V | |
| V_{EE} | Supply Voltage | -5.5 | | -4.5 | V | |
| V_{TT} | Load Termination Supply Voltage | | -2.0 | | V | 2 |
| R_{LOAD} | Output Termination Load Resistance | | 50 | | Ω | 2 |
| Θ_{JC} | Thermal Resistance Junction to Case | | | 7 | °C/W | |

Notes: 1. T_C measured at case top. Use of adequate heatsink is required.
 2. The V_{TT} and R_{LOAD} combination is subject to maximum output current and power restrictions.
 3. Functionality and/or adherence to electrical specifications is not implied when the device is subjected to conditions that exceed, singularly or in combination, the operating range specified.

Table 3. Pin Descriptions

| Signal | Name/Level | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------------|--|---|-----|-------------|-----|-----|-------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|
| I0 to I15, NI0 to NI15 | Data input true and complement. Differential ECL | Differential data input ports. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| O0 to O15, NO0 to NO15 | Data output true and complement. Differential ECL | Differential data output ports. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| IA0:3 | Input address, CMOS | Input port selection address that is written into the selected output port program latches (OA0:3). <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>IA3</th> <th>IA2</th> <th>IA1</th> <th>IA0</th> <th>Input port</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>2</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>15</td> </tr> </tbody> </table> | IA3 | IA2 | IA1 | IA0 | Input port | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 2 | : | : | : | : | : | 1 | 1 | 1 | 1 | 15 |
| IA3 | IA2 | IA1 | IA0 | Input port | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 0 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| : | : | : | : | : | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | 15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| OA0:3 | Output select address, CMOS | Output port selection address. Selects the output port program latches to which the input port selection address (IA0:3) is written. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>OA3</th> <th>OA2</th> <th>OA1</th> <th>OA0</th> <th>Output port</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>2</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>15</td> </tr> </tbody> </table> | OA3 | OA2 | OA1 | OA0 | Output port | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 2 | : | : | : | : | : | 1 | 1 | 1 | 1 | 15 |
| OA3 | OA2 | OA1 | OA0 | Output port | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 1 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 0 | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| : | : | : | : | : | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 1 | 15 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| LOAD | CMOS | Enables the selected output port program latches while set 'high'. Latches the data when set to a 'low' level. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CONFIGURE | CMOS | Transfers the program latches data to the configuration latches and implements the switch changes while set 'high'. Latches the data when set to a 'low' level. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RESET | CMOS | Sets the switch into broadcast or pass-through configuration, overwriting existing configurations. Broadcast mode: All output ports are connected to data input port 0. This mode is selected by applying a RESET "high" pulse with CONFIGURE held "low". | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

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Table 4. DC Characteristics¹ – Within recommended operating conditions, unless otherwise indicated.

| Symbol | Parameter | Min | Max | Units | Test Cond. | Notes |
|-------------------|--|-----------------|-----------------|-------|-----------------------------------|-------|
| V _{IH} | ECL Input Voltage High | -1100 | -500 | mV | | |
| V _{IL} | ECL Input Voltage Low | V _{TT} | -1500 | mV | | |
| I _{IH} | ECL Input Current High | | +30 | μA | V _{IH} = -0.7 V | |
| I _{IL} | ECL Input Current Low | -30 | | μA | V _{IL} = -2.0 V | |
| V _{ICM} | ECL Input Common Mode Voltage | -1500 | -1100 | mV | | |
| V _{IDIF} | ECL Input Differential Voltage (pk-pk) | 400 | 1200 | mV | | |
| V _{IH} | CMOS Input Voltage High | 3.5 | V _{CC} | V | | |
| V _{IL} | CMOS Input Voltage Low | 0 | 1.5 | V | | |
| I _{IH} | CMOS Input Current High | | +100 | μA | V _{IH} = V _{CC} | |
| I _{IL} | CMOS Input Current Low | | -100 | μA | V _{IL} = 0 V | |
| V _{OCM} | ECL Output Common Mode | -1500 | -1100 | mV | | |
| V _{ODIF} | ECL Output Differential Voltage | 600 | | mV | | |
| V _{OH} | ECL Output Voltage High | -1000 | -600 | mV | | |
| V _{OL} | ECL Output Voltage Low | V _{TT} | -1600 | mV | | |
| I _{OH} | ECL Output Current High | 20 | 27 | mA | | |
| I _{OL} | ECL Output Current Low | 0 | 8 | mA | | |
| I _{CC} | Power Supply Current (+) | | 20 | mA | | |
| I _{EE} | Power Supply Current (-) | | -950 | mA | | |

Notes: 1. Test conditions unless otherwise indicated: V_{TT} = -2.0 V, R_{LOAD} = 50 W to V_{TT}.

Table 5. AC Characteristics¹ – Within recommended operating conditions, unless otherwise indicated.

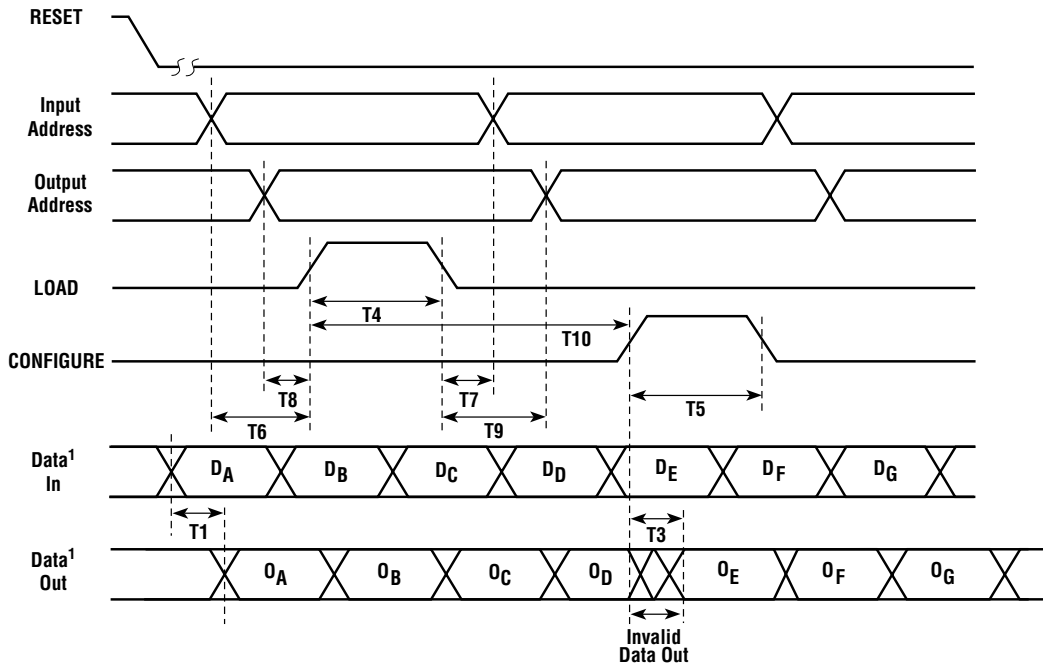
| Symbol | Parameter | Min | Typ | Max | Units | Notes |
|------------------|--|-----|-----|------|----------|-------|
| | Maximum Data Rate/Port | | | 1.25 | Gb/s | 1,2 |
| | Jitter | | | 150 | ps pk-pk | 1 |
| T ₁ | Channel Propagation Delay | | | 2000 | ps | |
| T ₂ | Ch-to-Ch Propagation Delay Skew | | | 500 | ps | |
| T ₃ | CONFIG to Data Out (O _i) Delay | | | 5 | ns | |
| T ₄ | LOAD Pulse Width | 7 | | | ns | |
| T ₅ | CONFIG Pulse Width | 7 | | | ns | |
| T ₆ | IA _i to LOAD High Setup Time | 0 | | | ns | |
| T ₇ | LOAD to IA _i Low Hold Time | 3 | | | ns | |
| T ₈ | OAI to LOAD High Setup Time | 0 | | | ns | |
| T ₉ | LOAD to OAI Low Hold Time | 3 | | | ns | |
| T ₁₀ | Load ↑ to CONFIG ↑ | 0 | | | ns | |
| T ₁₁ | RESET Pulse Width | 10 | | | ns | |
| T _{R,F} | Output Rise or Fall Time | | 250 | 400 | ps | 3 |

Notes: 1. Test conditions: V_{TT} = -2.0 V, R_{LOAD} = 50 W to V_{TT}; ECL inputs: V_{IH} = -1.1 V; V_{IL} = -1.5 V; CMOS inputs: V_{IH} = 3.5 V, V_{IL} = 1.5 V; ECL outputs: V_{OH} ≥ -1.0 V, V_{OL} ≤ -1.6 V; ECL inputs rise and fall times ≤ 1 ns; CMOS inputs rise and fall times ≤ 20 ns. A bit error rate of 1E-13 BER or better for 2²³-1PRBS pattern, jitter and rise/fall times are guaranteed through characterization.

2. 1.2 Gb/s Non-Return-Zero (NRZ) data equivalent to 600 MHz clock signal.

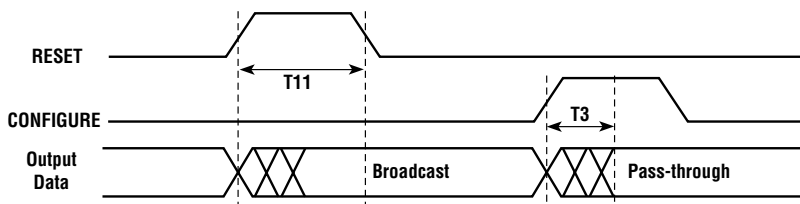
3. Rise and fall times are measured at the 20% and 80% points of the transition from V_{OL} max to V_{OL} min.

Figure 2. Switch Configuration Timing



Notes: 1. No data loss on unchanged paths.

Figure 5. Reset Timing



Notes: 1. LOAD input must remain LOW to insure correct programming of the switch.
 2. "Broadcast" is defined as data input 0 to all data outputs (0...15).
 3. "Pass-through" is defined as data input 0 to data output 0, data input 1 to data output 1, and so on.

Typical Performance Data

Figure 4. Data Eye Closure

Percent RMS vs. Data Rate (typical)

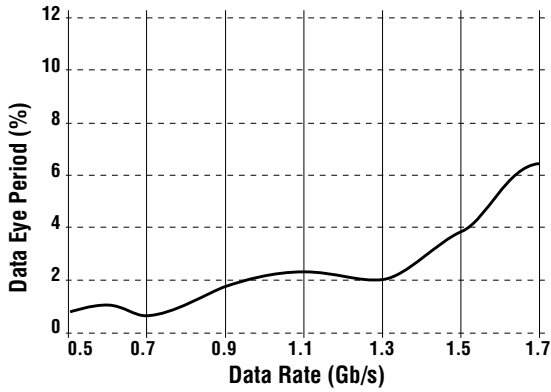


Figure 5. Data Eye Closure

Time & Amplitude vs. Data Rate (typical)

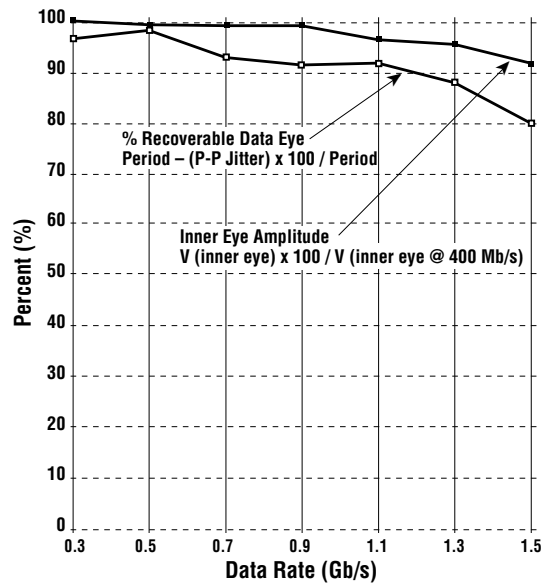


Figure 6. RMS Jitter vs. Data Rate (typical)

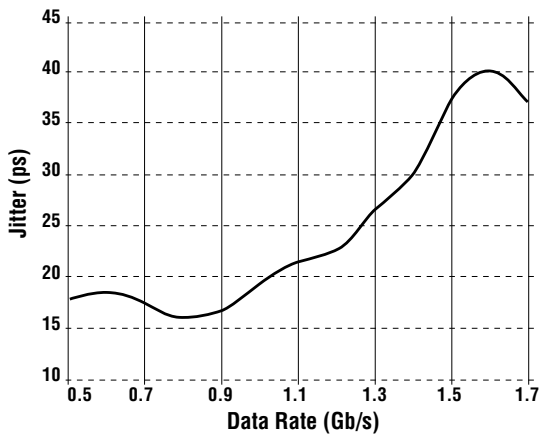
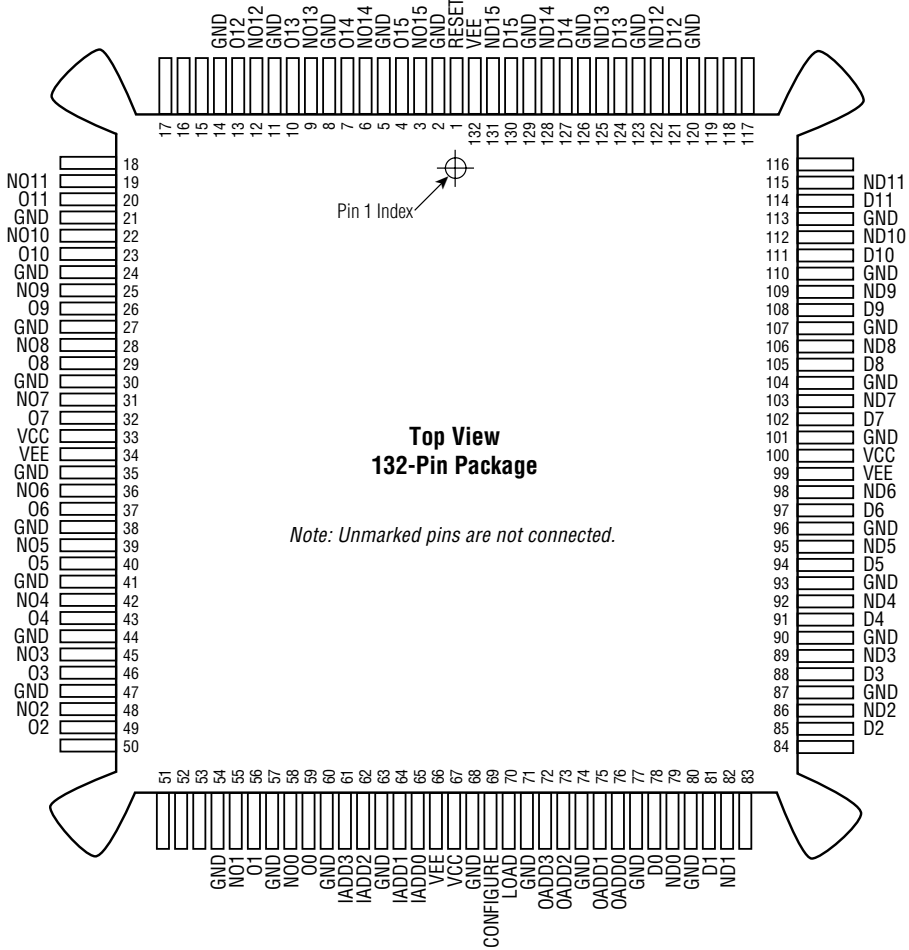


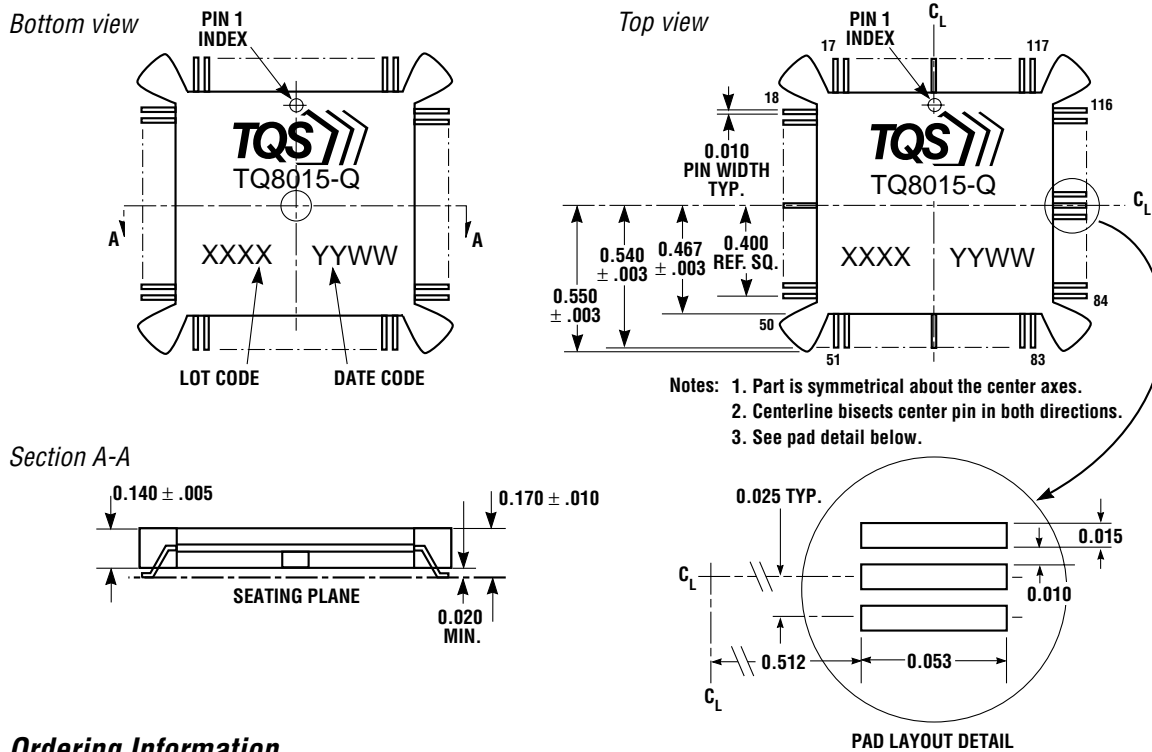
Figure 7. Package Pinout



SWITCHING PRODUCTS

TQ8015

Figure 8. Mechanical Dimensions (in inches)



Ordering Information

TQ8015-Q 1.25 16x16 Gb/s ECL Crosspoint Switch

Additional Information

For latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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