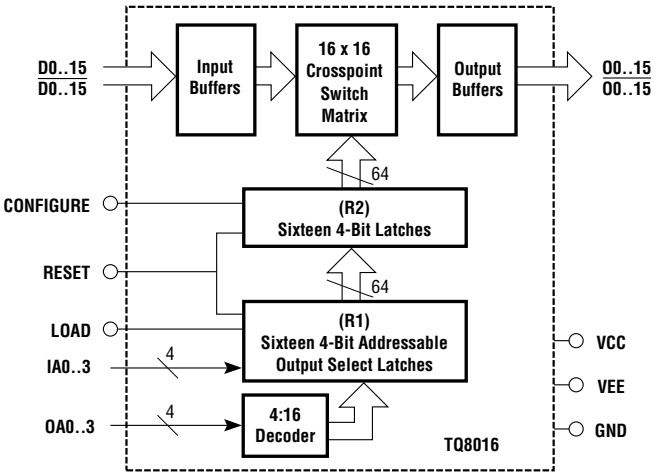
TQ8016

1.3 Gigabit/sec 16x16 Digital ECL Crosspoint Switch

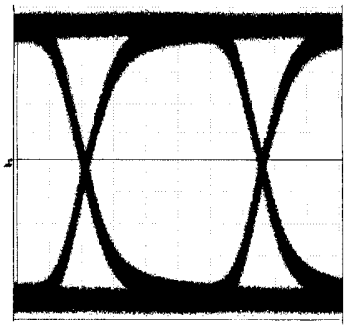


The TQ8016 is a 16 x 16 differential digital crosspoint switch capable of handling 1.3 Gbit/s data rate. The high data rate and exceptional signal fidelity is made possible with TriQuint's fully differential Source-Coupled FET Logic (SCFL) standard cells. The symmetrical switching characteristic inherent in differential logic results in low signal skew and crosstalk for maximum signal fidelity.

The user can independently configure any switch output to any input, including an input chosen by another output. To configure the switch, the 4-bit output address (OA0..3) is decoded to enable the loading of the 4-bit input selection data (IA0..3) on the rising edge of the LOAD signal. The process is repeated until all desired connections are programmed. By bringing the CONFIGURE signal high, the contents of the Output Select Latches are transferred in parallel to a second row of 4-bit latches (R2), causing the switch reconfiguration.

This double row architecture minimizes the time to completely reconfigure the switch since a new set of addresses can be loaded to the Output Select Latches (R1) while the switch is active (transmitting). At the time of reconfiguration, no data drop-out occurs for any output whose input connection does not change.

For applications which do not require synchronous configuration of the switch, the LOAD and CONFIGURE inputs may be tied together.



Typical output waveform with all channels driven

Features

- *>1.3 Gigabit/sec data rate*
- *Non-blocking architecture*
- *±200 ps delay match (one input to all outputs)*
- *ECL-level data inputs/outputs; CMOS-level control inputs*
- *Low crosstalk*
- *Fully differential data path*
- *Double row of output select latches minimizes reconfiguration time*
- *Available in 132-pin leaded chip carrier*

SWITCHING PRODUCTS

Figure 1. TQ8016 Architecture

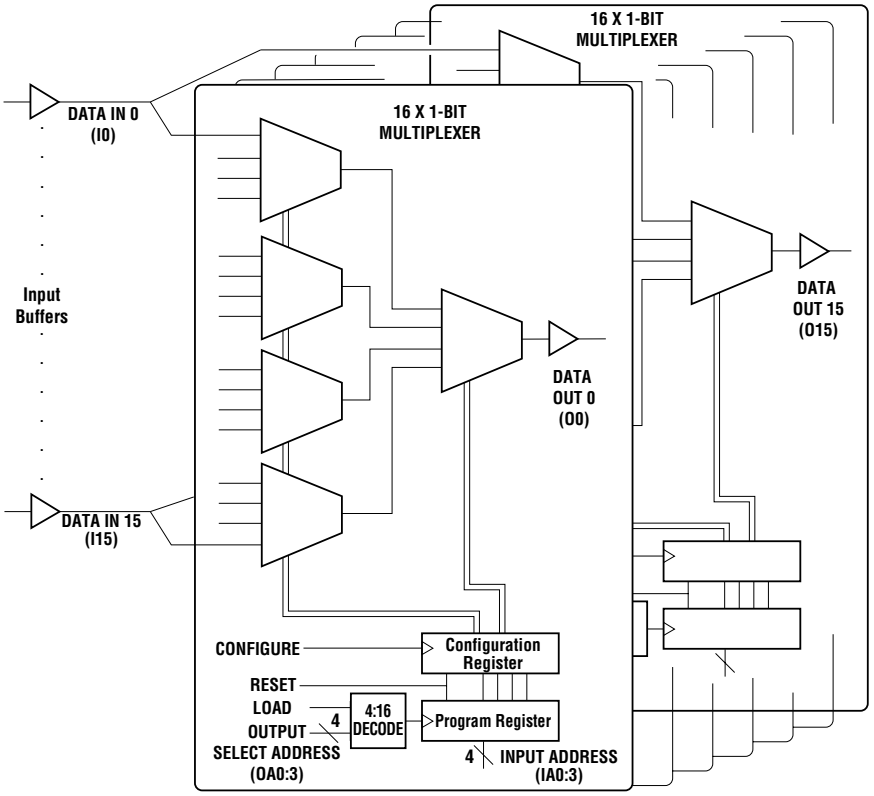


Table 1. Pin Descriptions

Pin Name	*Levels*	*Description*
D0–D15	ECL	Differential Data Inputs
D0–D15	ECL	Differential Data Inputs
D0–D15	ECL	Differential Data Inputs
O0–O15	ECL	Differential Data Outputs
O0–O15	ECL	Differential Data Outputs
IA0–IA3	CMOS	Input Address
OA0–OA3	CMOS	Output Address
CONFIGURE	CMOS	Switch Reconfiguration

Figure 2. Pinout

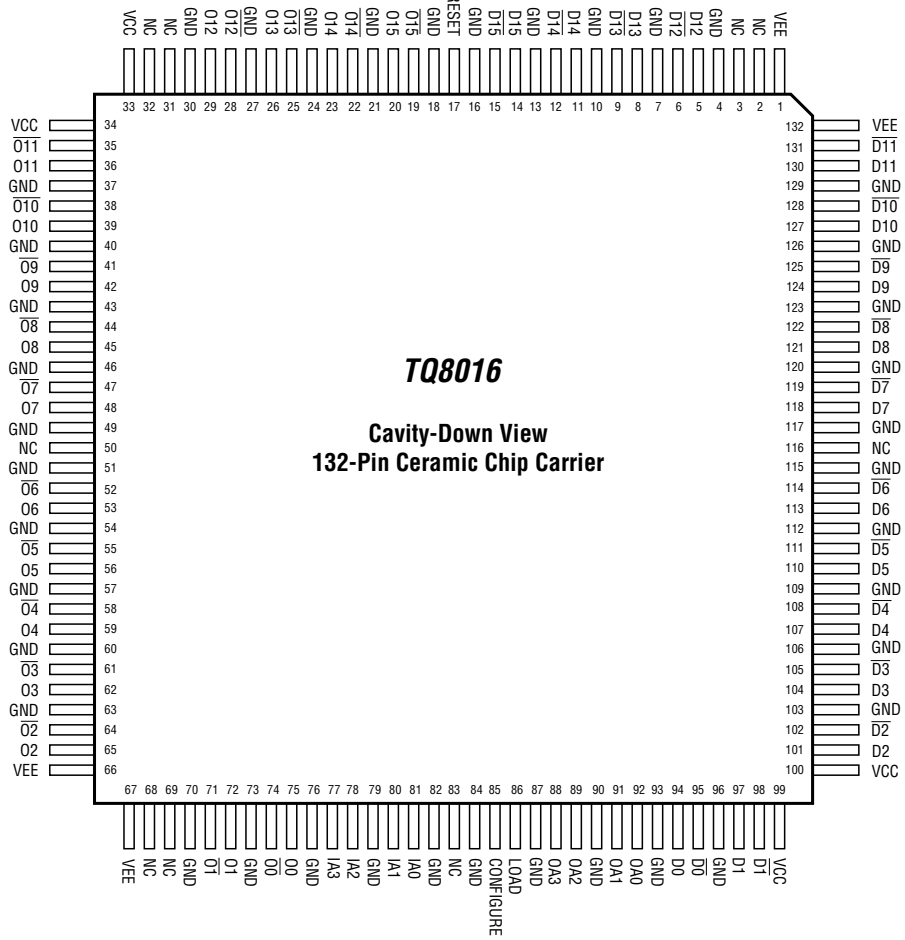


Table 1. Pin Descriptions (continued)

Pin Name	*Levels*	*Description*
RESET	CMOS	Configures the switch to *Broadcast* or *Pass-Through* modes, overwriting existing configurations. **Broadcast mode:** All output ports are connected to data input port 0. This mode is selected by applying a RESET "high" pulse with CONFIGURE held "low." **Pass-through mode:** I0 is connected to O0, I1 to O1, and so on. This mode is selected by applying a RESET "high" pulse with CONFIGURE held "high."
LOAD	CMOS	Loads Input Address
GND	0 V.	Ground Reference
VEE	–5 V	Power Supply
VCC	+5 V	Power Supply

Table 2. Absolute Maximum Ratings[4]

Symbol	Parameter	Absolute Max. Rating	Notes
T_{STOR}	Storage Temperature	–65° C to +150° C	
T_J	Junction Temperature	–55° C to +150° C	
T_C	Case Temperature Under Bias	–55° C to +125° C	1
V_{CC}	Supply Voltage	0 V to +7 V	2
V_{EE}	Supply Voltage	–7 V to 0 V	2
V_{TT}	Load Termination Supply Voltage	V_{EE} to 0 V	3
V_{IN}	Voltage Applied to Any ECL Input; Continuous	V_{EE} –0.5 V to +0.5 V	
I_{IN}	Current Into Any ECL Input; Continuous	–1.0 mA to +1.0 mA	
V_{IN}	Voltage Applied to Any TTL/CMOS Input; Continuous	–0.5 V to V_{CC} +0.5 V	
I_{IN}	Current Into Any TTL/CMOS Input; Continuous	–1.0 mA to +1.0 mA	
V_{OUT}	Voltage Applied to Any ECL Output	V_{EE} –0.5 V to +0.5 V	3
I_{OUT}	Current From Any ECL Output; Continuous	–40 mA	
P_D	Power Dissipation per Output $P_{OUT} = (GND – V_{OUT}) \times I_{OUT}$	50 mW	

Notes: 1. T_C is measured at case top.
2. All voltages specified with respect to GND, defined as 0V.
3. Subject to I_{OUT} and power dissipation limitations.
4. Absolute maximum ratings, as detailed in this table, are the ratings beyond which the device's performance may be impaired and/or permanent damage to the device may occur. Functionality and/or adherence to electrical specifications is not implied when the device is subjected to conditions that exceed, singularly or in combination, the operating range specified in the Recommended Operating Conditions table, below.

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Table 3. Recommended Operating Conditions[3]

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
T_C	Case Operating Temperature	0	25	85	°C	1
GND	Ground Reference Voltage		0		V	
V_{CC}	Supply Voltage	4.5		5.5	V	
V_{EE}	Supply Voltage	–5.5		–4.5	V	
V_{TT}	Load Termination Supply Voltage		–2.0		V	2
R_{LOAD}	Output Termination Load Resistance		50		Ω	2

Notes: 1. T_C measured at case top. Use of adequate heatsink is required.
2. The V_{TT} and R_{LOAD} combination is subject to maximum output current and power restrictions.
3. Functionality and/or adherence to electrical specifications is not implied whenthe device is subjected to conditions that exceed, singularly or in combination, the operating ranges specified.

Table 4. DC Characteristics[1] *T_C = 0°C to 85°C, V_{CC} = 4.5 V to 5.5 V, V_{EE} = –5.5 V to –4.5 V, GND = 0 V, unless otherwise indicated.*

Symbol	Parameter	Min	Typ	Max	Units	Test Cond.	Notes
V_{IH}	ECL Input Voltage High	–1100		–500	mV		
V_{IL}	ECL Input Voltage Low	V_{TT}		–1500	mV		
I_{IH}	ECL Input Current High			+30	uA	V_{IH} = 0.7 V	
I_{IL}	ECL Input Current Low	–30			uA	V_{IL} = –2.0 V	
V_{ICM}	ECL Input Common Mode Voltage	–1500		–1100	mV		
V_{IDIF}	ECL Input Differential Voltage (P–P)	400		1200	mV		
V_{IH}	CMOS Input Voltage High	3.5		V_{CC}	V		
V_{IL}	CMOS Input Voltage Low	0		1.5	V		
I_{IH}	CMOS Input Current High			+100	uA	V_{IH} = V_{CC}	
I_{IL}	CMOS Input Current Low	–100			uA	V_{IL} = 0 V	
V_{OCM}	ECL Output Common Mode	–1500		–1100	mV		
V_{ODIF}	ECL Output Differential Voltage	600			mV		
V_{OH}	ECL Output Voltage High	–1000		–600	mV		
V_{OL}	ECL Output Voltage Low	V_{TT}		–1600	mV		
I_{OH}	ECL Output Current High	20	23	27	mA		
I_{OL}	ECL Output Current Low	0	5	8	mA		
I_{CC}	Power Supply Current		15	20	mA		2
I_{EE}	Power Supply Current		730	950	mA		2

Notes: 1. Test conditions unless otherwise indicated: V_{TT} = –2.0 V, R_{LOAD} = 50 Ω to V_{TT}.
2. Positive current is defined as flowing into the device and negative current as flowing out of the device. I_{CC} typically flows into the device and I_{EE} flows out of the device.

Table 5. AC Characteristics[1] – *Within recommended operating conditions, unless otherwise indicated.*

Symbol	Parameter	Min	Typ	Max	Units	Notes
	Maximum Data Rate/Port			1.3	Gb/s	1,2
	Jitter			150	ps pk–pk	1
T_1	Channel Propagation Delay		1200	2000	ps	
T_2	Ch-to-Ch Propagation Delay Skew		400	500	ps	
T_3	CONFIG to Data Out (Oi) Delay			5	ns	
T_4	LOAD Pulse Width	7			ns	
T_5	CONFIG Pulse Width	7			ns	
T_6	IAi to LOAD High Setup Time	0			ns	
T_7	LOAD to IAi Low Hold Time	3			ns	
T_8	OAi to LOAD High Setup Time	0			ns	
T_9	LOAD to OAi Low Hold Time	3			ns	
T_{10}	Load ↑ to CONFIG ↑	0			ns	
T_{11}	RESET Pulse Width	10			ns	
$T_{R,F}$	Output Rise or Fall Time		250	400	ps	3

Notes: 1. Test conditions: V_{TT} = –2.0 V, R_{LOAD} = 50 Ω to V_{TT}; ECL inputs: V_{IH} = –1.1 V; V_{IL} = –1.5 V; CMOS inputs: V_{IH} = 3.5 V, V_{IL} = 1.5 V; ECL outputs: $V_{OH} \geq$ –1.0 V, $V_{OL} \leq$ –1.6 V; ECL inputs rise and fall times ≤ 1 ns; CMOS inputs rise and fall times ≤ 20 ns. A bit error rate of 1E – 13 BER or better for 2^{23} – 1 PRBS pattern, jitter and rise/fall times are guaranteed through characterization.
2. 1.2 Gb/s Non-Return-Zero (NRZ) data equivalent to 600 MHz clock signal.
3. Rise and fall times are measured at the 20% and 80% points of the transition from V_{OL} max to V_{OL} min.

Figure 3. Timing Diagram — Switch Configuration

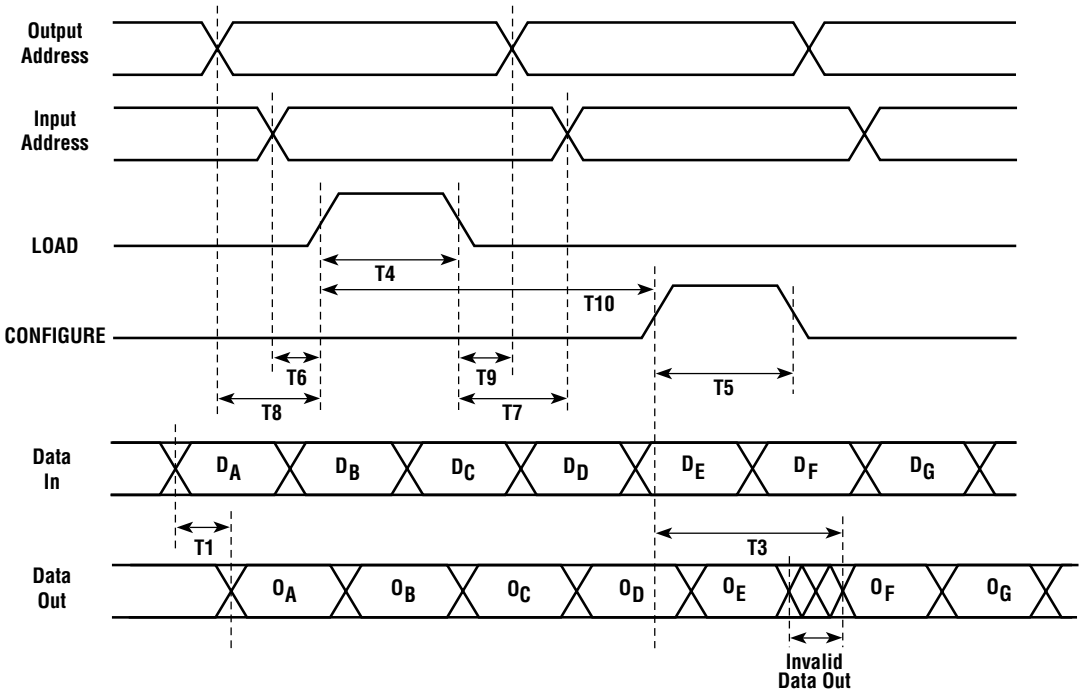
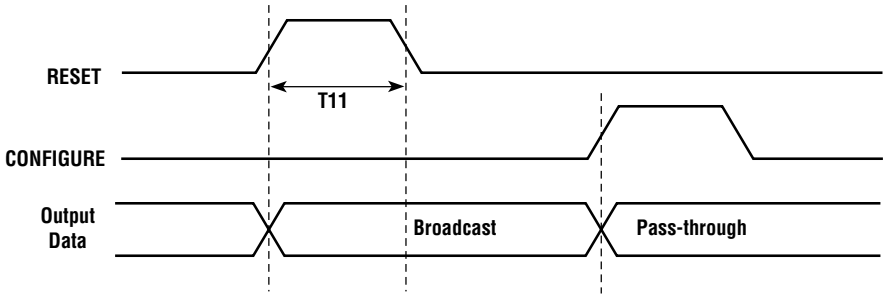
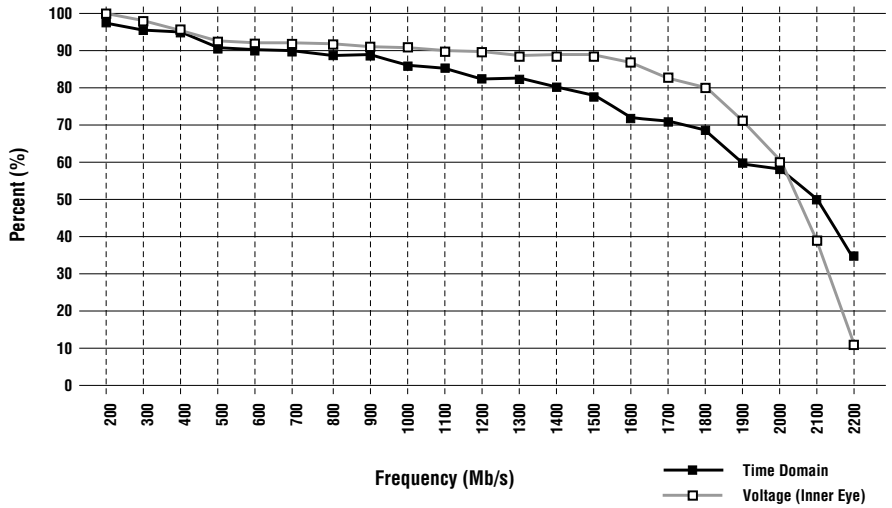


Figure 4. Timing Diagram — Reset



Notes: 1. LOAD input must remain LOW to insure correct programming of the switch
2. "Broadcast" is defined as data input 0 to all data outputs (0..15).
3. "Pass-through" is defined as data input 0 to data output 0, data input 1 to data output 1, etc.

Figure 5. AC Performance Measurements
(Percent Recoverable "Eye" vs. Frequency 16 x 16)



Typical Error-Free Area

The graph in Figure 5 shows the typical error-free area of a $2^{23} - 1$ Pseudo-Random Bit Stream (PRBS) "eye" pattern. Data is provided for both time and voltage domains of the differential DIN0 to DOUT0 data path for various data rates. An interference pattern was applied to all other inputs in parallel to induce worst-case cross talk.

For the time domain, Peak-to-Peak Jitter was measured at the eye crossing.

An error-free percentage value was computed using the following formula:

(Data_Period - PPJitter) x 100 / Data_Period

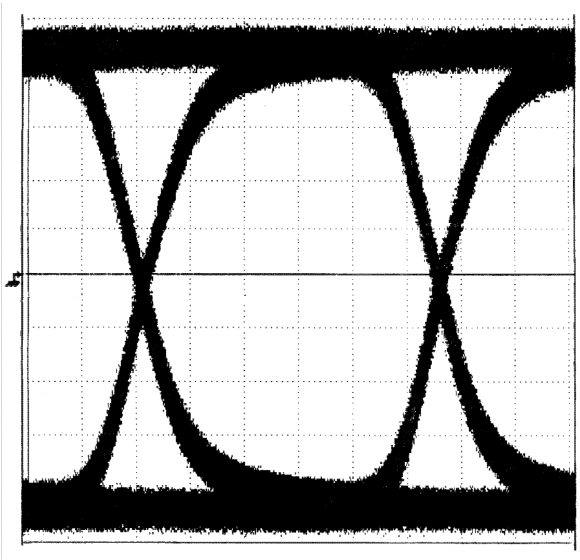
Voltage values are referenced to an initial inner eye measurement at 400 MBs. Subsequent percentage values were computed using the following formula:

V_{INNER} x 100 / V_{INNER} @ 400 MBs

Table 6. Typical Differential Waveform Characteristics *(OUT – $\overline{OUT}$)*

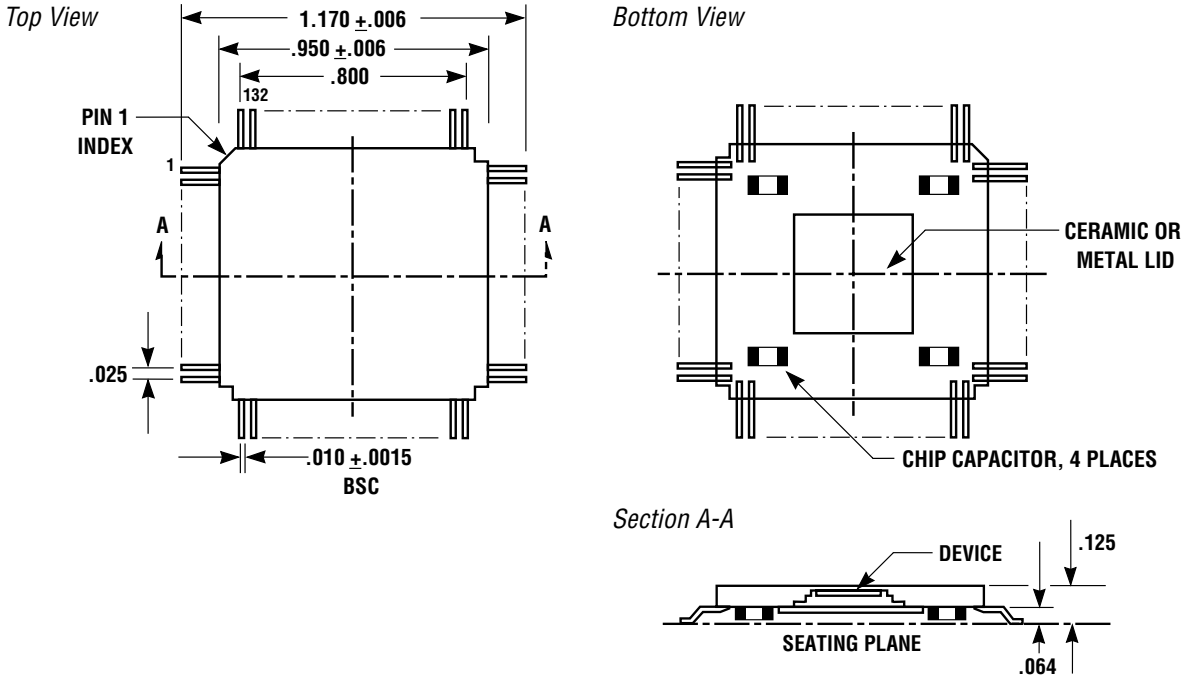
Frequency	1200 Mb/s
Fall Time (20% – 80%)	195 ps
Rise Time (20% – 80%)	1200 Mb/s
Jitter (peak-to-peak)	40 ps
Time/division	125 ps
Volts/division	250 mV

Figure 5. 1200 Mb/s Data "Eye" Pattern



Time/Div: 150 ps

Figure 6. Mechanical Dimensions



Ordering Information

TQ8016-M *1.3 Gb/s 16x16 ECL Crosspoint Switch*

Additional Information

For latest specifications, additional product information,
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