TRIQUINT SEMICONDUCTOR, INC.

TQS

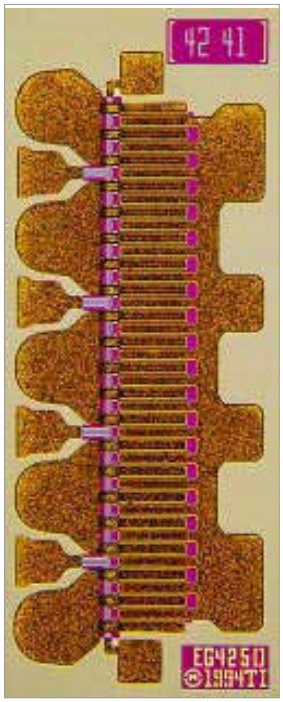
TGF4250-EEU

4.8 mm Discrete HFET

4250

- **4800 µm x 0.5 µm HFET**
- **Nominal Pout of 34-dBm at 8.5-GHz**
- **Nominal Gain of 8.5-dB at 8.5-GHz**
- **Nominal PAE of 53% at 8.5-GHz**
- **Suitable for high reliability applications**
- **0,572 x 1,334 x 0,102 mm (0.023 x 0.053 x 0.004 in.)**

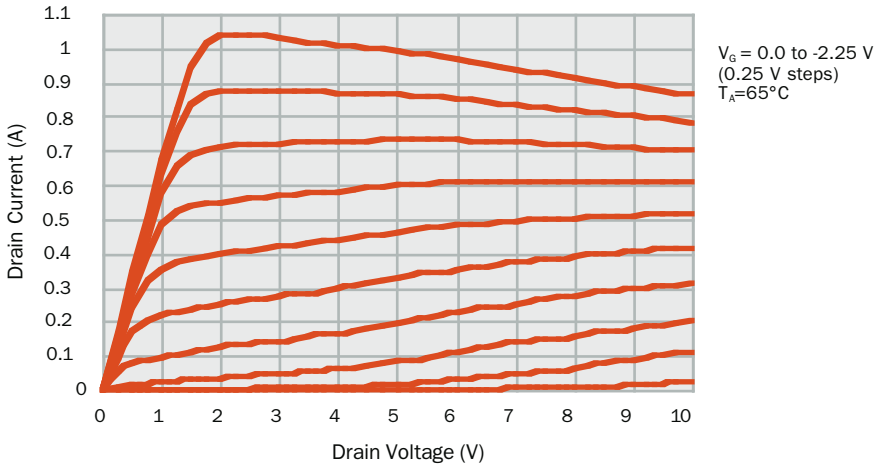
PHOTO ENLARGEMENT



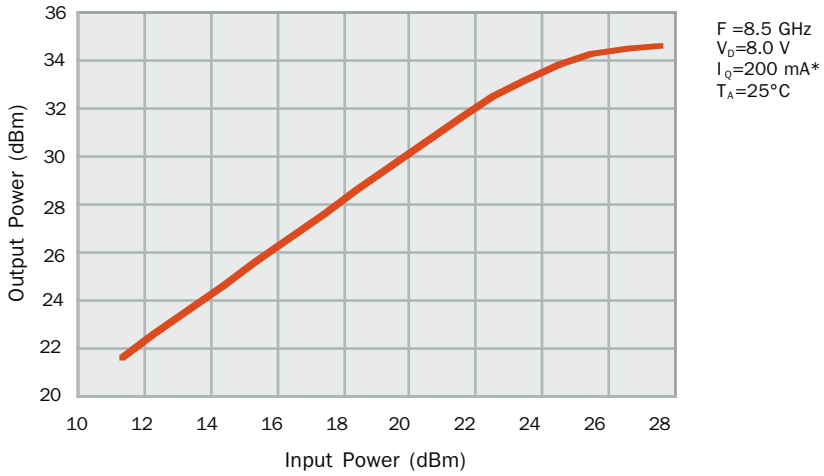
DESCRIPTION

The TriQuint TGF4250-EEU is a single gate 4.8 mm discrete GaAs Heterostructure Field Effect Transistor (HFET) designed for high efficiency power applications up to 10.5-GHz in Class A and Class AB operation. Typical performance at 2-GHz is 34-dBm power output, 13-dB gain, and 63% PAE. Bond pad and backside metalization is gold plated for compatibility with eutectic alloy attach methods as well as thermocompression and thermosonic wire-bonding processes. The TGF4250-EEU is readily assembled using automatic equipment.

EXAMPLE OF DC I-V CURVES

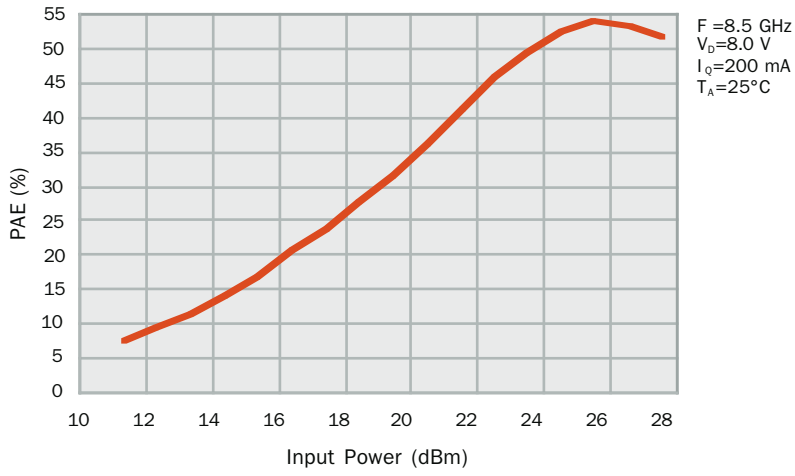


OUTPUT POWER VS. INPUT POWER

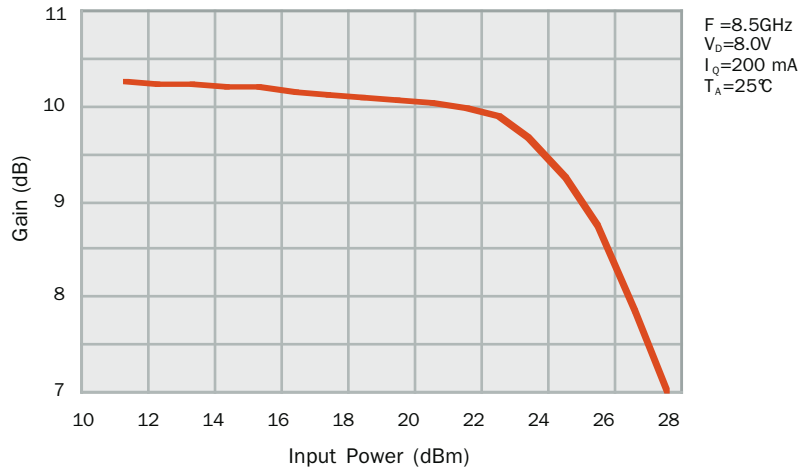


* I_Q is defined as the drain current before application of RF signal at the input.

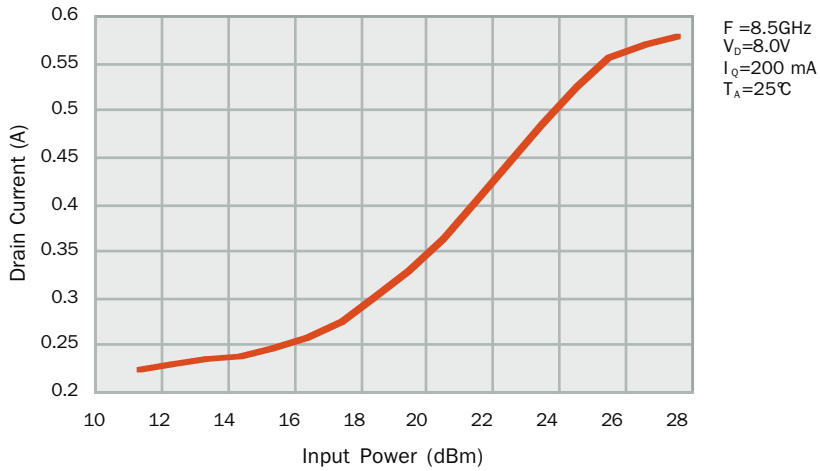
POWER ADDED EFFICIENCY VS. INPUT POWER



GAIN VS. INPUT POWER



DRAIN CURRENT VS. INPUT POWER



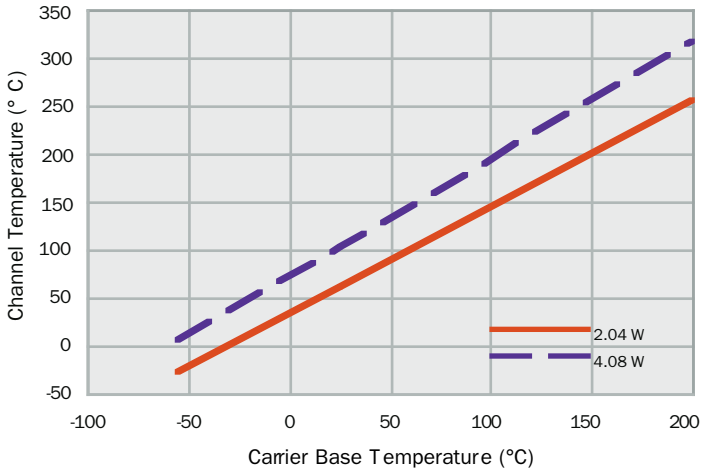
ABSOLUTE MAXIMUM RATINGS

Drain-to-source voltage, V_{DS}	12 V
Gate-to-source voltage, V_{GS}	-5 V to 0 V
Mounting temperature (30 sec), T_M	320 C
Storage temperature range, T_{STG}	-65 to 200 C
Power dissipation, P_D	(see thermal data on next page)
Operating channel temperature, T_{CH}	(see thermal data on next page)

Ratings over operating channel temperature (unless otherwise noted)

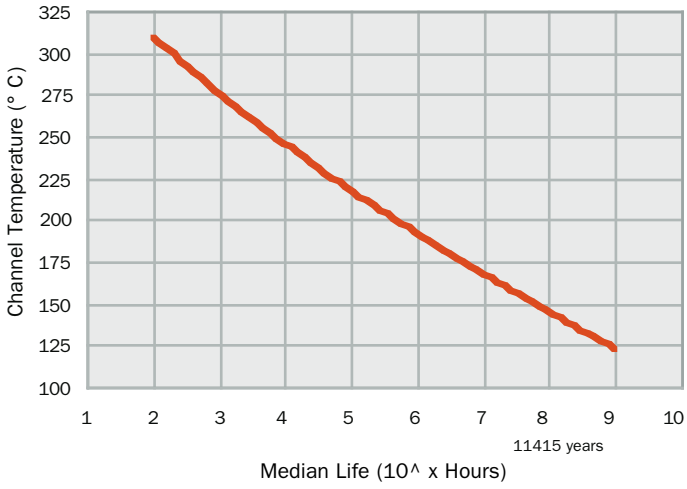
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "RF and DC Characteristics" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PREDICTED CHANNEL TEMPERATURE VS. CARRIER BASE TEMPERATURE
at 2.04 W and 4.08 W dissipated power



38 µm AuSn solder attach to 0.5 mm CuMo Carrier.

HFET CHANNEL TEMPERATURE VS. MEDIAN LIFE



RF AND DC CHARACTERISTICS

	PARAMETER	MIN	NOMINAL	MAX	UNIT
Pout	Output Power	33	34	-	dBm
G_P	Power Gain	7	8.5	-	dB
PAE	Power Added Efficiency	47	53	-	%
I_{DSS}	Drain Saturation Current	816	1176	1536	mA
G_M	Transconductance	576	792	1008	mS
V_P	Pinch Off Voltage	-2.7	-1.85	-1	V
BV_{GS}	Breakdown Voltage Gate-Source	-30	-22	-17	V
BV_{GD}	Breakdown Voltage Gate-Drain	-30	-22	-17	V

Pout, Gain, and PAE: Measured at 8.5-GHz, drain voltage of 8.0 V . Gate voltage is adjusted to achieve quiescent current of approximately 20% I_{DSS} with no RF signal applied. The source is grounded. Input power between 25 and 26-dBm.

I_{DSS}: Saturated drain-source current. Search for the maximum I_{DS} at V_{GS} = 0.0 V, and V_{DS} swept between 0.5 V to 3.5 V. Note that the drain voltage at which I_{DSS} is located and recorded as V_{DSP}.

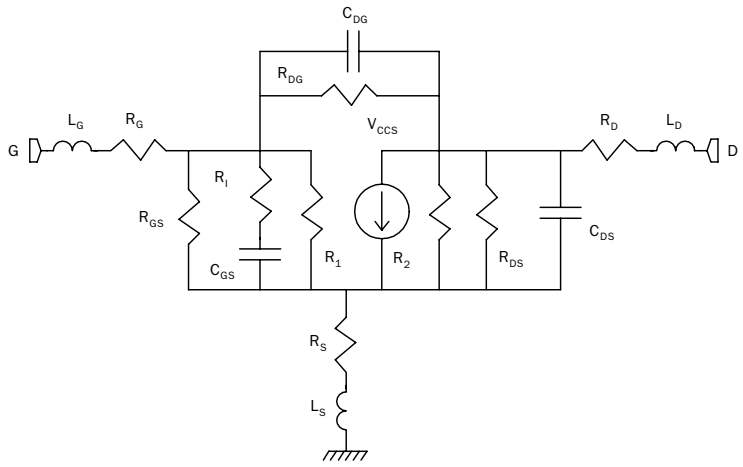
G_M: Transconductance. $(I_{DSS} - I_{DS1})/ |V_G1|$. I_{DS1} measured at V_{G1} = -0.25 V using the knee search technique; V_{DS} swept between 0.5 V and V_{DSP} to search for maximum I_{DS1}.

V_P: Pinch off voltage. V_{GS} for I_{DS} = 0.5 mA/mm of gate width. V_{DS} fixed at 2.0 V, V_{GS} swept to bring I_{DS} to 0.5 mA/mm. Sweep will stop if V_P current not found beyond 0.5 V of the minimum V_P specification.

BV_{GS}: Breakdown voltage, gate to source. I_{BD} = 1.0 mA/mm of gate width. Source fixed at ground, drain not connected (floating). When 1.0mA/mm drawn at gate, V_{GS} measured as BV_{GS}.

BV_{GD}: Breakdown voltage, gate to drain. I_{BD} = 1.0 mA/mm of gate width. Drain fixed at ground, source not connected (floating). When 1.0 mA/mm drawn at the gate, V_{GD} measured as BV_{GD}.

LINEAR MODEL



V_{DS} = 8.0 V and 30% I_{DSS} at T = 25°C

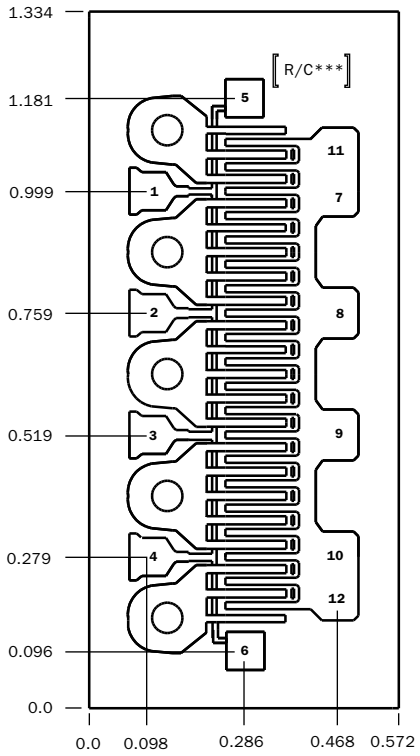
FET Elements		**VCCS Parameters**
L_G = 0.010525 nH	R_{DG} = 51000	M = 531.6 mS
R_G = 0.21075	R_S = 0.1	A = 0
R_{GS} = 20425	L_S = 0.011 nH	R1 = 1E19
R_I = 0.3025	R_{DS} = 24.5025	R2 = 1E19
C_{GS} = 4.84 pF	C_{DS} = 1.013 pF	F = 0
C_{DG} = 0.4015 pF	R_D = 0.165	T = 5.49 pS
	L_D = 0.0055 nH	

MODELED S-PARAMETERS

Frequency	S_{11}		S_{21}		S_{12}		S_{22}	
(GHz)	MAG	ANG(°)	MAG	ANG(°)	MAG	ANG(°)	MAG	ANG(°)
0.5	0.943	-106.98	9.887	122.68	0.026	35.10	0.533	-163.66
1.0	0.932	-139.41	5.725	103.61	0.030	19.75	0.591	-168.52
1.5	0.929	-152.35	3.935	94.21	0.031	13.81	0.608	-170.21
2.0	0.928	-159.14	2.978	87.84	0.031	10.87	0.617	-170.66
2.5	0.928	-163.31	2.386	82.79	0.031	9.25	0.625	-170.60
3.0	0.929	-166.14	1.984	78.43	0.030	8.38	0.633	-170.31
3.5	0.929	-168.18	1.694	74.50	0.030	8.00	0.641	-169.91
4.0	0.930	-169.74	1.474	70.85	0.029	7.98	0.650	-169.49
4.5	0.931	-170.97	1.302	67.41	0.029	8.27	0.659	-169.07
5.0	0.932	-171.97	1.163	64.14	0.028	8.84	0.668	-168.69
5.5	0.933	-172.82	1.048	61.02	0.028	9.67	0.678	-168.35
6.0	0.935	-173.54	0.952	58.01	0.027	10.77	0.688	-168.07
6.5	0.936	-174.17	0.870	55.13	0.026	12.13	0.698	-167.84
7.0	0.937	-174.73	0.800	52.35	0.026	13.74	0.708	-167.66
7.5	0.938	-175.23	0.738	49.67	0.025	15.62	0.718	-167.54
8.0	0.940	-175.69	0.684	47.09	0.025	17.75	0.728	-167.47
8.5	0.941	-176.12	0.637	44.61	0.024	20.12	0.738	-167.44
9.0	0.942	-176.51	0.594	42.22	0.024	22.72	0.748	-167.46
9.5	0.944	-176.88	0.556	39.92	0.024	25.51	0.757	-167.52
10.0	0.945	-177.23	0.521	37.70	0.024	28.46	0.767	-167.61
10.5	0.946	-177.57	0.490	35.58	0.023	31.54	0.776	-167.73

V_{DS} = 8 V and 30% I_{DSS} at T_A = 25°C

MECHANICAL DRAWING



Units: millimeters
Thickness: 0.102
Chip size ± 0.0508

Bond pad 1 (gate): 0.075 x 0.075
Bond pad 2 (gate): 0.075 x 0.075
Bond pad 3 (gate): 0.075 x 0.075
Bond pad 4 (gate): 0.075 x 0.075
Bond pad 5 (gate): 0.075 x 0.075*
Bond pad 6 (gate): 0.075 x 0.075*

Bond pad 7 (drain): 0.089 x 0.089
Bond pad 8 (drain): 0.102 x 0.089
Bond pad 9 (drain): 0.102 x 0.089
Bond pad 10 (drain): 0.089 x 0.089
Bond pad 11 (drain): 0.089 x 0.089**
Bond pad 12 (drain): 0.089 x 0.089**

Minimum connections to Bond Pads 1 to 4 and 7 to 10.

Sources are connected to backside metalization.

* Gate pad used when paralleling HFETS.

** Drain pad used when paralleling HFETS.

*** R/C denotes the row, column location of the device on the wafer.

NOTES

Gate bias supplies should be designed to sink or source gate current. The magnitude and direction of the gate current is a function of bias point, load impedance, and drive level.

Space qualification is in progress; contact TriQuint for details.