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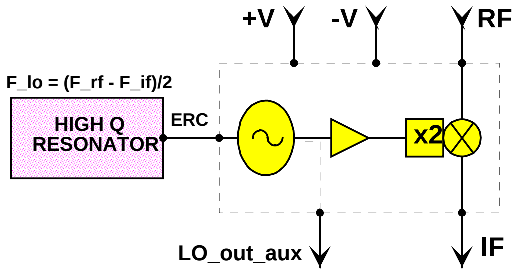
CHV2241

K-band Oscillator with integrated Q-band Harmonic Mixer

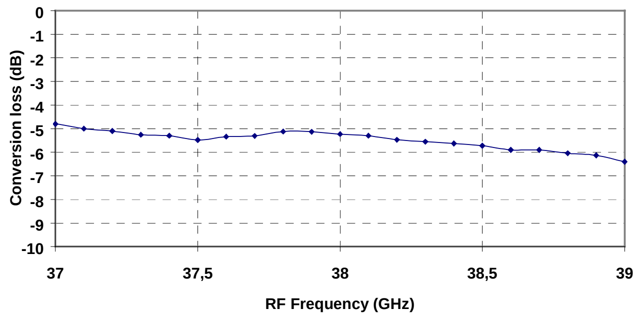
GaAs Monolithic Microwave IC

Description

The CHV2241 is a monolithic multifunction proposed for frequency generation and transposition. It integrates a K-band oscillator, a Q-band harmonic mixer and buffer amplifiers. For performance optimisation, an external port (ERC) allows a passive resonator coupling to the oscillator (at half output frequency). All the active devices are internally self biased.
The circuit is manufactured with the P-HEMT process : 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.



Multifunction block diagram



Typical conversion loss characteristic

Main Features

- K-band Oscillator + Q-band harmonic mixer
- External resonator for centre frequency control and phase noise optimisation
- High quality oscillator when coupled to a dielectric resonator
- Low conversion loss
- High temperature range
- On chip self biasing
- Automatic assembly oriented
- Chip size 1.82 x 0.97 x 0.1 mm

Main Characteristics

Tamb = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F_rf	RF frequency	37.5	38.25	39	GHz
F_lo	Oscillator frequency	(F_rf - F_if)/2			
Pn	Oscillator phase noise @ 100kHz (38GHz)		-100		dBc/Hz
Lc	Conversion loss		7		dB

ESD Protections : Electrostatic discharge sensitive device observe handling precautions !

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Electrical Characteristics

Full temperature range, used according to section “Typical assembly and bias configuration”

Symbol	Parameter	Min	Typ	Max	Unit
F_rf	RF frequency	37.5	38.25	39	GHz
F_if	IF frequency	0.1		1.5	GHz
F_lo	Oscillator frequency (1)	(F_rf - F_if)/2			
P_lo	Auxiliary LO output power (optional)	-15	-8	-4	dBm
Pn	Phase noise (given at RF frequency) (2) @ 1kHz @ 10kHz @ 100kHz @ 200kHz @ 1MHz		 -45 -78 -105 -114 -129	 -35 -68 -95 -104 -119	 dBc/Hz
P_V+	Frequency pushing vs positive supply voltage		300	1000	kHz/v
Lc	Conversion loss	3	7	11	dB
P_1dB_rf	RF input power at 1dB	-13	-8	0	dBm
Plolk_if	LO leakage at IF port (3)		-25	-18	dBm
P2lo_rf	2LO leakage at RF port (3)		-40	-30	dBm
VSWR_rf	VSWR at RF input port		2:1	2.5:1	
IMP_if	IF load impedance		50		Ω
+V	Positive supply voltage (4)	4.4	4.5	4.6	V
+I	Positive supply current		50	90	mA
-V	Negative supply voltage (4)	-4.6	-4.5	-4.4	V
-I	Negative supply current		6	10	mA
Top	Operating temperature range	-40		+100	°C

(1) The centre frequency is given by the external passive resonator.
See part “*Proposed external high Q resonator*“ for frequency temperature drift example.
DRO frequency long term stability is DR environment stability dependant (hermeticity …).
(2) This characteristic depends on the external resonator Q, the given performance has been obtained by using an external dielectric resonator (see section “Proposed External High Q resonator”)
(3) Without external filtering
(4) Negative supply voltage must be applied at least 1us before positive supply voltage.

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Absolute Maximum Ratings (1)

Symbol	Parameter	Values	Unit
P_rf	Maximum RF input power (2)	7	dBm
+V	Positive supply voltage	5	V
-V	Negative supply voltage	-5	V
+I	Positive supply current	100	mA
-I	Negative supply current	15	mA
Tstg	Storage temperature range	-55 to +155	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.
(2) CW mode.

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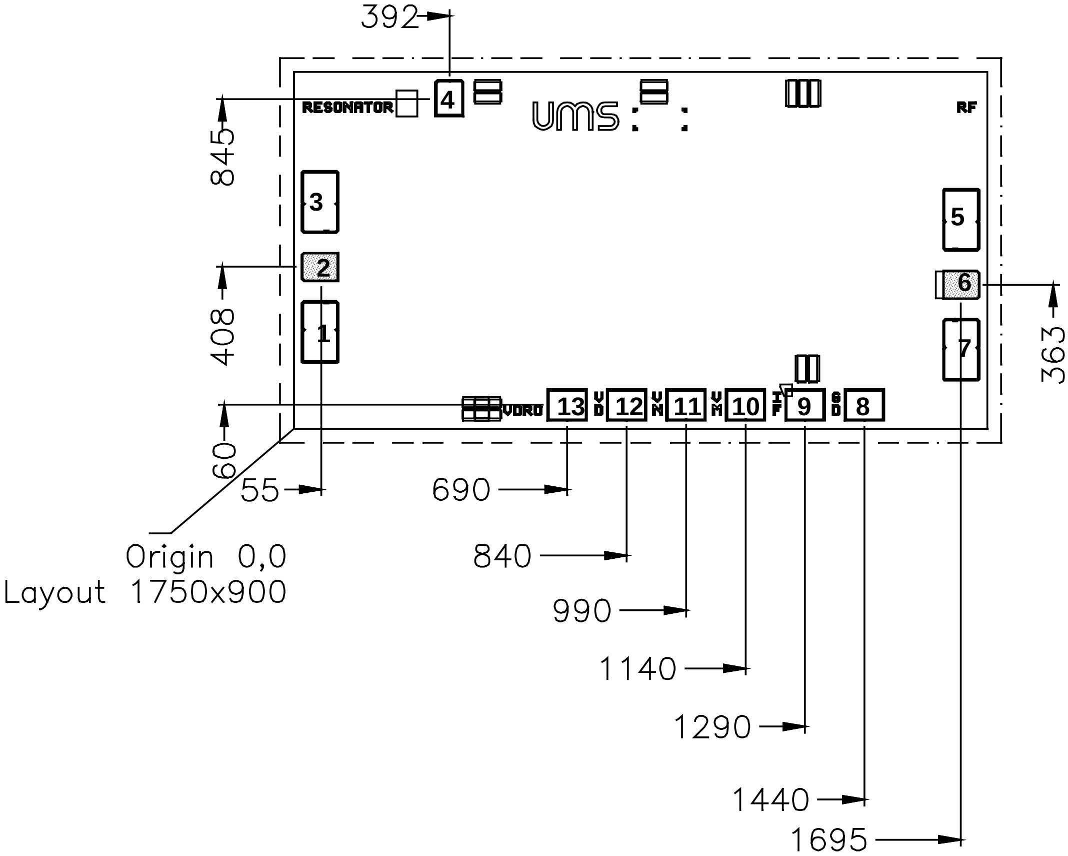
Chip Mechanical Data and Pin References



Unit = µm
External chip size (including saw streets)= 1820 x 970 +/- 35
Chip thickness = 100 +/- 10
HF Pads (2, 6) = 68 x 118
DC/IF Pads (+auxiliary LO output) = 100 x 100

Pin number	Pin name	Description
1,3,5,7,8		Ground : should not be bonded. If required, please ask for more information
2	**ERC**	External Resonator Coupling Port
4	**LO_OUT_AUX**	Oscillator auxiliary output port (optional)
6	**RF**	RF input port
9	**IF**	IF output port
10		NC
11	**-V**	Negative supply voltage
12,13	**+V**	Positive supply voltage

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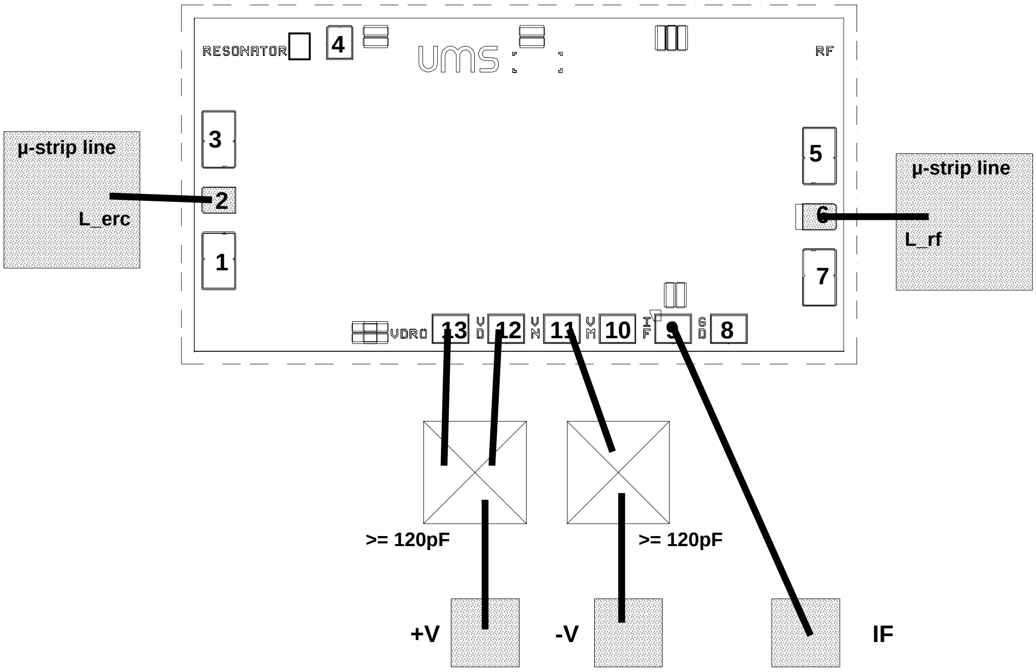
Typical Assembly and Bias Configuration



DC and control lines

This drawing shows an example of assembly and bias configuration. All the transistors are internally self biased. The positive and negative voltages can be respectively connected together (see drawing) according to the recommended values given in the electrical characteristics table.
For the RF pads the equivalent wire bonding inductances (diameter=25µm) have to be according to the following recommendation.

Port	Equivalent inductance (nH)	Approximative wire length (mm)
ERC (2)	L_erc = 0.4	0.5
LO_OUT_AUX (4) Optional	Not critical , < 1nH	
RF (6)	L_rf = 0.28	0.35

For a micro-strip configuration a hole in the substrate is recommended for chip assembly.

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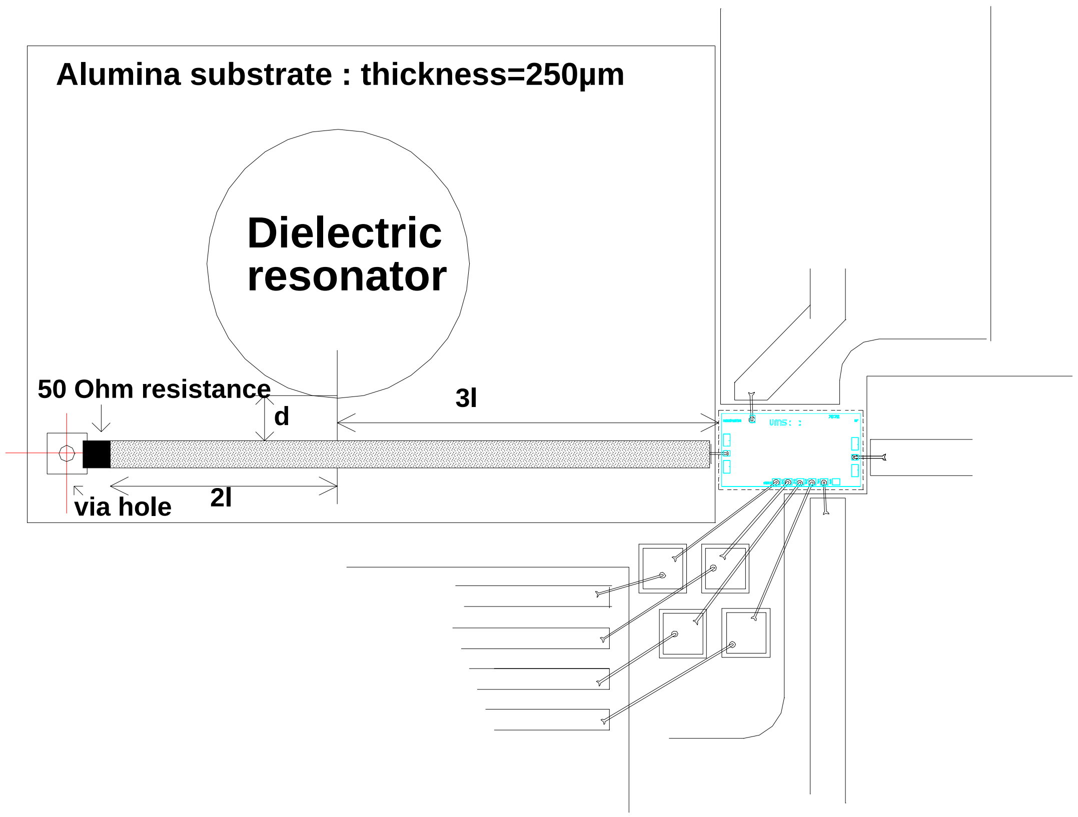
Proposed external high Q resonator

This chip has been especially designed to be coupled to a high Q dielectric resonator (For example typical Q. @ 10 GHz=24000 for MURATA /DRD036EC016). The resonance is given by a dielectric cylinder coupled to a 50Ω line. The size of the resonator gives the centre frequency and the space between the resonator and the line gives the loaded quality factor. The following drawing shows an example of external configuration. As it is the assembly of a test fixture all the biases are used and the auxiliary LO output is connected. However, for a fixed application the configuration given in the previous section can by applied.



Additional information

- **Resonator reference** example = MURATA /DRD036EC016. Other kind of resonators can be used (from TEKELEC or TRANS-TECH). The temperature coefficient has to be chosen according to the environment.
- **Temperature drift** : For example, in the –40 to +100°C temperature range, the frequency drift @ 38GHz is 12 MHz with the MURATA / DRD036EC016 resonator.
- **Resonator coupling** : d=0.3mm , l=1.5mm. These values have been used in the test fixture, of course they can be modified if the environment is different.
- **50Ω line width** on alumina (heigth=0.25mm) = 0.238mm
- **Cavity size** (mm) : 18 x 17 x 7

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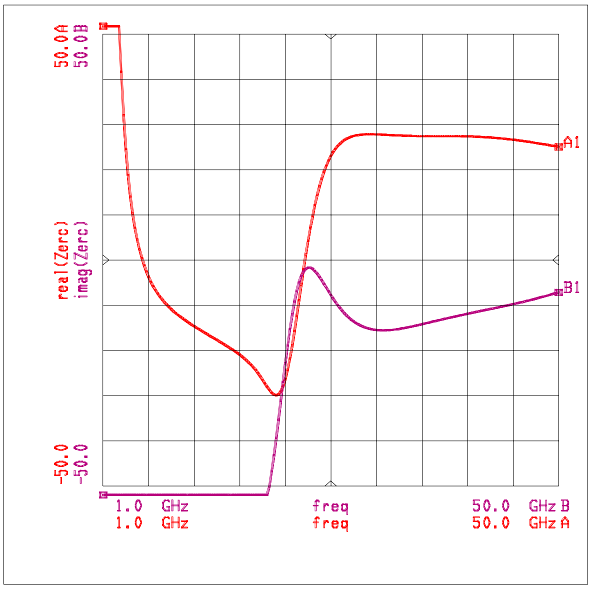
External Resonator Coupling Information

The external resonator has to be an equivalent series resonance. However, this impedance must be compatible to the negative impedance of the oscillator ERC port in order to obtain the oscillation conditions and to avoid parasitic oscillations. Typical impedance of ERC port (Zerc) is given in the following table. The diagram shows this impedance in a wider band. These values don’t include the wire bonding (self L_erc given in the previous section).

freq	real(Zerc)	imag(Zerc)
17.00E+09	-23.388	-69.744
17.42E+09	-24.410	-65.906
17.84E+09	-25.584	-61.883
18.26E+09	-26.882	-57.527
18.68E+09	-28.201	-52.662
19.10E+09	-29.326	-47.125
19.52E+09	-29.916	-40.849
19.94E+09	-29.565	-33.947
20.36E+09	-27.921	-26.763
20.78E+09	-24.830	-19.815
21.21E+09	-20.415	-13.648
21.63E+09	-15.035	-8.674
22.05E+09	-9.161	-5.087
22.47E+09	-3.250	-2.866
22.89E+09	2.338	-1.836
23.31E+09	7.371	-1.751
23.73E+09	11.732	-2.349
24.15E+09	15.397	-3.392
24.57E+09	18.398	-4.687
25.00E+09	20.805	-6.087



The recommended external resonator properties are:

- **series equivalent resonance**
- **highest possible Q (dielectric resonator, cavity ...) if no tuning bandwidth required**
- **resistance at resonant frequency lower than 20Ω**
- **out-off band impedance has to be designed to avoid parasitic oscillation.**

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Ordering Information

Chip form : CHV2241-99F/00

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