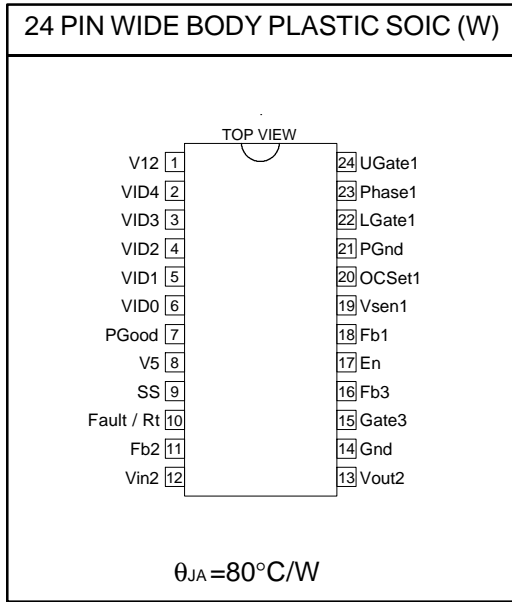


US3018

ABSOLUTE MAXIMUM RATINGS

V5 supply Voltage 7V
 V12 Supply Voltage 20V
 Storage Temperature Range -65 TO 150°C
 Operating Junction Temperature Range 0 TO 125°C

PACKAGE INFORMATION



ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over $V_{12} = 12\text{V}$, $V_5 = 5\text{V}$ and $T_a = 0$ to 70°C . Typical values refer to $T_a = 25^{\circ}\text{C}$. Low duty cycle pulse testing are used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Supply UVLO Section						
UVLO Threshold-12V		Supply ramping up		10		V
UVLO Hysterises-12V				0.4		V
UVLO Threshold-5V		Supply ramping up		4.3		V
UVLO Hysterises-5V				0.3		V
Supply Current						
Operating Supply Current	I_{12} I_5	V12 V5		6 20		mA

Switching Controller, Vcore (Vout 1)

VID Section

DAC output voltage (note 1)	Vdac		0.99Vs	Vs	1.01Vs	V
DAC Output Line Regulation				0.1		%
DAC Output Temp Variation				0.5		%
VID Input LO					0.8	V
VID Input HI			2			V
VID input internal pull-up resistor to V5				27		kΩ

Error Comparator Section						
Input bias current					2	uA
Input Offset Voltage			-2		+2	mV
Delay to Output		Vdiff=10mV			100	nS
Current Limit Section						
C.S Threshold Set Current				200		uA
C.S Comp Offset Voltage			-5		+5	mV
Hiccup Duty Cycle		Css=0.1 uF		10		%
Output Drivers Section						
Rise Time		CL=3000pF		70		nS
Fall Time		CL=3000pF		70		nS
Dead band Time Between High side and Synch Drive Vcore Switcher Only		CL=3000pF		200		nS
Oscillator Section (internal)						
Osc Frequency				200		Khz
2.5V Regulator (Vout 2)						
Reference Voltage	Vo2	Ta=25, Vout2 = FB2		1.260		V
Reference Voltage				1.260		V
Dropout Voltage		Io = 200 mA		0.6		V
Load Regulation		1mA < Io < 200 mA		0.5		%
Line Regulation		3.1V < Vin2 < 4V, Vo=2.5V		0.2		%
Input bias current					2	uA
Output Current			200			mA
Current limit			300			mA
Thermal Shutdown				145		°C
1.5V Regulator (Vout 3)						
Reference Voltage	Vo3	Ta=25, GATE3 = FB3		1.260		V
Reference Voltage				1.260		V
Input bias current					2	uA
Output Drive Current			50			mA
Power Good Section						
Core U.V lower trip point		Vsen1 ramping down		0.90Vs		V
Core U.V upper trip point		Vsen1 ramping up		0.92Vs		V
Core U.V Hysterises				.02Vs		V
Core O.V upper trip point		Vsen1 ramping up		1.10Vs		V
Core O.V lower trip point		Vsen1 ramping down		1.08Vs		V
Core O.V Hysterises				.02Vs		V
FB2 lower trip point		FB2 ramping down		0.95		V
FB2 upper trip point		FB2 ramping up		1.05		V
FB3 lower trip point		FB3 ramping down		0.95		V
FB3 upper trip point		FB3 ramping up		1.05		V
Power Good Output LO		RL=3mA		0.4		V
Power Good Output HI		RL=5K pull up to 5V		4.8		V
Fault (Overvoltage) Section						
Core O.V upper trip point		Vsen1 ramping up		1.17Vs		V
Core O.V lower trip point		Vsen1 ramping down		1.15Vs		V
Vin2 upper trip point		Vin2 ramping up		4.3		V
Vin2 lower trip point		Vin2 ramping down		4.2		V
FAULT Output HI		Io=3mA		10		V
Soft Start Section						
Pull up resistor to 5V		OCset=0V, Phase=5V		23		KΩ

Note 1: Vs refers to the set point voltage given in Table 1.

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Enable Section

En pin input LO voltage	Venl	Regulator OFF			0.8	V
En pin input HI voltage	Venh	Regulator ON	2			V
En pin input LO current		Ven=0V to 0.8V		0.01		uA
En pin input HI current		Ven=2V to 5V		20		uA

D4	D3	D2	D1	D0	Vs
0	1	1	1	1	1.30
0	1	1	1	0	1.35
0	1	1	0	1	1.40
0	1	1	0	0	1.45
0	1	0	1	1	1.50
0	1	0	1	0	1.55
0	1	0	0	1	1.60
0	1	0	0	0	1.65
0	0	1	1	1	1.70
0	0	1	1	0	1.75
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05

D4	D3	D2	D1	D0	Vs
1	1	1	1	1	2.0
1	1	1	1	0	2.1
1	1	1	0	1	2.2
1	1	1	0	0	2.3
1	1	0	1	1	2.4
1	1	0	1	0	2.5
1	1	0	0	1	2.6
1	1	0	0	0	2.7
1	0	1	1	1	2.8
1	0	1	1	0	2.9
1	0	1	0	1	3.0
1	0	1	0	0	3.1
1	0	0	1	1	3.2
1	0	0	1	0	3.3
1	0	0	0	1	3.4
1	0	0	0	0	3.5

Table 1 - Set point voltage vs. VID codes

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	Pin Description
6	VID0	LSB input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic "1" as either HI or Open. When left open, his pin is pulled up internally by a 27kΩ resistor to 5V supply.
5	VID1	Input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic "1" as either HI or Open. When left open, his pin is pulled up internally by a 27kΩ resistor to 5V supply.
4	VID2	Input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic "1" as either HI or Open. When left open, his pin is pulled up internally by a 27kΩ resistor to 5V supply.
3	VID3	MSB input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic "1" as either HI or Open. When left open, his pin is pulled up internally by a 27kΩ resistor to 5V supply.
2	VID4	This pin selects a range of output voltages for the DAC. When in the LOW state the range is 1.3V to 2.05V and when it switches to HI state the range is 2.0V to 3.5V. This pin is TTL compatible that realizes a logic "1" as either HI or Open. When left open, his pin is pulled up internally by a 27kΩ resistor to 5V supply.
7	PGOOD	This pin is an open collector output that switches LO when any of the outputs are outside of the specified under voltage trip point. It also switches low when Vsen1 pin is more than 10% above the DAC voltage setting.
18	FB1	This pin provides the feedback for the synchronous switching regulator. Typically this pin can be connected directly to the output of the switching regulator. However, a resistor divider is recommended to be connected from this pin to vout1 and GND to adjust the output voltage for any drop in the output voltage that is caused by the trace resistance. The value of the resistor connected from Vou1 to FB1 must be less than 100Ω.

PIN#	PIN SYMBOL	Pin Description
19	VSEN1	This pin is internally connected to the undervoltage and overvoltage comparators sensing the Vcore status. It must be connected directly to the Vcore supply.
12	VIN2	This pin is the input that provides power for the internal LDO regulator. It is also monitored for the under voltage and over voltage conditions.
20	OCSET1	This pin is connected to the Drain of the power MOSFET of the Core supply and it provides the positive sensing for the internal current sensing circuitry. An external resistor programs the C.S threshold depending on the Rds of the power MOSFET. An external capacitor is placed in parallel with the programming resistor to provide high frequency noise filtering.
23	PHASE1	This pin is connected to the Source of the power MOSFET for the Core supply and it provides the negative sensing for the internal current sensing circuitry.
9	SS	This pin provides the soft start for the switching regulator. An internal resistor charges an external capacitor that is connected from 5V supply to this pin which ramps up the outputs of the switching regulators, preventing the outputs from overshooting as well as limiting the input current. The second function of the Soft Start cap is to provide long off time (HICCUP) for the synchronous MOSFET during current limiting.
10	FAULT/Rt	This pin has dual function. It acts as an output of the OVP circuitry or it can be used to program the frequency using an external resistor. When used as a fault detector, if the switcher output exceed the OVP trip point, the FAULT pin switches to 12V and the soft start cap is discharged. If the FAULT pin is to be connected to any external circuitry, it needs to be buffered as shown in the application circuit.
15	GATE3	This pin controls the gate of an external transistor for the 1.5V GTL+ linear regulator.
16	FB3	This pin provides the feedback for the linear regulator that its output drive is GATE3.
13	VOUT2	This pin is the output of the internal LDO regulator.
11	FB2	This pin provides the feedback for the internal LDO regulator that its output is Vout4.
14	GND	This pin serves as the ground pin and must be connected directly to the ground plane.
21	PGND	This pin serves as the Power ground pin and must be connected directly to the GND plane close to the source of the synchronous MOSFET. A high frequency capacitor (typically 1 uF) must be connected from V12 pin to this pin for noise free operation.
22	LGATE1	Output driver for the synchronous power MOSFET for the Core supply.
24	UGATE1	Output driver for the high side power MOSFET for the Core supply.
1	V12	This pin is connected to the 12 V supply and serves as the power Vcc pin for the output drivers. A high frequency capacitor (typically 1 uF) must be placed close to this pin and PGND pin and be connected directly from this pin to the GND plane for the noise free operation.
8	V5	5V supply voltage. A high frequency capacitor (0.1 to 1 uF) must be placed close to this pin and connected from this pin to the GND plane for noise free operation.
17	En	This pin is a TTL compatible Enable pin. When this pin is left open or pulled high, the device is enabled and when is pulled low, it will disable the switcher and the LDO controller (Vout 3) leaving the internal 200mA regulator operational. When signal is given to enable the device, both switcher and Vout 3 will go through soft start, the same as during start up.

BLOCK DIAGRAM

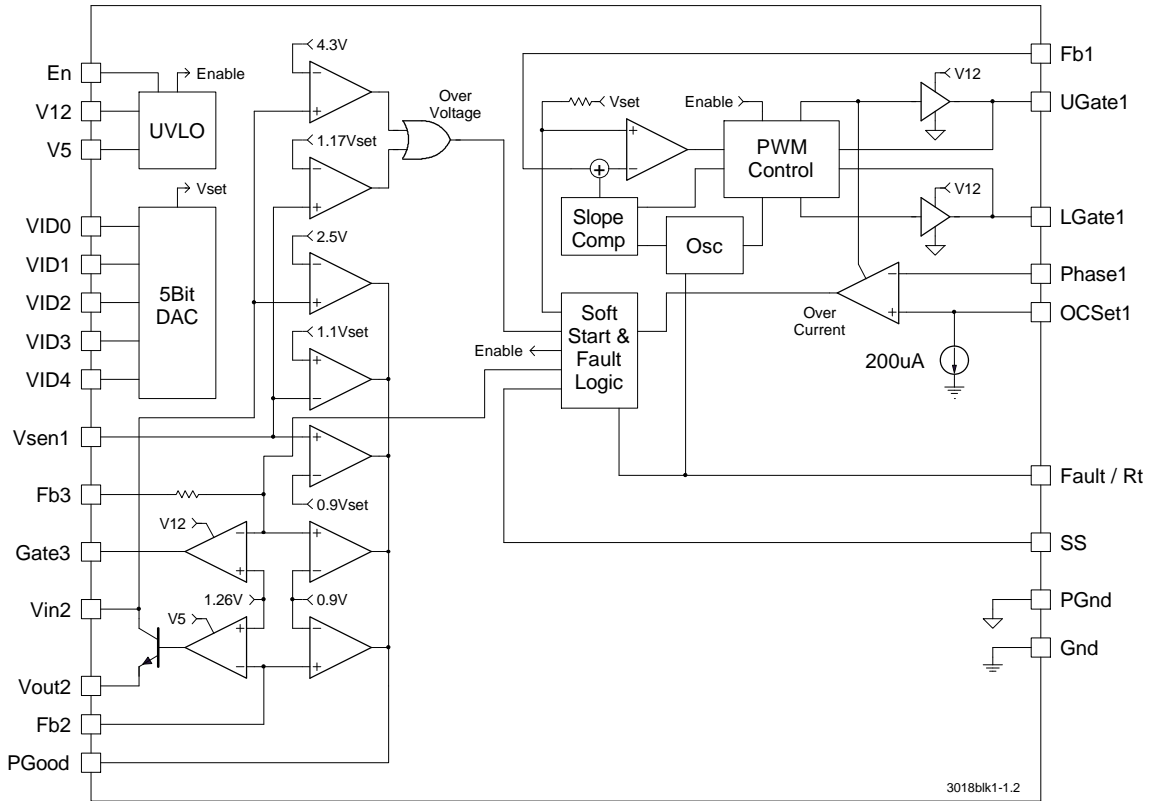


Figure 1 - Simplified block diagram of the US3018

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US3018 Application Parts List

Ref Desig	Description	Qty	Part #	Manuf
Q2	MOSFET	1	IRLR024, TO252 package	IR
Q3	MOSFET	1	IRL3103S, TO263 package	IR
Q4	MOSFET with Schottky	1	IRL3103D1S, TO263 package	IR
L1	Inductor	1	L=1uH, 5052 core with 4 turns of 1.0mm wire	Micro Metal
L3	Inductor	1	L=2.7uH, 5052B core with 7 turns of 1.2mm wire	Micro Metal
C1,17	Capacitor, Electrolytic	2	6MV1000GX, 1000uF,6.3V	Sanyo
C2	Capacitor, Electrolytic	1	10MV470GX, 470uF,10V	Sanyo
C3	Capacitor, Electrolytic	1	10MV1200GX, 1200uF,10V	Sanyo
C8	Capacitor, Ceramic	1	1uF, 0805	
C9,15,19	Capacitor, Ceramic	3	1uF, 0603	
C10	Capacitor, Ceramic	1	220pF, 0603	
C13	Capacitor, Ceramic	1	1000pF, 0603	
C14	Capacitor, Electrolytic	2	10MV1200GX, 1200uF,10V	Sanyo
C16	Capacitor, Electrolytic	6	6MV1500GX, 1500uF,6.3V,	Sanyo
C18	Capacitor, Electrolytic	1	6MV150GX, 150uF,6.3V	Sanyo
R5	Resistor	1	19.1 Ω , 1%, 0603	
R6,7,8	Resistor	3	100 Ω , 1%, 0603	
R12	Resistor	1	3.3k Ω , 5%, 0603	
R13,14,15	Resistor	3	4.7 Ω , 5%, 1206	
R16,17,21	Resistor	3	2.2k Ω , 1%, 0603	
R22	Resistor	1	10 Ω , 5%, 0603	

TYPICAL APPLICATION
(Dual Layout with HIP6018)

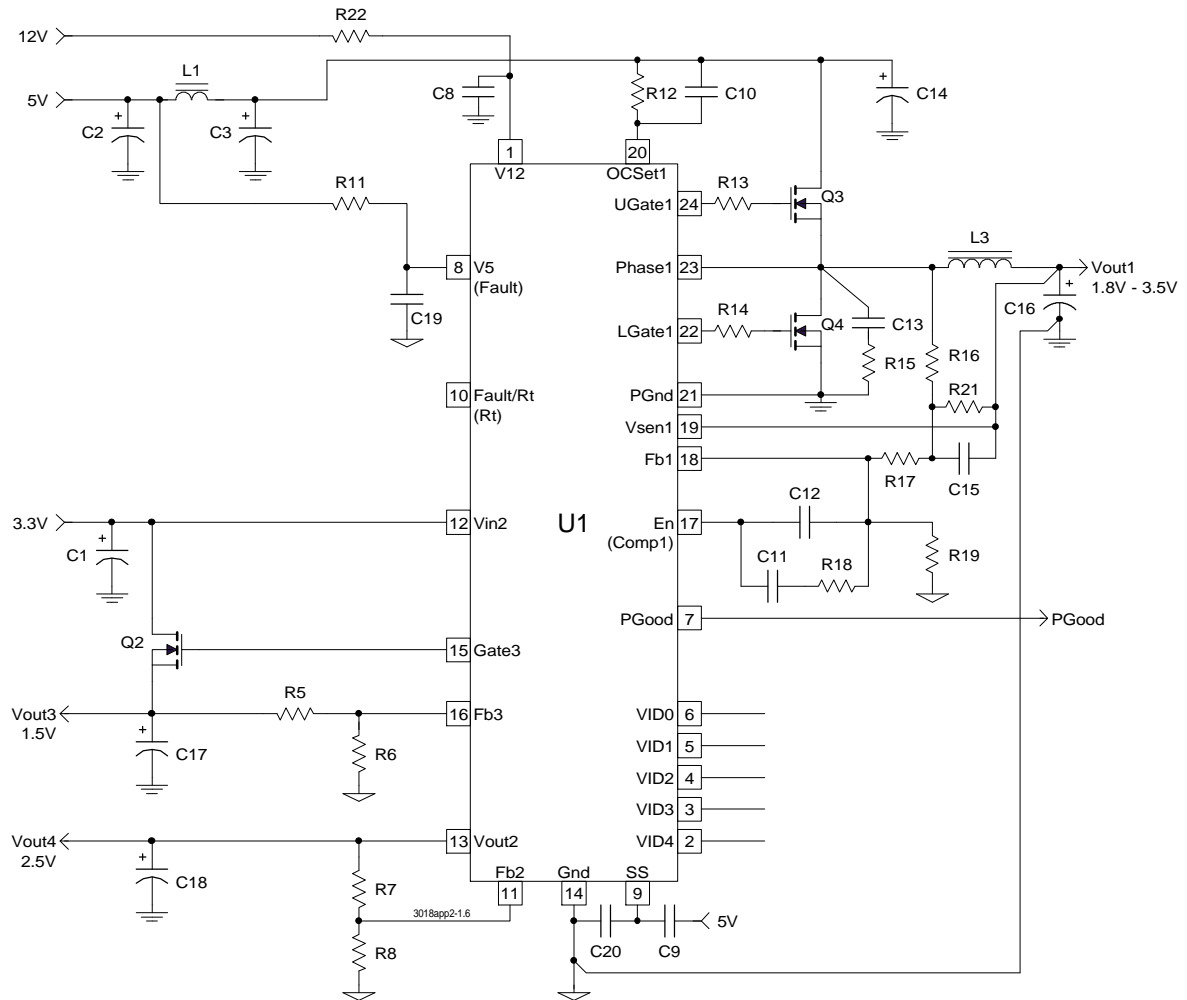


Figure 3 - Typical application of US3018 in a dual layout with HIP6018 for an on board DC-DC converter providing power for the Vcore , GTL+ & Clock supply for the Deschutes and the next generation processor applications.

Components that need to be modified to make the dual layout work for US3018 and HIP6018.

Part #	R11	R18	C9	C11	C12	C19	C20
HIP6018	O	V	O	V	V	O	V
US3018	S	O	V	O	O	V	O

S - Short, O - Open, V - See Unisem or Harris parts list for the value.

Table 2 - Dual layout component table

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US3018 Application Parts List Dual Layout with HIP6018

Ref Desig	Description	Qty	Part #	Manuf
Q2	MOSFET	1	IRLR024, TO252 package	IR
Q3	MOSFET	1	IRL3103S, TO263 package	IR
Q4	MOSFET with Schottky	1	IRL3103D1S, TO263 package	IR
L1	Inductor	1	L=1uH, 5052 core with 4 turns of 1.0mm wire	Micro Metal
L3	Inductor	1	L=2.7uH, 5052B core with 7 turns of 1.2mm wire	Micro Metal
C1,17	Capacitor, Electrolytic	2	6MV1000GX, 1000uF,6.3V	Sanyo
C2	Capacitor, Electrolytic	1	10MV470GX, 470uF,10V	Sanyo
C3	Capacitor, Electrolytic	1	10MV1200GX, 1200uF,10V	Sanyo
C8	Capacitor, Ceramic	1	1uF, 0805	
C9,15,19	Capacitor, Ceramic	3	1uF, 0603	
C10	Capacitor, Ceramic	1	220pF, 0603	
C11,12,20	Capacitor, Ceramic	3	See Table 2, dual layout component 0603 * 3	
C13	Capacitor, Ceramic	1	1000pF, 0603	
C14	Capacitor, Electrolytic	2	10MV1200GX, 1200uF,10V	Sanyo
C16	Capacitor, Electrolytic	6	6MV1500GX, 1500uF,6.3V,	Sanyo
C18	Capacitor, Electrolytic	1	6MV150GX, 150uF,6.3V	Sanyo
R5	Resistor	1	19.1Ω, 1%, 0603	
R6,7,8	Resistor	3	100Ω, 1%, 0603	
R11	Resistor	1	0Ω, 0603	
R12	Resistor	1	3.3kΩ, 5%, 0603	
R13,14,15	Resistor	3	4.7Ω, 5%, 1206	
R16,17,21	Resistor	3	2.2kΩ, 1%, 0603	
R18	Resistor	1	See Table 2, dual layout component 0603 * 1	
R19	Resistor	1	220kΩ, 1%, 0603	
R22	Resistor	1	10Ω, 5%, 0603	

Application Information

An example of how to calculate the components for the application circuit is given below.

Assuming, two set of output conditions that this regulator must meet for Vcore :

a) Vo=2.8V , Io=14.2A, ΔVo=185mV, ΔIo=14.2A

b) Vo=2V , Io=14.2A, ΔVo=140mV, ΔIo=14.2A

The regulator design will be done such that it meets the worst case requirement of each condition.

Output Capacitor Selection

The first step is to select the output capacitor. This is done primarily by selecting the maximum ESR value that meets the transient voltage budget of the total ΔVo specification. Assuming that the regulators DC initial accuracy plus the output ripple is 2% of the output voltage, then the maximum ESR of the output capacitor is calculated as :

$$ESR \leq \frac{100}{14.2} = 7 \text{ m}\Omega$$

The Sanyo MVGX series is a good choice to achieve both the price and performance goals. The 6MV1500GX , 1500uF, 6.3V has an ESR of less than 36 mΩ typ . Selecting 6 of these capacitors in parallel has an ESR of ≈6 mΩ which achieves our low ESR goal.

Other type of Electrolytic capacitors from other manufacturers to consider are the Panasonic “FA” series or the Nichicon “PL” series.

Reducing the Output Capacitors Using Voltage Level Shifting Technique

The trace resistance or an external resistor from the output of the switching regulator to the Slot 1 can be used to the circuit advantage and possibly **reduce the number of output capacitors, by level shifting the DC regulation point when transitioning from light load to full load and vice versa**. To accomplish this, the output of the regulator is typically set about half the DC drop that results from light load to full load. For example, if the total resistance from the output capacitors to the Slot 1 and back to the GND pin of the 3018 is 5mΩ and if the total ΔI, the change from light load to full load is 14A, then the output voltage measured at the top of the resistor divider which is also connected to the output capacitors in this case, must be set at half of the 70 mV or 35mV higher than the DAC voltage setting. This intentional voltage level shifting during the load transient

eases the requirement for the output capacitor ESR at the cost of load regulation. One can show that the new ESR requirement eases up by **half the total trace resistance**. For example, if the ESR requirement of the output capacitors without voltage level shifting must be 7mΩ then after level shifting the new ESR will only need to be 8.5mΩ if the trace resistance is 5mΩ (7+5/2=9.5). However, one must be careful that the combined “voltage level shifting” and the transient response is still within the maximum tolerance of the Intel specification. To insure this, the maximum trace resistance must be less than:

$$R_s \leq 2(V_{spec} - 0.02 * V_o - \Delta V_o) / \Delta I$$

Where :

Rs=Total maximum trace resistance allowed

Vspec=Intel total voltage spec

Vo=Output voltage

ΔVo=Output ripple voltage

ΔI=load current step

For example, assuming:

Vspec=±140 mV=±0.1V for 2V output

Vo=2V

ΔVo=assume 10mV=0.01V

ΔI=14.2A

Then the Rs is calculated to be:

$$R_s \leq 2(0.140 - 0.02 * 2 - 0.01) / 14.2 = 12.6 \text{ m}\Omega$$

However, if a resistor of this value is used, the maximum power dissipated in the trace (or if an external resistor is being used) must also be considered. For example if Rs=12.6 mΩ , the power dissipated is (Io^2)*Rs=(14.2^2)*12.6=2.54W. This is a lot of power to be dissipated in a system. So, if the Rs=5mΩ, then the power dissipated is about 1W which is much more acceptable. If level shifting is not implemented, then the maximum output capacitor ESR was shown previously to be 7mΩ which translated to ≈ 6 of the 1500uF, 6MV1500GX type Sanyo capacitors. With Rs=5mΩ, the maximum ESR becomes 9.5mΩ which is equivalent to ≈ 4 caps. Another important consideration is that **if a trace is being used to implement the resistor, the power dissipated by the trace increases the case temperature of the output capacitors which could seriously effect the life time of the output capacitors**.

Output Inductor Selection

The output inductance must be selected such that under low line and the maximum output voltage condition, the inductor current slope times the output capacitor ESR is ramping up faster than the capacitor voltage is drooping during a load current step.

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However if the inductor is too small, the output ripple current and ripple voltage become too large. One solution to bring the ripple current down is to increase the switching frequency, however that will be at the cost of reduced efficiency and higher system cost. The following set of formulas are derived to achieve the optimum performance without many design iterations. The maximum output inductance is calculated using the following equation:

$$L = ESR * C * (V_{in\ min} - V_{om\ ax}) / (2 * \Delta I)$$

Where:

$V_{in\ min}$ = Minimum input voltage

For $V_o = 2.8\text{ V}$, $\Delta I = 14.2\text{ A}$

$$L = 0.006 * 9000 * (4.75 - 2.8) / (2 * 14.2) = 3.7\ \mu\text{H}$$

Assuming that the programmed switching frequency is set at 200 KHZ, an inductor is designed using the Micrometals' powder iron core material. The summary of the design is outlined below:

The selected core material is Powder Iron, the selected core is T50-52D from Micro Metal wounded with 8 Turns of # 16 AWG wire, resulting in 3 uH inductance with $\approx 3\text{ m}\Omega$ of DC resistance.

Assuming $L = 3\ \mu\text{H}$ and the switching frequency; $F_{sw} = 200\text{ KHZ}$, the inductor ripple current and the output ripple voltage is calculated using the following set of equations:

$$T = 1 / F_{sw}$$

$T \equiv$ Switching Period

$$D \approx (V_o + V_{sync}) / (V_{in} - V_{sw} + V_{sync})$$

$D \equiv$ Duty Cycle

$$T_{on} = D * T$$

$V_{sw} \equiv$ High side Mosfet ON Voltage = $I_o * R_{ds}$

$R_{ds} \equiv$ Mosfet On Resistance

$$T_{off} = T - T_{on}$$

$V_{sync} \equiv$ Synchronous MOSFET ON Voltage = $I_o * R_{ds}$

$$\Delta I_r = (V_o + V_{sync}) * T_{off} / L$$

$\Delta I_r \equiv$ Inductor Ripple Current

$$\Delta V_o = \Delta I_r * ESR$$

$\Delta V_o \equiv$ Output Ripple Voltage

In our example for $V_o = 2.8\text{V}$ and 14.2 A load, Assuming IRL3103 MOSFET for both switches with maximum on resistance of $19\text{ m}\Omega$, we have:

$$T = 1 / 200000 = 5\ \mu\text{Sec}$$

$$V_{sw} = V_{sync} = 14.2 * 0.019 = 0.27\text{ V}$$

$$D \approx (2.8 + 0.27) / (5 - 0.27 + 0.27) = 0.61$$

$$T_{on} = 0.61 * 5 = 3.1\ \mu\text{Sec}$$

$$T_{off} = 5 - 3.1 = 1.9\ \mu\text{Sec}$$

$$\Delta I_r = (2.8 + 0.27) * 1.9 / 3 = 1.94\text{ A}$$

$$\Delta V_o = 1.94 * .006 = .011\text{ V} = 11\text{ mV}$$

Power Component Selection

Assuming IRL3103 MOSFETs as power components, we will calculate the maximum power dissipation as follows:

For high side switch the maximum power dissipation happens at maximum V_o and maximum duty cycle.

$$D_{max} \approx (2.8 + 0.27) / (4.75 - 0.27 + 0.27) = 0.65$$

$$P_{dh} = D_{max} * I_o^2 * R_{ds(max)}$$

$$= 0.65 * 14.2^2 * 0.029 = 3.8\text{ W}$$

$R_{ds(max)}$ = Maximum R_{ds-on} of the MOSFET at 125°C

For synch MOSFET, maximum power dissipation happens at minimum V_o and minimum duty cycle.

$$D_{min} \approx (2 + 0.27) / (5.25 - 0.27 + 0.27) = 0.43$$

$$P_{ds} = (1 - D_{min}) * I_o^2 * R_{ds(max)}$$

$$= (1 - 0.43) * 14.2^2 * 0.029 = 3.33\text{ W}$$

Heatsink Selection

Selection of the heat sink is based on the maximum allowable junction temperature of the MOSFETs. Since we previously selected the maximum R_{ds-on} at 125°C , then we must keep the junction below this temperature. Selecting TO220 package gives $\theta_{jc} = 1.8^\circ\text{C/W}$ (From the vendors' datasheet) and assuming that the selected heatsink is Black Anodized, the Heat sink to Case thermal resistance is; $\theta_{cs} = 0.05^\circ\text{C/W}$, the maximum heat sink temperature is then calculated as:

$$T_s = T_j - P_d * (\theta_{jc} + \theta_{cs})$$

$$T_s = 125 - 3.82 * (1.8 + 0.05) = 118^\circ\text{C}$$

With the maximum heat sink temperature calculated in the previous step, the Heat Sink to Air thermal resistance (θ_{sa}) is calculated as follows:

Assuming $T_a = 35^\circ\text{C}$

$$\Delta T = T_s - T_a = 118 - 35 = 83^\circ\text{C} \quad \text{Temperature Rise Above Ambient}$$

$$\theta_{sa} = \Delta T / P_d$$

$$\theta_{sa} = 83 / 3.82 = 22^\circ\text{C/W}$$

Next, a heat sink with lower θ_{sa} than the one calculated in the previous step must be selected. One way to do this is to simply look at the graphs of the "Heat Sink Temp Rise Above the Ambient" vs. the "Power Dissipation" given in the heatsink manufacturers' catalog and select a heat sink that results in lower temperature rise than the one calculated in previous step. The following heat sinks from AAVID and Thermalloy meet this criteria.

Co.	Part #
Thermalloy	6078B
AAVID	577002

Following the same procedure for the Schottky diode results in a heatsink with $\theta_{sa} = 25 \text{ }^\circ\text{C/W}$. Although it is possible to select a slightly smaller heatsink, for simplicity the same heatsink as the one for the high side MOSFET is also selected for the synchronous MOSFET.

Switcher Current Limit Protection

The US3018 uses the MOSFET R_{ds-on} as the sensing resistor to sense the MOSFET current and compares to a programmed voltage which is set externally via a resistor (R_{cs}) placed between the drain of the MOSFET and the "CS+" terminal of the IC as shown in the application circuit. For example, if the desired current limit point is set to be 22A for the synchronous and 16A for the non synchronous, and from our previous selection, the maximum MOSFET $R_{ds-on}=19\text{m}\Omega$, then the current sense resistor R_{cs} is calculated as :

$$V_{cs}=I_{cL}*R_{ds}=22*0.019=0.418\text{V}$$

$$R_{cs}=V_{cs}/I_b=(0.418\text{V})/(200\mu\text{A})=2.1\text{k}\Omega$$

Where: $I_b=200\mu\text{A}$ is the internal current setting of the US3018

Switcher Frequency Selection

The US3018 frequency is internally set at 200kHz with no external timing resistor. However, it can be adjusted up by using an external resistor from R_t pin to GND or can be adjusted down if the resistor is connected to the 12V supply.

1.5V, GTL+ Supply LDO Power MOSFET Selection

The first step in selecting the power MOSFET for the 1.5V linear regulator is to select its maximum R_{ds-on} of the pass transistor based on the input to output Dropout voltage and the maximum load current.

$$R_{ds(max)}=(V_{in} - V_o)/I_L$$

$$\text{For } V_o=1.5\text{V, and } V_{in}=3.3\text{V, } I_L=2\text{A}$$

$$R_{ds-max}=(3.3 - 1.5)/2=0.9\Omega$$

Note that since the MOSFETs R_{ds-on} increases with temperature, this number must be divided by ≈ 1.5 , in order to find the R_{ds-on} max at room temperature. The Motorola MTP3055VL has a maximum of 0.18Ω R_{ds-on} at room temperature, which meets our requirement.

To select the heatsink for the LDO Mosfet the first step is to calculate the maximum power dissipation of the device and then follow the same procedure as for the switcher.

$$P_d = (V_{in} - V_o) * I_L$$

Where :

P_d = Power Dissipation of the Linear Regulator

I_L = Linear Regulator Load Current

For the 1.5V and 2A load:

$$P_d = (3.3 - 1.5)*2=3.6 \text{ W}$$

Assuming $T_j\text{-max}=125^\circ\text{C}$

$$T_s = T_j - P_d * (\theta_{jc} + \theta_{cs})$$

$$T_s = 125 - 3.6 * (1.8 + 0.05) = 118 \text{ }^\circ\text{C}$$

With the maximum heat sink temperature calculated in the previous step, the Heat Sink to Air thermal resistance (θ_{sa}) is calculated as follows :

Assuming $T_a=35^\circ\text{C}$

$$\Delta T = T_s - T_a = 118 - 35 = 83 \text{ }^\circ\text{C} \quad \text{Temperature Rise Above Ambient}$$

$$\theta_{sa} = \Delta T/P_d$$

$$\theta_{sa} = 83 / 3.6 = 23 \text{ }^\circ\text{C/W}$$

The same heat sink as the one selected for the switcher MOSFETs is also suitable for the 1.5V regulator.

2.5V, Clock Supply

The US3018 provides an internal **ultra low dropout regulator with a minimum of 200mA** current capability that converts 3.3V supply to a programmable regulated 2.5V supply to power the clock chip. The internal regulator has short circuit protection with internal thermal shutdown.

1.5V and 2.5V Supply Resistor Divider Selection

Since the internal voltage reference for the linear regulators is set at 1.26V for US3018, there is a need to use external resistor dividers to step up the voltage. The resistor dividers are selected using the following equations:

$$V_o=(1+R_t/R_b)*V_{ref}$$

Where:

R_t =Top resistor divider

R_b =Bottom resistor divider

$V_{ref}=1.26\text{V}$ typical

For 1.5V supply :

Assuming $R_b=100\Omega$

$$R_t=R_b*[(V_o/V_{ref}) - 1]$$

$$R_t=100*[(1.5/1.26) - 1]=19.1\Omega$$

For 2.5V supply :

Assuming $R_b=200\Omega$

$$R_t=R_b*[(V_o/V_{ref}) - 1]$$

$$R_t=200*[(2.5/1.26) - 1]=197\Omega$$

Select $R_t=200\Omega$

Switcher Output Voltage Adjust

As it was discussed earlier, the trace resistance from the output of the switching regulator to the Slot 1 can be used to the circuit advantage and possibly reduce the number of output capacitors, by level shifting the DC

regulation point when transitioning from light load to full load and vice versa. To account for the DC drop, the output of the regulator is typically set about half the DC drop that results from light load to full load. For example, if the total resistance from the output capacitors to the Slot 1 and back to the GND pin of the 3018 is $5\text{m}\Omega$ and if the total ΔI , the change from light load to full load is 14A, then the output voltage measured at the top of the resistor divider which is also connected to the output capacitors in this case, must be set at half of the 70 mV or 35mV higher than the DAC voltage setting. To do this, the top resistor of the resistor divider (R17 in the application circuit) is set at 100Ω , and the R19 is calculated. For example, if DAC voltage setting is for 2.8V and the desired output under light load is 2.835V, then R19 is calculated using the following formula :

$$R19 = 100 \cdot \left\{ \frac{V_{\text{dac}}}{(V_o - 1.004 \cdot V_{\text{dac}})} \right\} \quad [\Omega]$$

$$R19 = 100 \cdot \left\{ \frac{2.8}{(2.835 - 1.004 \cdot 2.800)} \right\} = 11.76 \text{ k}\Omega$$

Select 11.8 k Ω , 1%

Note: The value of the top resistor must not exceed 100 Ω . The bottom resistor can then be adjusted to raise the output voltage.

Soft Start Capacitor Selection

The soft start capacitor must be selected such that during the start up when the output capacitors are charging

limit threshold. A minimum of 1 μF capacitor insures this for most applications. An internal resistor charges the soft start capacitor which slowly ramps up the inverting

cap thereby limiting the input current. For example, with 1 μF of soft start capacitor, the ramp up rate is approximated to be 1V/20mS. For example if the output capacitance is 9000 μF , the maximum start up current will be:

$$I = 9000\mu\text{F} \cdot (1\text{V}/20\text{mS}) = 0.45\text{A}$$

The other function of the soft start cap is to provide an off time between the current limit cycles (HICCUP) in order for the synchronous MOSFET to cool off and survive the short circuit condition. The off time between the current limit cycles is approximated as:

$$T(\text{hicup}) = 60 \cdot C_{\text{ss}} \quad (\text{mS})$$

Input Filter

It is highly recommended to place an inductor between the system 5V supply and the input capacitors of the switching regulator to isolate the 5V supply from the switching noise that occurs during the turn on and off of the switching components. Typically an inductor in the range of 1 to 3 μH will be sufficient in this type of application.

External Shutdown

The best way to shutdown the US3018 is to pull down on the soft start pin using an external small signal transistor such as 2N3904 or 2N7002 small signal MOSFET. This allows slow ramp up of the output, the same as the power up.

Layout Considerations

Switching regulators require careful attention to the layout of the components, specifically power components since they switch large currents. These switching components can create large amount of voltage spikes and high frequency harmonics if some of the critical components are far away from each other and are connected with inductive traces. The following is a guideline of how to place the critical components and the connections between them in order to minimize the above issues. Start the layout by first placing the power components:

- 1) Place the input capacitor C14 and the high side mosfet, Q3 as close to each other as possible.
- 2) Place the synchronous mosfet, Q4 and the Q3 as close to each other as possible with the intention that the source of Q3 and drain of the Q4 has the shortest length.
- 3) Place the snubber R15 & C13 between Q4 & Q3.
- 4) Place the output inductor, L3 and the output capacitors, C16 between the mosfet and the load with output capacitors distributed along the slot 1 and close to it.
- 5) Place the bypass capacitors, C8 and C19 right next to 12V and 5V pins. C8 next to the 12V, pin 1 and C19 next to the 5V, pin 8.
- 6) Place the US3018 such that the pwm output drives, pins 24 and 22 are relatively short distance from gates of Q3 and Q4.
- 7) Place all resistor dividers close to their respective feedback pins.

8) Place the 2.5V output capacitor, C18 close to the pin13 of the IC and the 1.5V output capacitor, C17 close to the Q2 MOSFET. Note: It is better to place the 1.5V linear regulator components close to the 3018 and then run a trace from the output of the regulator to the load. However, if this is not possible then the trace from the linear drive output pin, pin 16 **must be run away from any high frequency data signals.**

It is critical, to place high frequency ceramic capacitors close to the clock chip and termination resistors to provide local bypassing.

9) Place R12 and C10 close to pin 20.

10) Place C9 close to pin 9.

Component connections:

Note : It is extremely important that no data bus should be passing through the switching regulator section specifically close to the fast transition nodes such as PWM drives or the inductor voltage.

Using the 4 layer board, dedicate on layer to GND, another layer as the power layer for the 5V, 3.3V, Vcore, 1.5V and if it is possible for the 2.5V.

Connect all grounds to the ground plane using direct vias to the ground plane.

Use large low inductance/low impedance plane to connect the following connections either using component side or the solder side.

- a) C14 to Q3 Drain
- b) Q3 Source to Q4 Drain
- c) Q4 drain to L3
- d) L3 to the output capacitors, C16
- e) C16 to the load, slot 1
- f) Input filter L1 to the C16 and C3
- g) C1 to Q2 drain
- h) C17 to the Q2 source
- i) A minimum of 0.2 inch width trace from the C18 capacitor to pin 13

Connect the rest of the components using the shortest connection possible

TYPICAL APPLICATION (Dual Layout with HIP6016)

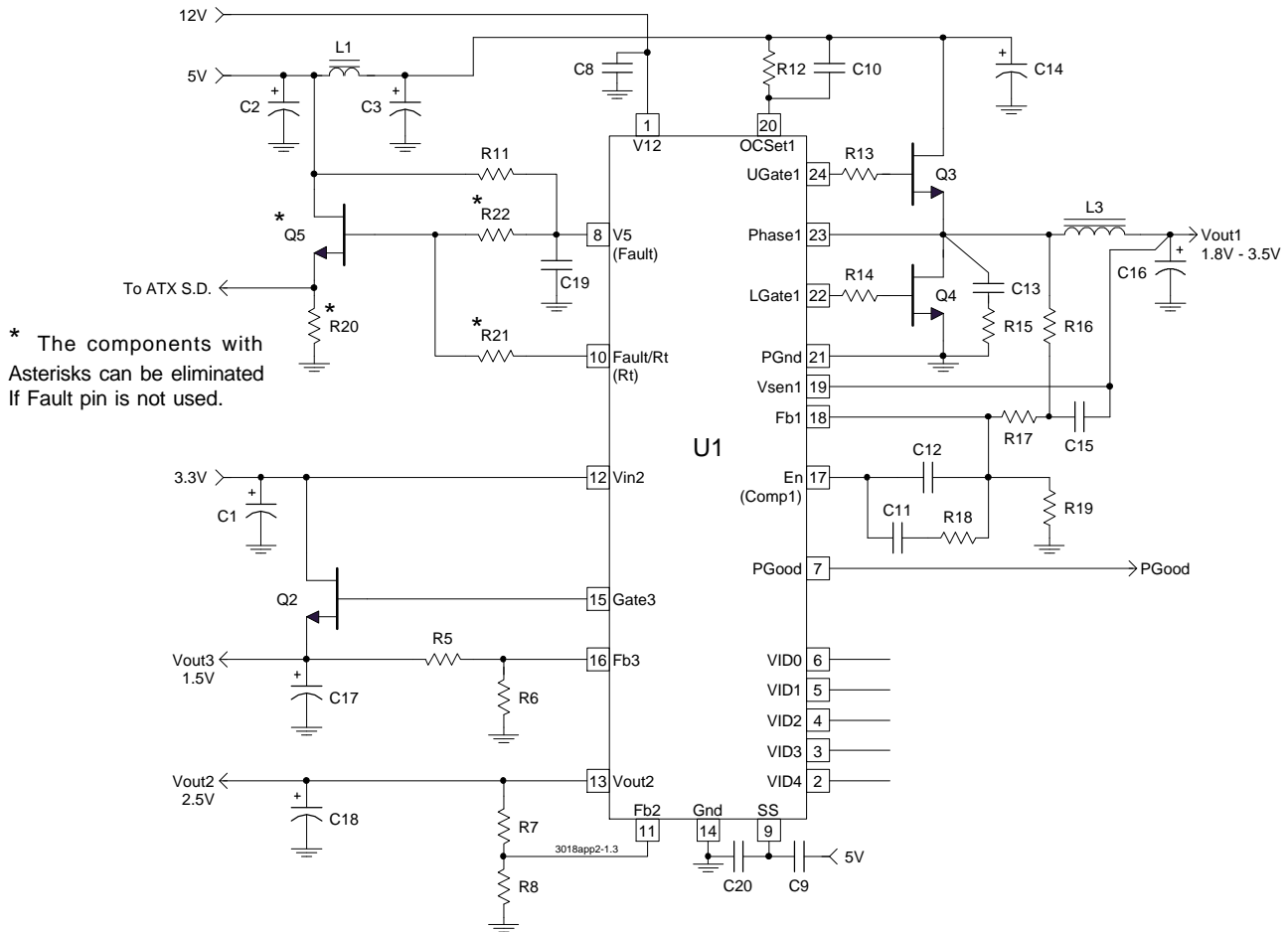


Figure 3 - Typical application of US3018 in a dual layout with HIP6016 for an on board DC-DC converter providing power for the Vcore , GTL+ & Clock supply for the Deschutes and the next generation processor applications.

Components that need to be modified to make the dual layout work for US3018 and HIP6016.

Part #	R5,R7,R11,R21	R6,R8,R16,R18,C11,C12,C20	R22	C9,C19	C15
HIP6016	O	V	S	O	V
US3018	S	O	O	V	S

S - Short O - Open V - See Unisem or Harris parts list for the value.

Table 2 - Dual layout component table

**US3018 Application Parts List
Dual Layout with HIP6016**

Ref Desig	Description	Qty	Part #	Manuf
Q3,4	MOSFET	2	IRL3103 IRL3103S (Note 1)	IR
Q5	MOSFET, GP	1	2N7002	MOT
Q2	MOSFET	1	MTP3055VL, TO263 package	MOT
L1	Inductor	1	L=1 uH	
L3	Inductor	1	Core :L=2 uH R=2 mohm	Micro Metal
C16	Capacitor ,Electrolytic	6	6MV1500GX ,1500uF,6.3V,	Sanyo
C14	Capacitor ,Electrolytic	2	6MV1500GX ,1500uF,6.3V,	Sanyo
C3	Capacitor ,Electrolytic	1	6MV1500GX ,1500uF,6.3V,	Sanyo
C18	Capacitor ,Electrolytic	1	220uF , 6.3V, ECAOJFQ221	Panasonic
C17,C1	Capacitor ,Electrolytic	2	680uF,10V, EEUFA1A681L	Panasonic
C2	Capacitor ,Electrolytic	1	680uF,10V, EEUFA1A681L	Panasonic
C8,19	Capacitor , Ceramic	2	0805Z105P250NT 1uF,25V,Z5U,0805 smt	Novacap
C9	Capacitor , Ceramic	1	0805Z105P250NT 1uF,25V,Z5U,0805 smt See Table 2, dual layout component	Novacap
C10	Capacitor , Ceramic	1	220pF, SMT 0805 size	
C13	Capacitor , Ceramic	1	470pF, SMT 0805 size	
C9,11, 12,15,20			See Table 2, dual layout component	
R12	Resistor	1	2.21k Ω ,1%, SMT 0805 size	
R13,14	Resistor	2	10 Ω , 5%, SMT 1206 size	
R15	Resistor	1	10 Ω , 5%, SMT 1206 size	
R20	Resistor	1	10k Ω , 5%, SMT 0805 size	
R6	Resistor	1	100 Ω , 1%, SMT 0805 size	
R8	Resistor	1	200 Ω , 1%, SMT 0805 size	
R5	Resistor	1	19.1 Ω , 1%, SMT 0805 size	
R7	Resistor	1	200 Ω , 1%, SMT 0805 size	
R17	Resistor	1	100 Ω , 1%, SMT 0805 size	
R19	Resistor	1	10k Ω , 1%, SMT 0805 size	
R11 16,18, 21,22			See Table 2, dual layout component	
HS3,4	Q1,3,4 Heatsink	2	6270	Thermalloy

Note 1 : For the applications where it is desirable not to use the Heatsink, the IRL3103S MOSFET in the TO263 SMT package with 1" square of pad area using top and bottom layers of the board as a minimum is required.