

QUADRATURE CLOCK CONVERTER

October 2000

FEATURES:

- x1, x2 and x4 mode selection
- Up to 16 MHz output clock frequency
- INDEX input and output
- UP/DOWN indicator output
- Programmable output clock pulse width
- On-chip filtering of inputs for optical or magnetic encoder applications.
- TTL and CMOS compatible I/Os
- +4.5V to +10.0V operation (VDD-VSS)
- LS7082 (DIP), LS7082-S (SOIC) - See Figure 1

DESCRIPTION:

The LS7082 is a monolithic CMOS silicon gate quadrature clock converter. Quadrature clocks derived from optical or magnetic encoders, when applied to the A and B Inputs of the LS7082, are converted to strings of Up Clocks and Down Clocks. Pulses derived from the Index Track of an encoder, when applied to the INDX input, produce absolute position reference pulses which are synchronized to the Up Clocks and Down Clocks. These outputs can be interfaced directly with standard Up/Down counters for direction and position sensing of the encoder.

INPUT/OUTPUT DESCRIPTION:

VDD (Pin 1)

Supply Voltage positive terminal.

INDX (Pin 2)

Encoder Index pulses are applied to this input.

RBIAS (Pin 3)

Input for external component connection. A resistor connected between this input and Vss adjusts the output clock pulse width (Tow). For proper operation, the output clock pulse width must be less than or equal to the A,B pulse separation (Tow - TPs).

Vss (Pin 4)

Supply Voltage negative terminal.

A (Pin 5)

Quadrature Clock Input A. This input has a filter circuit to validate input logic level and eliminate encoder dither.

x2 (Pin 8)

A low level applied to this input selects x2 mode of operation. See Table 1 for Mode Selection Truth Table and Figure 2 for Input/Output timing relationship.

B (Pin 9)

Quadrature Clock Input B. This input has a filter circuit identical to input A.

PIN ASSIGNMENT - TOP VIEW

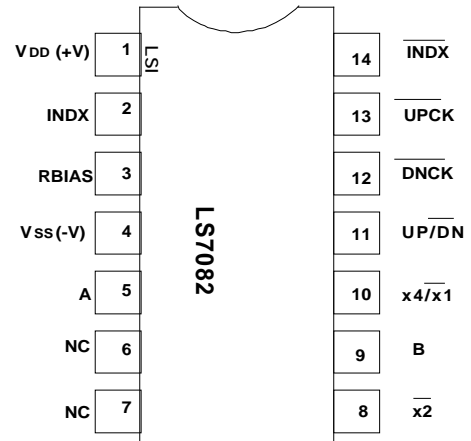


FIGURE 1

TABLE 1. MODE SELECTION TRUTH TABLE

x2 Input	x4/x1 Input	MODE
0	Don't Care	x2
1	0	x1
1	1	x4

x4/x1 (Pin 10)

This input selects between x1 and x4 modes of operation. See Table 1 for Mode Selection Truth Table and Figure 2 for Input/Output timing relationship.

UP/DN (Pin 11)

The count direction at any instant is indicated at this output. An UP count direction is indicated by a high, and a DOWN count direction is indicated by a low (See Figure 2).

DNCK (Pin 12)

This DOWN Clock output consists of low-going pulses generated when A input lags the B input (See Figure 2).

UPCK (Pin 13)

This UP Clock output consists of low-going pulses generated when A input leads the B input (See Figure 2).

INDX (Pin 14)

This output consists of low-going pulses generated by clock transitions at the A input when INDX input is high and B input is low (See Figure 2).

NOTE: All unused input pins must be tied to VDD or VSS.

ABSOLUTE MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNITS
DC Supply Voltage	V _{DD} - V _{SS}	11.0	V
Voltage at any input	V _{IN}	V _{SS} - 3 to V _{DD} + 3	V
Operating temperature	T _A	0 to +70	°C
Storage temperature	T _{STG}	-55 to +150	°C

DC ELECTRICAL CHARACTERISTICS:(All voltages referenced to V_{SS}, T_A = 0°C to 70°C.)

PARAMETER	SYMBOL	MIN	MAX	UNITS	CONDITION
Supply voltage	V _{DD}	4.5	10.0	V	-
Supply current	I _{DD}	-	6.0	μA	V _{DD} = 10.0V, All input frequencies = 0 Hz RBIAS = 2M
x4/x1, x2, INDx Logic Low	V _{IL}	-	0.3V _{DD}	V	-
A,B Logic Low	V _{IL}	-	0.6	V	V _{DD} = 4.5V
		-	1.0	V	V _{DD} = 9V
		-	1.1	V	V _{DD} = 10.0V
x4/x1, x2, INDx Logic High	V _{IH}	0.7V _{DD}	-	V	-
A,B Logic High	V _{IH}	3.1	-	V	V _{DD} = 4.5V
		5.0	-	V	V _{DD} = 9V
		5.6	-	V	V _{DD} = 10.0V
ALL OUTPUTS:					
Sink Current	I _{OL}	1.75	-	mA	V _{DD} = 4.5V
V _{OL} = 0.4V		5.0	-	mA	V _{DD} = 9V
		5.7	-	mA	V _{DD} = 10.0V
Source Current	I _{OH}	1.0	-	mA	V _{DD} = 4.5V
V _{OH} = V _{DD} - 0.5V		2.5	-	mA	V _{DD} = 9V
		3.0	-	mA	V _{DD} = 10.0V

TRANSIENT CHARACTERISTICS:(T_A = 0°C to 70°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	CONDITION
A,B inputs:					
Validation Delay	T _{VD}	-	85	ns	V _{DD} = 10.0V
		-	100	ns	V _{DD} = 9V
		-	160	ns	V _{DD} = 4.5V
A,B inputs:					
Pulse Width	T _{PW}	T _{VD} +T _{OW}	Infinite	ns	-
A to B or B to A					
Phase Delay	T _{PS}	T _{OW}	Infinite	ns	-
A,B frequency	f _{A,B}	-	$\frac{1}{2T_{PW}}$	Hz	-
Input to Output Delay	T _{DS}	-	120	ns	V _{DD} = 10.0V
		-	150	ns	V _{DD} = 9V
		-	235	ns	V _{DD} = 4.5V Includes input validation delay
Output Clock Pulse Width	T _{OW}	50	-	ns	See Fig. 4 & 5

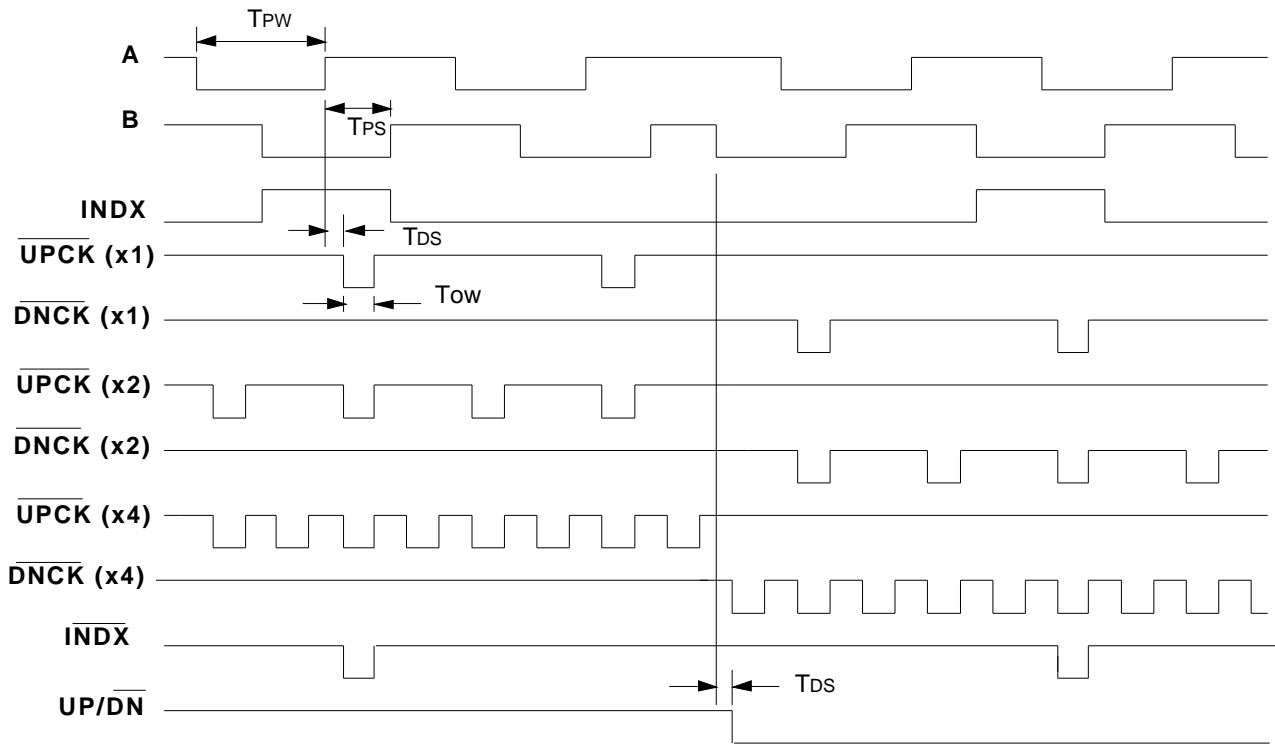


FIGURE 2. LS7082 INPUT/OUTPUT TIMING DIAGRAM

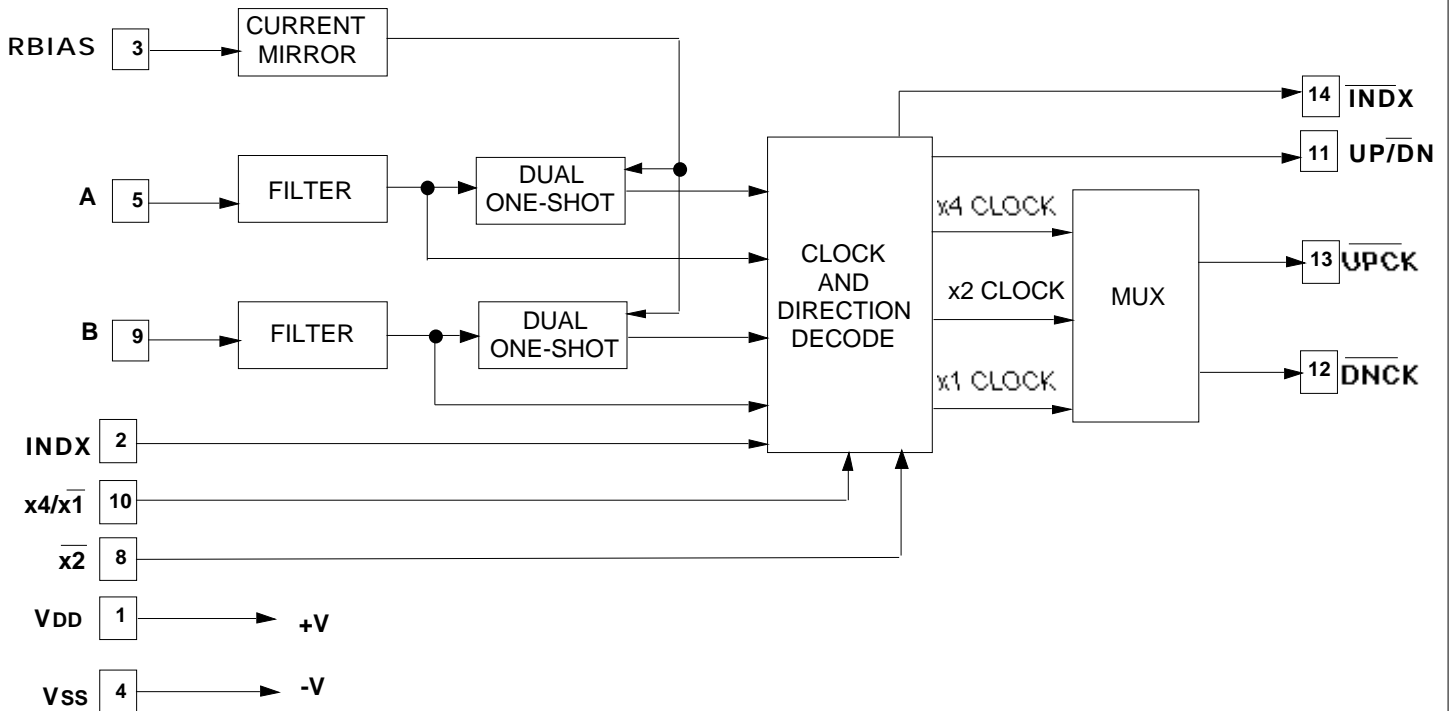


FIGURE 3. LS7082 BLOCK DIAGRAM

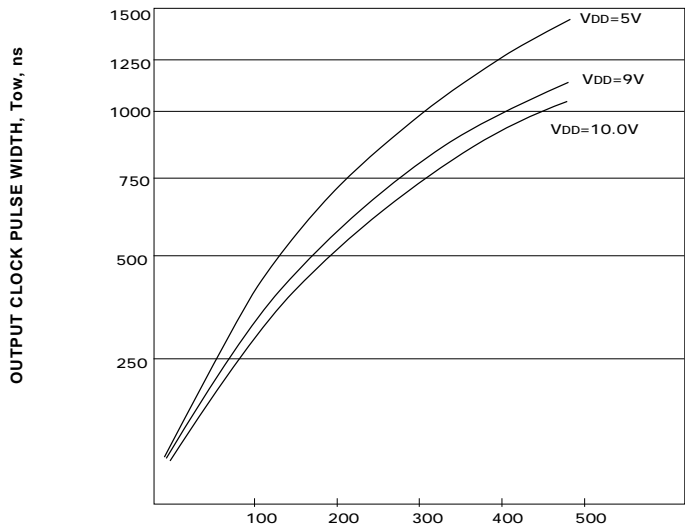


Figure 4. Tow vs RBIAS, KΩ

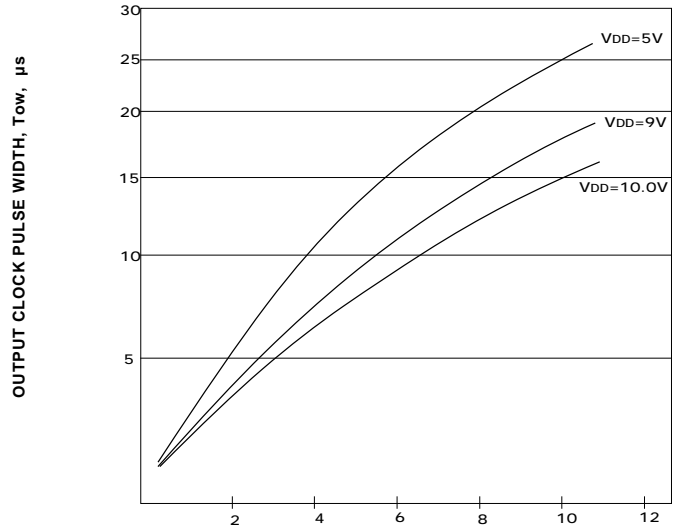


Figure 5. Tow vs RBIAS, MΩ

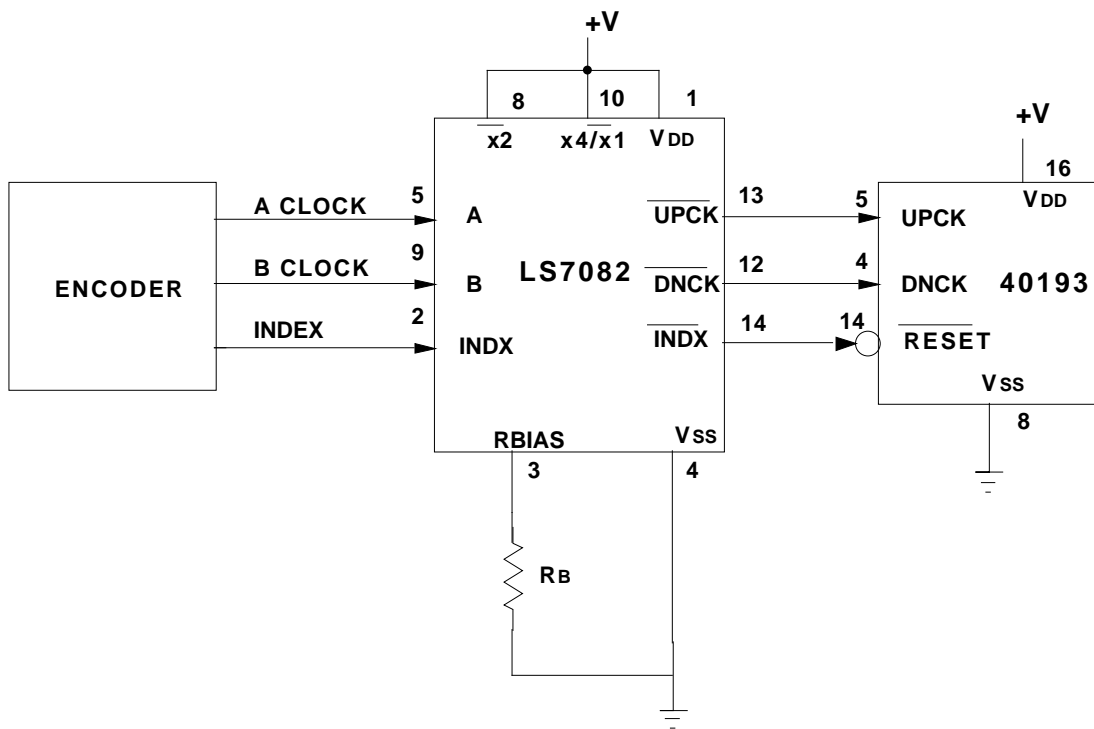


FIGURE 6. A TYPICAL APPLICATION IN x4 MODE

The information included herein is believed to be accurate and reliable. However, LSI Computer Systems, Inc. assumes no responsibilities for inaccuracies, nor for any infringements of patent rights of others which may result from its use.