UT54ACS165/UT54ACTS165

Radiation-Hardened
8-Bit Parallel Shift Registers

FEATURES

- Complementary outputs
- Direct overriding load (data) inputs
- Gated clock inputs
- Parallel-to-serial data conversions
- 1.2µ radiation-hardened CMOS
  - Latchup immune
- High speed
- Low power consumption
- Single 5 volt supply
- Available QML Q or V processes
- Flexible package
  - 16-pin DIP
  - 16-lead flatpack

DESCRIPTION

The UT54ACS165 and the UT54ACTS165 are 8-bit serial shift registers that, when clocked, shift the data toward serial output Q_H. Parallel-in access to each stage is provided by eight individual data inputs that are enabled by a low level at the SH/$\overline{LD}$ input. The devices feature a clock inhibit function and a complemented serial output $\overline{Q}_H$.

Clocking is accomplished by a low-to-high transition of the CLK input while SH/$\overline{LD}$ is held high and CLK INH is held low. The functions of the CLK and CLK INH (clock inhibit) inputs are interchangeable. Since a low CLK input and a low-to-high transition of CLK INH will also accomplish clocking, CLK INH should be changed to the high level only while the CLK input is high. Parallel loading is disabled when SH/$\overline{LD}$ is held high. Parallel inputs to the registers are enabled while SH/$\overline{LD}$ is low independently of the levels of CLK, CLK INH or SER inputs.

The devices are characterized over full military temperature range of -55°C to +125°C.

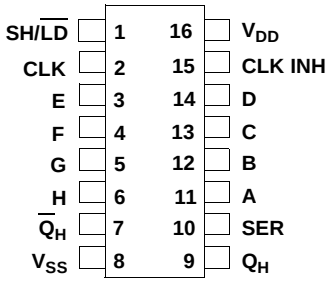
FUNCTION TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUTS	
SH/$\overline{LD}$	CLK INH	CLK	SER	PARALLEL A . . . H	$\overline{Q}_A$	$\overline{Q}_B$	Q_H	$\overline{Q}_H$
L	X	X	X	a . . . h	a	b	h	$\overline{h}$
H	L	L	X	X	Q_A	Q_B	Q_H	$\overline{Q}_H$
H	L	↑	H	X	H	Q_A	Q_G	$\overline{Q}_G$
H	L	↑	L	X	L	Q_A	Q_G	$\overline{Q}_G$
H	H	X	X	X	Q_A	Q_B	Q_H	$\overline{Q}_H$

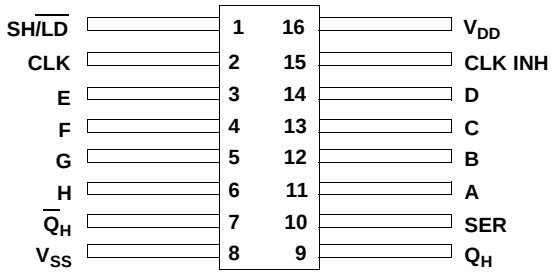
Note:
1. Q_n = The state of the referenced output one setup time prior to the Low-to-High clock transition.

PINOUTS

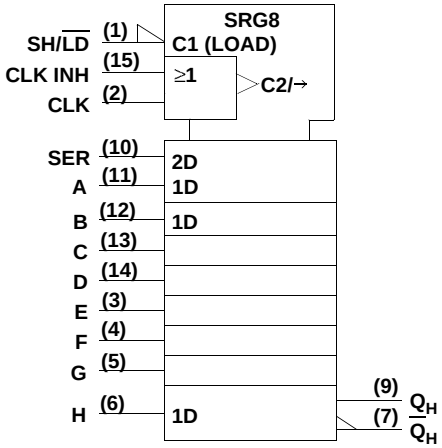
16-Pin DIP
Top View



16-Lead Flatpack
Top View

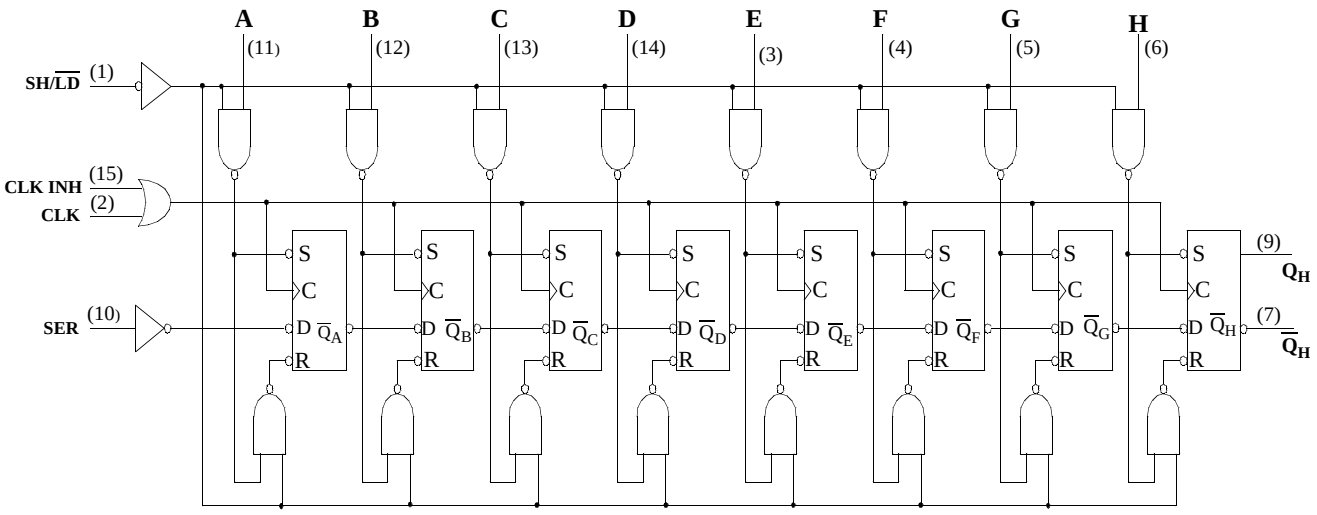


LOGIC SYMBOL



Note:
1. Logic symbol in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM



RADIATION HARDNESS SPECIFICATIONS [1]

PARAMETER	LIMIT	UNITS
Total Dose	1.0E6	rads(Si)
SEU Threshold [2]	80	MeV-cm^2/mg
SEL Threshold	120	MeV-cm^2/mg
Neutron Fluence	1.0E14	n/cm^2

Notes:
1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Device storage elements are immune to SEU affects.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD}	Supply voltage	-0.3 to 7.0	V
$V_{I/O}$	Voltage any pin	-.3 to V_{DD} +.3	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
T_{LS}	Lead temperature (soldering 5 seconds)	+300	°C
Θ_{JC}	Thermal resistance junction to case	20	°C/W
I_I	DC input current	±10	mA
P_D	Maximum power dissipation	1	W

Note:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD}	Supply voltage	4.5 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
T_C	Temperature range	-55 to + 125	°C

DC ELECTRICAL CHARACTERISTICS [7]

(V_{DD} = 5.0V ±10%; V_{SS} = 0V [6], -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{IL}	Low-level input voltage [1] ACTS ACS			0.8 $.3V_{DD}$	V
V_{IH}	High-level input voltage [1] ACTS ACS		$.5V_{DD}$ $.7V_{DD}$		V
I_{IN}	Input leakage current ACTS/ACS	V_{IN} = V_{DD} or V_{SS}	-1	1	µA
V_{OL}	Low-level output voltage [3] ACTS ACS	I_{OL} = 8.0mA I_{OL} = 100µA		0.40 0.25	V
V_{OH}	High-level output voltage [3] ACTS ACS	I_{OH} = -8.0mA I_{OH} = -100µA	$.7V_{DD}$ V_{DD} - 0.25		V
I_{OS}	Short-circuit output current [2,4] ACTS/ACS	V_O = V_{DD} and V_{SS}	-200	200	mA
I_{OL}	Output current[10] (Sink)	V_{IN} = V_{DD} or V_{SS} V_{OL} = 0.4V	8		mA
I_{OH}	Output current[10] (Source)	V_{IN} = V_{DD} or V_{SS} V_{OH} = V_{DD} - 0.4V	-8		mA
P_{total}	Power dissipation [2, 8, 9]	C_L = 50pF		2.9	mW/MHz
I_{DDQ}	Quiescent Supply Current	V_{DD} = 5.5V		10	µA
ΔI_{DDQ}	Quiescent Supply Current Delta ACTS	For input under test V_{IN} = V_{DD} - 2.1V For all other inputs V_{IN} = V_{DD} or V_{SS} V_{DD} = 5.5V		1.6	mA
C_{IN}	Input capacitance [5]	f = 1MHz @ 0V		15	pF
C_{OUT}	Output capacitance [5]	f = 1MHz @ 0V		15	pF

Notes:

1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(min) + 20\%, - 0\%$; $V_{IL} = V_{IL}(max) + 0\%, - 50\%$, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(min)$ and $V_{IL}(max)$.
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density $\leq 5.0E5$ amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF/MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
6. Maximum allowable relative shift equals 50mV.
7. All specifications valid for radiation dose $\leq$ 1E6 rads(Si).
8. Power does not include power contribution of any TTL output sink current.
9. Power dissipation specified per switching output.
10. This value is guaranteed based on characterization data, but not tested.

AC ELECTRICAL CHARACTERISTICS [2]

(V_{DD} = 5.0V ±10%; V_{SS} = 0V [1], -55°C < T_C < +125°C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{PHL}	CLK or CLK INH to Q_H or $\overline{Q}_H$	2	21	ns
t_{PLH}	CLK or CLK INH to Q_H or $\overline{Q}_H$	2	18	ns
t_{PHL}	SH/$\overline{LD}$ to Q_H or $\overline{Q}_H$	2	21	ns
t_{PLH}	SH/$\overline{LD}$ to Q_H or $\overline{Q}_H$	2	18	ns
t_{PHL}	H to Q_H	2	21	ns
t_{PLH}	H to Q_H	2	17	ns
t_{PHL}	H to $\overline{Q}_H$	2	20	ns
t_{PLH}	H to $\overline{Q}_H$	2	18	ns
f_{MAX}	Maximum clock frequency		71	MHz
t_{SU1}	SER, SH/$\overline{LD}$, CLKINH or CLK Setup time before CLK ↑or CLK INH ↑	7		ns
t_{SU2}	Data setup time before SH/$\overline{LD}$	7		ns
t_{H1}	SER hold time after CLK or CLK INH ↑	2		ns
t_{H2}	CLK INH hold time after CLK ↑	2		ns
t_{H3} [3]	Hold time for any input after SH/$\overline{LD}$	2		ns
t_W	Minimum pulse width CLK or CLK INH high CLK or CLK INH low SH/$\overline{LD}$	7		ns

Notes:
1. Maximum allowable relative shift equals 50mV.
2. All specifications valid for radiation dose ≤ 1E6 rads(Si).
3. Based on characterization, hold time (t_{H3}) of 0ns for data pins A-H, can be assumed if data setup time (t_{SU2}) is ≥10ns. This is guaranteed, but not tested.