UTI760A RTS Remote Terminal for Stores

FEATURES

- ❒ Complete MIL-STD-1760A Notice I through III remote terminal interface
- ❒ 1K x 16 of on-chip static RAM for message data, completely accessible to host
- ❒ Self-test capability, including continuous loop-back compare
- ❒ Programmable memory mapping via pointers for efficient use of internal memory, including buffering multiple messages per subaddress
- ❒ RT-RT Terminal Address Compare
- ❒ Command word stored with incoming data for enhanced data management
- ❒ User selectable RAM Busy (RBUSY) signal for slow or fast processor interfacing
- ❒ Full military operating temperature range, -55°C to +125°C, screened to the specific test methods listed in Table I of MIL-STD-883, Method 5004, Class B, also Standard Military Drawing available
- ❒ Available in 68-pin pingrid array package

INTRODUCTION

The UT1760A RTS is a monolithic CMOS VLSI solution to the requirements of the dual-redundant MIL-STD-1553B interface as specified by MIL-STD-1760A. Designed to reduce cost and space in the mission stores interface, the RTS integrates the remote terminal logic with a user-configured 1K x 16 static RAM. In addition, the RTS has a flexible subsystem interface to permit use with most processors or controllers.

The RTS provides all protocol, data handling, error checking, and memory control functions, as well as comprehensive self-test capabilities. The RTS's memory meets all of a mission store's message storage needs through user-defined memory mapping. This memory-mapped architecture allows multiple message buffering at

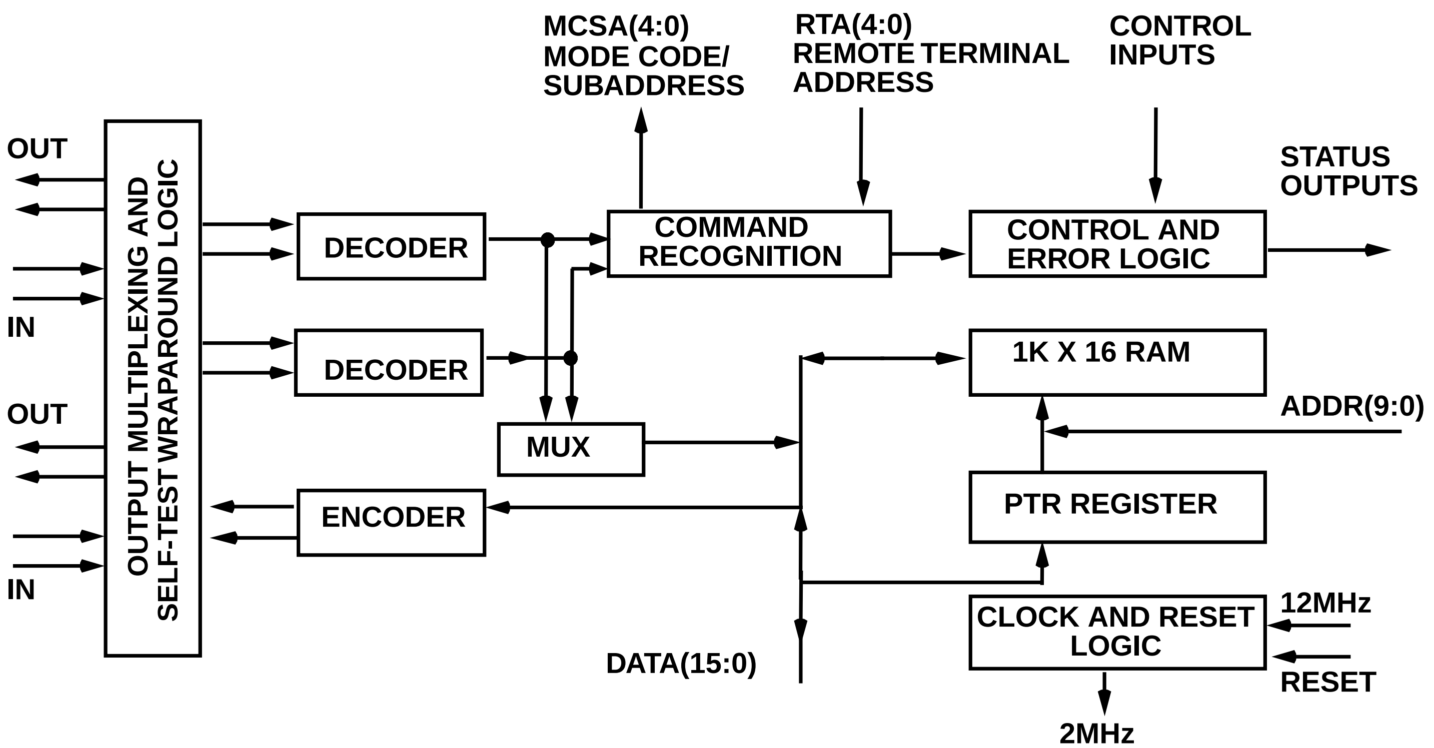

Figure 1. UT1760A RTS Functional Block Diagram

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1.0 ARCHITECTURE AND OPERATION

The UT1760A RTS is an interface device linking a MIL-STD-1553 serial data bus and a host microprocessor system. The RTS's MIL-STD-1553B interface includes encoding/decoding logic, error detection, command recognition, 1K x 16 of SRAM, pointer registers, clock, and reset circuits. Illegal subaddress circuitry makes the RTS MIL-STD-1760A-specific.

1.1 Memory Map and Host Memory Interface

The host can access the 1K x 16 RAM memory like a standard RAM device through the 10-bit address and 16-bit data buses. The host uses the Chip Select ($\overline{CS}$), Read/Write (RD/$\overline{WR}$), and Output Enable ($\overline{OE}$) signals to control data transfer to and from memory. When the RTS requires access to its own internal RAM, it asserts the RBUSY signal to alert the host. The RBUSY signal is programmable via the internal Control Register to be asserted either 5.7ms or 2.7ms prior to the RTS needing access to its internal RAM.

The RTS stores MIL-STD-1760A messages in 1K x 16 of on-chip RAM. For efficient use of the 1K x 16 memory on the RTS, the host programs a set of pointers to map where the 1760A message is stored. The RTS uses the upper 64 words (address 3C0 (hex) through 3FF (hex)) as pointers. The RTS provides pointers for all 30 receive subaddresses, all 30 transmit subaddresses, and four mode code commands with associated data words as defined in MIL-STD-1553B. The remaining 960 words of memory contain receive, transmit, and mode code data in a host-defined structure.

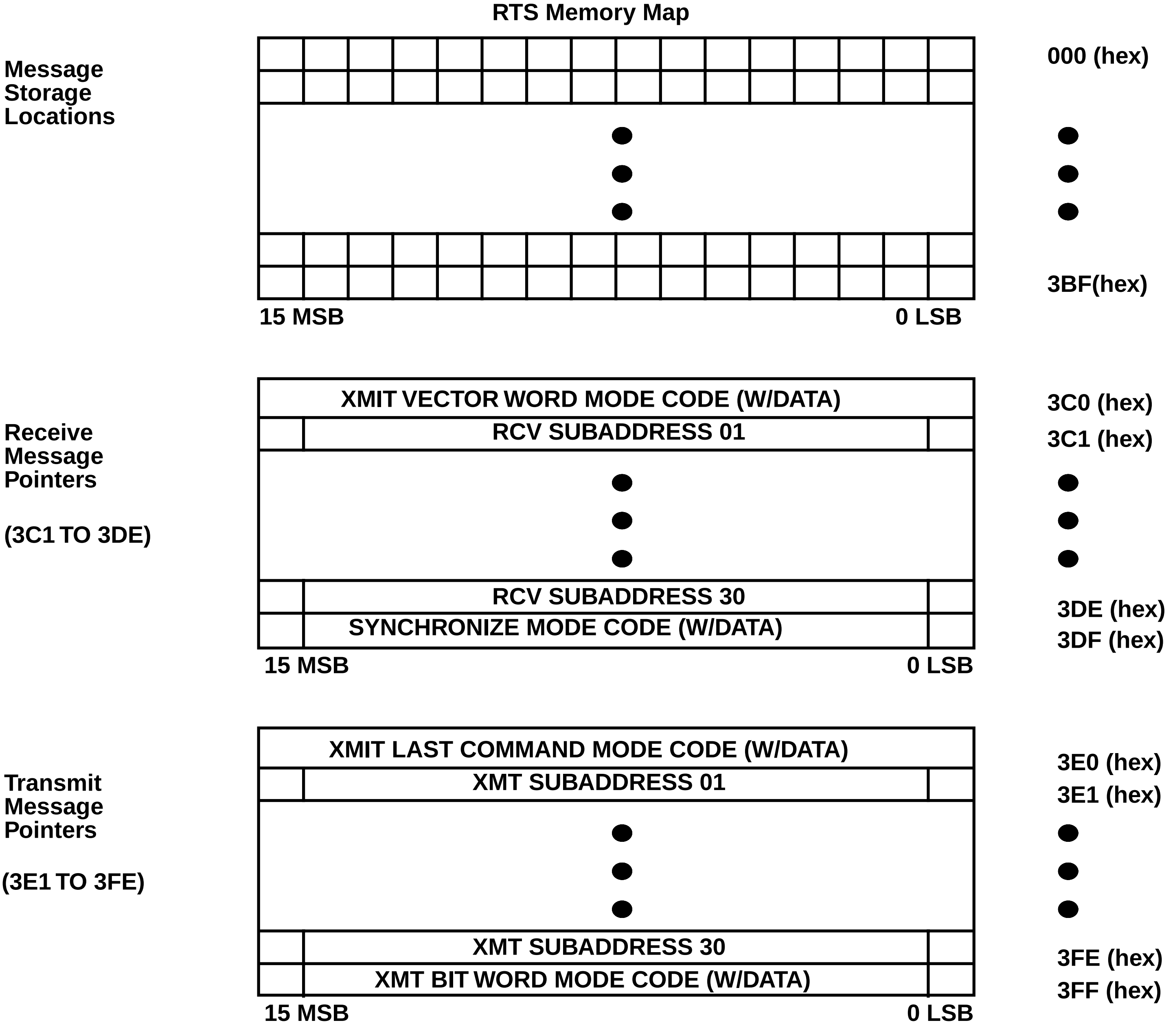


Figure 2. RTS Memory Map

MESSAGE INDEX	MESSAGE DATA ADDRESS
15 (MSB) 10	9 0 (LSB)

Message Index:
Defines the maximum messages buffered for the given subaddress.

Message Data Address:
Indicates the starting memory address for incoming message storage.

Figure 3. Message Pointer Structure

1.2 RTS RAM Pointer Structure

The RAM 16-bit pointers have a 6-bit index field and a 10-bit address field. The 6-bit index field allows for the storage of up to 64 messages per subaddress. A message consists of the 1553 command word and its associated data words.

The 16-bit pointer for Transmit Last Command Mode Code is located at memory location 3E0 (hex). The Transmit Last Command Mode Code pointer buffers up to 63 command words. An example of command word storage follows:

Example:

3E0 (hex) Contents = FC00 (hex)

11 1111 00 0000 0000

Address Field = 000 (hex)
Index Field = 3F (hex)

First command word storage location (3E0 = F801):

Address Field = 001 (hex)
Index Field = 3E (hex)

Sixty-third command word storage location (3E0 = 003F):

Address Field = 03F (hex)
Index Field = 00 (hex)

Sixty-fourth command word storage location (3E0 = 003F) (previous command word overwritten):

Address Field = 03F (hex)
Index Field = 00 (hex)

The Transmit Last Command Mode Code has Address Field boundary conditions for the location of command word buffers. The host can allocate a maximum 63 sequential locations following the Address Field starting address. For proper operation, the Address Field must start on an I x 40 (hex) address boundary, where I is greater than or equal to zero and less than or equal to 14. A list of valid Index and Address Fields follows:

I	Valid Index Fields	Valid Address Fields
0	3F (hex) to 00 (hex)	000 (hex) to 03F(hex)
1	3F (hex) to 00 (hex)	040 (hex) to 07F (hex)
2	3F (hex) to 00 (hex)	080 (hex) to 0BF(hex)
3	3F (hex) to 00 (hex)	0C0 (hex) to 0FF (hex)
4	3F (hex) to 00 (hex)	100 (hex) to 13F (hex)
5	3F (hex) to 00 (hex)	140 (hex) to 17F (hex)
6	3F (hex) to 00 (hex)	180 (hex) to 1BF (hex)
7	3F (hex) to 00 (hex)	1C0 (hex) to 1FF (hex)
8	3F (hex) to 00 (hex)	200 (hex) to 23F (hex)
9	3F (hex) to 00 (hex)	240 (hex) to 27F (hex)
10	3F (hex) to 00 (hex)	280 (hex) to 2BF (hex)
11	3F (hex) to 00 (hex)	2C0 (hex) to 2FF (hex)
12	3F (hex) to 00 (hex)	300 (hex) to 33F (hex)
13	3F (hex) to 00 (hex)	340 (hex) to 37F (hex)
14	3F (hex) to 00 (hex)	380 (hex) to 3BF (hex)

Subaddress/Mode Code		RAM Location	Subaddress/Mode Code		RAM Location
Transmit Vector Word Mode Code		3C0 (hex)	Transmit Last Command Mode Code		3E0 (hex)
Receive Subaddress	01	3C1 (hex)	Transmit Subaddress	01	3E1 (hex)
Receive Subaddress	02	3C2 (hex)	Transmit Subaddress	02	3E2 (hex)
Receive Subaddress	03	3C3 (hex)	Transmit Subaddress	03	3E3 (hex)
Receive Subaddress	04	3C4 (hex)	Transmit Subaddress	04	3E4 (hex)
Receive Subaddress	05	3C5 (hex)	Transmit Subaddress	05	3E5 (hex)
Receive Subaddress	06	3C6 (hex)	Transmit Subaddress	06	3E6 (hex)
Receive Subaddress	07	3C7 (hex)	Transmit Subaddress	07	3E7 (hex)
Receive Subaddress	08	3C8 (hex)	Transmit Subaddress	08	3E8 (hex)
Receive Subaddress	09	3C9 (hex)	Transmit Subaddress	09	3E9 (hex)
Receive Subaddress	10	3CA (hex)	Transmit Subaddress	10	3EA (hex)
Receive Subaddress	11	3CB (hex)	Transmit Subaddress	11	3EB (hex)
Receive Subaddress	12	3CC (hex)	Transmit Subaddress	12	3EC (hex)
Receive Subaddress	13	3CD (hex)	Transmit Subaddress	13	3ED (hex)
Receive Subaddress	14	3CE (hex)	Transmit Subaddress	14	3EE (hex)
Receive Subaddress	15	3CF (hex)	Transmit Subaddress	15	3EF (hex)
Receive Subaddress	16	3D0 (hex)	Transmit Subaddress	16	3F0 (hex)
Receive Subaddress	17	3D1 (hex)	Transmit Subaddress	17	3F1 (hex)
Receive Subaddress	18	3D2 (hex)	Transmit Subaddress	18	3F2 (hex)
Receive Subaddress	19	3D3 (hex)	Transmit Subaddress	19	3F3 (hex)
Receive Subaddress	20	3D4 (hex)	Transmit Subaddress	20	3F4 (hex)
Receive Subaddress	21	3D5 (hex)	Transmit Subaddress	21	3F5 (hex)
Receive Subaddress	22	3D6 (hex)	Transmit Subaddress	22	3F6 (hex)
Receive Subaddress	23	3D7 (hex)	Transmit Subaddress	23	3F7 (hex)
Receive Subaddress	24	3D8 (hex)	Transmit Subaddress	24	3F8 (hex)
Receive Subaddress	25	3D9 (hex)	Transmit Subaddress	25	3F9 (hex)
Receive Subaddress	26	3DA (hex)	Transmit Subaddress	26	3FA (hex)
Receive Subaddress	27	3DB (hex)	Transmit Subaddress	27	3FB (hex)
Receive Subaddress	28	3DC (hex)	Transmit Subaddress	28	3FC (hex)
Receive Subaddress	29	3DD (hex)	Transmit Subaddress	29	3FD (hex)
Receive Subaddress	30	3DE (hex)	Transmit Subaddress	30	3FE (hex)
Synchronize w/Data Word Mode Code		3DF (hex)	Transmit Bit Word Mode Code		3FF (hex)

1.3 Internal Registers

The RTS uses two internal registers to allow the host to control the RTS operation and monitor its status. The host uses the Control ($\overline{CTRL}$) signal along with Chip Select ($\overline{CS}$), Read/Write (RD/$\overline{WR}$), and Output Enable ($\overline{OE}$) to read the 16-bit Status Register or write to the 13-bit Control Register. No address data is needed to select a register. The Control Register toggles bits in the MIL-STD-1553B status word, enables the biphase inputs, recognizes broadcast commands, selects Notice I and II or III, determines RAM Busy (RBUSY) timing, selects disconnect or terminal active flag, and puts the part in self-test mode. The Status Register supplies operational status of the UT1760A RTS to the host. These registers must be initialized before attempting RTS operation. Internal registers can be accessed while RBUSY is active.

Control Register (Write Only)

The 13-bit write-only Control Register manages the operation of the RTS. Write to the Control Register by applying a logic one to $\overline{\text{OE}}$, and a logic zero to $\overline{\text{CTRL}}$, $\overline{\text{CS}}$, and RD/$\overline{\text{WR}}$. Data is loaded into the Control Register via I/O pins DATA(12:0). Control register write must occur 50ns before the rising edge of $\overline{\text{COMSTR}}$ to latch data into the outgoing status word.

Bit Number	Initial Condition	Description
Bit 0	[1]	Channel A Enable. A logic 1 enables Channel A biphase inputs.
Bit 1	[1]	Channel B Enable. A logic 1 enables Channel B biphase inputs.
Bit 2	[0]	Terminal Flag. A logic 1 sets the Terminal Flag bit of the Status Word.
Bit 3	[1]	System Busy. A logic 1 sets the Busy bit of the Status Word and limits RTS access to the memory. No data word can be retrieved or stored; command words will be stored.
Bit 4	[0]	Subsystem Busy. A logic 1 sets the Subsystem Flag bit of the Status Word.
Bit 5	[0]	Self-Test Channel Select. This bit selects which channel the self-test checks; a logic 1 selects Channel A and a logic 0 selects Channel B.
Bit 6	[0]	Self-Test Enable. A logic 1 places the RTS in the internal self-test mode and inhibits normal operation. Channels A and B should be disabled if self-test is chosen.
Bit 7	[0]	Service Request. A logic 1 sets the Service Request bit of the Status Word.
Bit 8	[0]	Instrumentation. A logic 1 sets the Instrumentation bit of the Status Word.
Bit 9	[1]	Broadcast Enable. A logic 1 enables the RTS to recognize broadcast commands.
Bit 10	[1]	Notice Select. A logic 1 enables Notice III operation; logic 0 enables Notice I or II operation.
Bit 11	[1]	DSCNCT/$\overline{\text{TERACT}}$ Pin Select. A logic 1 selects the “Disconnect” function; a logic 0 selects the “Terminal Active” function.
Bit 12	[1]	RBUSY Time Select. A logic 1 selects a 5.7µs RBUSY alert; a logic 0 selects a 2.7µs RBUSY alert.

[] - Values in parentheses indicate the initialized values of these bits.

CONTROL REGISTER (WRITE ONLY):

X	X	X	RBUSY TS	PS	NO TICE	BCEN	INS	SRQ	ITST	ITCS	SUBS	BUSY	TF	CH B EN	CH A EN
			[1]	[1]	[1]	[1]	[0]	[0]	[0]	[0]	[0]	[1]	[0]	[1]	[1]

MSB **LSB**

[ ] defines reset state

Figure 4a. Control Register

Status Register (Read Only):
The 16-bit read-only Status Register provides the RTS system status. Read the Status Register by applying a logic 0 to $\overline{\text{CTRL}}$, $\overline{\text{CS}}$, and $\overline{\text{OE}}$, and a logic 1 to RD/$\overline{\text{WR}}$. The 16-bit contents of the Status Register are read from data I/O pins DATA(15:0).

Bit Number	**Initial Condition**	**Description**
Bit 0	[0]	MCSA0. The LSB of the mode code or subaddress as indicated by the logic state of bit 5.
Bit 1	[0]	MCSA1. Mode code or subaddress as indicated by the logic state of bit 5.
Bit 2	[0]	MCSA2. Mode code or subaddress as indicated by the logic state of bit 5.
Bit 3	[0]	MCSA3. Mode code or subaddress as indicated by the logic state of bit 5.
Bit 4	[0]	MCSA4. Mode code or subaddress as indicated by the logic state of bit 5.
Bit 5	[0]	$\overline{\text{MC}}$/SA. A logic 1 indicates that bits 4 through 0 are the subaddress of the last command word, and that the last command word was a normal transmit or receive command. A logic 0 indicates that bits 4 through 0 are a mode code, and that the last command was a mode command.
Bit 6	[1]	Channel A/$\overline{\text{B}}$. A logic 1 indicates that the most recent command arrived on Channel A; a logic 0 indicates that it arrived on Channel B.
Bit 7	[1]	Channel B Enabled. A logic 1 indicates that Channel B is available for both reception and transmission.
Bit 8	[1]	Channel A Enabled. A logic 1 indicates that Channel A is available for both reception and transmission.
Bit 9	[1]	Terminal Flag Enabled. A logic 1 indicates that the Bus Controller has not issued an Inhibit Terminal Flag Mode Code. A logic 0 indicates that the Bus Controller, via the above mode code, is overriding the host system's ability to set the Terminal Flag bit of the status word.
Bit 10	[1]	Busy. A logic 1 indicates the Busy bit is set. This bit is reset when the System Busy bit in the Control Register is reset.
Bit 11	[0]	Self-Test. A logic 1 indicates that the chip is in the internal self-test mode. This bit is reset when the self-test is terminated.
Bit 12	[0]	TA Parity Error. A logic 1 indicates the wrong Terminal Address parity; it causes the biphase inputs to be disabled. TA Parity Error results in the Message Error bit being set to a logic one, and Channels A and B become disabled.
Bit 13	[0]	Message Error. A logic 1 indicates that a message error has occurred since the last Status Register read. This bit is not reset until the Status Register has been examined. Message error condition must be removed before reading the Status Register to reset the Message Error bit.
Bit 14	[0]	Valid Message. A logic 1 indicates that a valid message has been received since the last Status Register read. This bit is not reset until the Status Register has been examined.
Bit 15	[0]	Terminal Active. A logic 1 indicates the device is executing a transmit or receive operation. Same as $\overline{\text{TERACT}}$ output except active high. (Always $\overline{\text{TERACT}}$; never DSCNCT.)

[] - Values in parentheses indicate the initialized values of these bits.

STATUS REGISTER (READ ONLY):

TERM ACTV	VAL MESS	MESS ERR	TAPA ERR	SELF-TEST	BUSY	TFEN	CH A EN	CH B EN	CHNL A/B	$\overline{\text{MC}}$/ SA	MCSA 4	MCSA 3	MCSA 2	MCSA 1	MCSA 0
[0] MSB	[0]	[0]	[0]	[0]	[1]	[1]	[1]	[1]	[1]	[0]	[0]	[0]	[0]	[0]	[0] LSB

[ ] defines reset state

Figure 4b. Status Register

1.4 Mode Code and Subaddress

The UT1760A RTS provides two modes of illegal subaddress decoding, one meeting MIL-STD-1760A Notices I and II, and the other meeting MIL-STD-1760A Notice III. In addition, the device has automatic internal illegal command decoding for reserved MIL-STD-1553B mode codes. These definitions are extracted from MIL-STD-1760A and reviewed in section 1.5 of this document. Upon command word validation and decode, status pins MCSA(4:0) and $\overline{MC}$/SA become valid. Status pin $\overline{MC}$/SA will indicate whether the data on pins MCSA(4:0) is mode code or subaddress information. Status Register bits 0 through 5 contain the same information as pins MCSA(4:0) and $\overline{MC}$/SA. The system designer can use signals MCSA(4:0), $\overline{MC}$/SA, $\overline{BRDCST}$, RTRT, etc. to illegalize mode codes, subaddresses, and other message formats (broadcast and RT-to-RT) via the Illegal Command (ILLCOM) input to the part.

RTS MODE CODE HANDLING PROCEDURE

T/R	Mode Code	Function	Operation
0	10100	Selected Transmitter Shutdown [2]	1. Command word stored 2. MERR pin asserted 3. MERR bit set in Status Register 4. Status word transmitted
0	10101	Override Selected Transmitter Shutdown [2]	1. Command word stored 2. MERR pin asserted 3. MERR bit set in Status Register 4. Status word transmitted
0	10001	Synchronize (w/Data)	1. Command word stored 2. Data word stored 3. Status word transmitted
1	00000	Dynamic Bus Control [2]	1. Command word stored 2. MERR pin asserted 3. MERR bit set in Status Register 4. Status word transmitted
1	00001	Synchronize [1]	1. Command word stored 2. Status word transmitted
1	00010	Transmit Status Word [3]	1. Command word stored 2. Status word transmitted
1	00011	Initiate Self-Test [1]	1. Command word stored 2. Status word transmitted
1	00100	Transmitter Shutdown	1. Command word stored 2. Alternate bus shutdown 3. Status word transmitted
1	00101	Override Transmitter Shutdown	1. Command word stored 2. Alternate bus enabled 3. Status word transmitted
1	00110	Inhibit Terminal Flag Bit	1. Command word stored 2. Terminal Flag bit set to zero and disabled 3. Status word transmitted
1	00111	Override Inhibit Terminal Flag	1. Command word stored 2. Terminal Flag bit enabled, but not set to logic one 3. Status word transmitted
1	01000	Reset Remote Terminal [1]	1. Command word stored 2. Status word transmitted
1	10010	Transmit Last Command Word [3]	1. Status word transmitted 2. Last command word transmitted
1	10000	Transmit Vector Word	1. Command word stored 2. Status word transmitted 3. Data word transmitted
1	10011	Transmit BIT Word	1. Command word stored 2. Status word transmitted 3. Data word transmitted

Notes:
1. Further host interaction required for mode code operation.
2. Reserved mode code; A) MERR pin asserted, B) MESS ERR bit set, C) status word transmitted (ME bit set to logic one).
3. Status word not affected.
4. Undefined mode codes are treated as reserved mode codes.

1.5 MIL-STD-1760A Subaddress and Mode Code Definitions

Table 1. Subaddress and Mode Code Definitions Per MIL-STD-1760A Notice I

Subaddress Field Binary (Decimal)	Message Format		Description
	Receive	Transmit	
00000 (00)	B.40.1.1.3 [1]	B.40.1.1.3	Mode Code Indicator
00001 (01)	Reserved B.40.2.1 [2]	Store Description	
00010 (02)	User Defined	User Defined	
00011 (03)	Reserved	Reserved	
00100 (04)	User Defined	User Defined	
00101 (05)	Reserved	Reserved	
00110 (06)	User Defined	User Defined	
00111 (07)	User Defined	User Defined	
01000 (08)	Reserved	Reserved	
01001 (09)	User Defined	User Defined	
01010 (10)	User Defined	User Defined	
01011 (11)	Reserved	Reserved	
01100 (12)	User Defined	User Defined	
01101 (13)	User Defined	User Defined	
01110 (14)	Reserved	Reserved	
01111 (15)	Reserved	User Defined	
10000 (16)	User Defined	User Defined	
10001 (17)	User Defined	User Defined	
10010 (18)	User Defined	User Defined	
10011 (19)	Reserved	Reserved	Nuclear Weapon
10100 (20)	User Defined	User Defined	
10101 (21)	Reserved	User Defined	
10110 (22)	User Defined	User Defined	
10111 (23)	User Defined	User Defined	
11000 (24)	User Defined	User Defined	
11001 (25)	User Defined	User Defined	
11010 (26)	User Defined	User Defined	
11011 (27)	Reserved	Reserved	Nuclear Weapon
11100 (28)	User Defined	User Defined	
11101 (29)	User Defined	User Defined	
11110 (30)	User Defined	User Defined	
11111 (31)	B.40.1.1.3	B.40.1.1.3	Mode Code Indicator

Notes:
1. Refer to section B.40.1.1.3 of the MIL-STD-1760A specification for definition.
2. Refer to section B.40.2.1 of the MIL-STD-1760A specification for definition.
3. Reserved subaddresses illegalized; Message Error bit and pin set; SW transmitted.

Table 2. Subaddress and Mode Code Definitions Per MIL-STD-1760A Notice II

Subaddress Field Binary (Decimal)	Message Format		Description
	Receive	Transmit	
00000 (00)	B.40.1.1.3 [1]	B.40.1.1.3	Mode Code Indicator
00001 (01)	Reserved B.40.2.1 [2]	Store Description	
00010 (02)	User Defined	User Defined	
00011 (03)	Reserved	Reserved	
00100 (04)	User Defined	User Defined	
00101 (05)	Reserved	Reserved	
00110 (06)	User Defined	User Defined	
00111 (07)	User Defined	User Defined	
01000 (08)	Reserved	Reserved	
01001 (09)	User Defined	User Defined	
01010 (10)	User Defined	User Defined	
01011 (11)	Reserved	Reserved	
01100 (12)	User Defined	User Defined	
01101 (13)	User Defined	User Defined	
01110 (14)	Reserved	Reserved	
01111 (15)	Reserved	User Defined	
10000 (16)	User Defined	User Defined	
10001 (17)	User Defined	User Defined	
10010 (18)	User Defined	User Defined	
10011 (19)	Reserved	Reserved	Nuclear Weapon
10100 (20)	User Defined	User Defined	
10101 (21)	Reserved	User Defined	
10110 (22)	User Defined	User Defined	
10111 (23)	User Defined	User Defined	
11000 (24)	User Defined	User Defined	
11001 (25)	User Defined	User Defined	
11010 (26)	User Defined	User Defined	
11011 (27)	Reserved	Reserved	Nuclear Weapon
11100 (28)	User Defined	User Defined	
11101 (29)	User Defined	User Defined	
11110 (30)	User Defined	User Defined	
11111 (31)	B.40.1.1.3	B.40.1.1.3	Mode Code Indicator

Notes:
1. Refer to section B.40.1.1.3 of the MIL-STD-1760A specification for definition.
2. Refer to section B.40.2.1 of the MIL-STD-1760A specification for definition.
3. Reserved subaddresses illegalized; Message Error bit and pin set; SW transmitted.

Table 3. Subaddress and Mode Code Definitions Per MIL-STD-1760A Notice III

Subaddress Field Binary (Decimal)	Message Format		Description
	Receive	Transmit	
00000 (00)	B.40.1.1.3 [1]	B.40.1.1.3	Mode Code Indicator
00001 (01)	Reserved B.40.2.1 [2]	Store Description	
00010 (02)	User Defined	User Defined	
00011 (03)	User Defined	User Defined	
00100 (04)	User Defined	User Defined	
00101 (05)	User Defined	User Defined	
00110 (06)	User Defined	User Defined	
00111 (07)	User Defined	User Defined	
01000 (08)	Reserved	Reserved	Test Only
01001 (09)	User Defined	User Defined	
01010 (10)	User Defined	User Defined	
01011 (11)	B.40.2.2.1 [3]	B.40.2.2.1	Mission Store Control/Monitor
01100 (12)	User Defined	User Defined	
01101 (13)	User Defined	User Defined	
01110 (14)	B.40.1.1.5.8 [4]	B.40.1.5.8	Mass Data Transfer
01111 (15)	User Defined	User Defined	
10000 (16)	User Defined	User Defined	
10001 (17)	User Defined	User Defined	
10010 (18)	User Defined	User Defined	
10011 (19)	B.40.2.2.4 [5]	B.40.2.2.5 [6]	Nuclear Weapon
10100 (20)	User Defined	User Defined	
10101 (21)	User Defined	User Defined	
10110 (22)	User Defined	User Defined	
10111 (23)	User Defined	User Defined	
11000 (24)	User Defined	User Defined	
11001 (25)	User Defined	User Defined	
11010 (26)	User Defined	User Defined	
11011 (27)	B.40.2.2.4	B.40.2.2.5	Nuclear Weapon
11100 (28)	User Defined	User Defined	
11101 (29)	User Defined	User Defined	
11110 (30)	User Defined	User Defined	
11111 (31)	B.40.1.1.3	B.40.1.1.3	Mode Code Indicator

Notes:

1. Refer to section B.40.1.1.3 of the MIL-STD-1760A specification for definition.
2. Refer to section B.40.2.1 of the MIL-STD-1760A specification for definition.
3. Refer to section B.40.2.2.1 of the MIL-STD-1760A specification for definition.
4. Refer to section B.40.1.1.5.8 of the MIL-STD-1760A specification for definition.
5. Refer to section B.40.2.2.4 of the MIL-STD-1760A specification for definition.
6. Refer to section B.40.2.2.5 of the MIL-STD-1760A specification for definition.
7. Reserved subaddresses illegalized; Message Error bit and pin set; SW transmitted.

1.6 Terminal Address

The Terminal Address of the RTS is programmed via five input pins: RTA(4:0) and RTPTY. Asserting $\overline{\text{MRST}}$ latches the RTS's Terminal Address from pins RTA(4:0) and parity bit RTPTY. The address and parity cannot change until the next assertion of the $\overline{\text{MRST}}$. The parity of the Terminal Address is odd; input pin RTPTY is set to a logic state to satisfy this requirement. A logic 1 on Status Register bit 12 indicates incorrect Terminal Address parity. An example follows:

RTA(4:0) = 05 (hex) = 00101
RTPTY = 1 (hex) = 1
Sum of 1's = 3 (odd), Status Register bit 12 = 0

RTA(4:0) = 04 (hex) = 00100
RTPTY = 0 (hex) = 0
Sum of 1's = 1 (odd), Status Register bit 12 = 0

RTA(4:0) = 04 (hex) = 00100
RTPTY = 1 (hex) = 1
Sum of 1's = 2 (even), Status Register bit 12 = 1

The RTS checks the Terminal Address and parity on Master Reset. The state of the DSCNCT signal indicates the mated status of the store. When all six Terminal Address pins (RTA(4:0), RTPTY) go to a logic one, the DSCNCT pin is asserted. To enable the disconnect function (DSCNCT pin) bit 11 of the Control Register is set to a logic one. With broadcast disabled, RTA (4:0) = 11111 operates as a normal RT address.

1.7 Internal Self-Test

Setting bit 6 of the Control Register to a logic one enables the internal self-test. Disable Channels A and B at this time to prevent bus activity during self-test by setting bits 0 and 1 of the Control Register to a logic zero. Normal operation is inhibited when internal self-test is enabled. The self-test capability of the RTS is based on the fact that the MIL-STD-1553B status word sync pulse is identical to the command word sync pulse. Thus, if the status word from the encoder is fed back to the decoder, the RTS will recognize the incoming status word as a command word and thus cause the RTS to transmit another status word. After the host invokes self-test, the RTS self-test logic forces a status word transmission even though the RTS has not received a valid command. The status word is sent to decoder A or B depending on the channel the host selected for self-test. The self-test is controlled by the host periodically changing the bit patterns in the status word being transmitted. Writing to the Control Register bits 2, 3, 4, 7, 8, and 10 changes the status word. Monitor the self-test by sampling either the Status Register or the external status pins (i.e., Command Strobe ($\overline{\text{COMSTR}}$), Transmit/Receive (T/$\overline{\text{R}}$)). For more detailed explanation of internal self-test, consult UTMC publication *RTR/RTS Internal Self-Test Routine.*

1.8 Power-up and Master Reset

After power-up, reset initializes the part with its biphase ports enabled, latches the Terminal Address, selects Notice III subaddress decoding, and turns on the busy option. The device is ready to accept commands from the MIL-STD-1553B bus. The busy flag is asserted while the host is loading the message pointers and messages. After this task is completed, the host removes the busy condition via a Control Register write to the RTS. On power-up if the terminal address parity (odd) is incorrect, the biphase inputs are disabled and the message error pin (MERR) is asserted. This condition can also be monitored via bit 12 of the Status Register. The MERR pin is negated on reception of first valid command.

1.9 Encoder and Decoder

The RTS interfaces directly to a bus transmitter/ receiver via the RTS Manchester II encoder/decoder. The UT1760A RTS receives the command word from the MIL-STD-1553B bus and processes it either by the primary or secondary decoder. Each decoder checks for the proper sync pulse and Manchester waveform, edge skew, correct number of bits, and parity. If the command is a receive command, the RTS processes each incoming data word for correct format and checks the control logic for correct word count and contiguous data. If an invalid message error is detected, the message error pin is asserted, the RTS ceases processing the remainder (if any) of the message, and it then suppresses status word transmission. Upon command validation recognition, the external status outputs are enabled. Reception of illegal commands does not suppress status word transmission.

The RTS automatically compares the transmitted word (encoder word) to the reflected decoder word by way of the continuous loop-back feature. If the encoder word and reflected word do not match, the transmitter error pin (TXERR) is asserted. In addition to the loop-back compare test, a timer precludes a transmission greater than 760μs by the assertion of Fail-safe Timer ($\overline{\text{TIMERON}}$). This timer is reset upon receipt of another command. (RT-to-RT transfer time-out = 57μs).

1.10 RT-RT Transfer Compare

The RT-to-RT Terminal Address compare logic makes sure that the incoming status word's Terminal Address matches the Terminal Address of the transmitting RT specified in the command word. An incorrect match results in setting the message error bit and suppressing transmission of the status word.

1.11 Illegal Command Decoding

The host has the option of asserting the ILLCOM pin to illegalize a received command word. On receipt of an illegal command, the RTS sets the Message Error bit in the status word, sets the message error output, and sets the message error latch in the Status Register.

The following RTS outputs may be used to externally decode an illegal command, Mode Code or Subaddress indicator ($\overline{MC}$/SA), Mode Code or Subaddress bus MCSA(4:0), Command Strobe ($\overline{COMSTR}$), Broadcast ($\overline{BRDCST}$), and Remote Terminal to Remote Terminal transfer (RTRT) (see figure 21 on page 34.)

To illegalize a transmit command, the ILLCOM pin must be asserted within 3.3μs after VALMSG goes to a logic 1 if the RTS is to respond with the Message Error bit of the status word at a logic 1. If the illegal command is mode code 2, 4, 5, 6, 7, or 18, the ILLCOM pin must be asserted within 664ns after Command Strobe ($\overline{COMSTR}$) transitions to logic 0. Asserting the ILLCOM pin within the 664ns inhibits the mode code function. For mode code illegalization, assert the ILLCOM pin until the VALMSG signal is asserted.

For an illegal receive command, the ILLCOM pin must be asserted within 18.2μs after the $\overline{COMSTR}$ transitions to a logic 0 in order to suppress data words from being stored. In addition, the ILLCOM pin must be at a logic 1 throughout the reception of the message until VALMSG is asserted. This does not apply to illegal transmit commands since the status word is transmitted first.

The above timing conditions also apply when the host externally decodes an illegal broadcast command. The host must remove the illegal command condition so that the next command is not falsely decoded as illegal.

2.0 Memory Map Example

Figures 5 and 6 illustrate the UT1760A RTS buffering three receive command messages to Subaddress 4. The receive message pointer for Subaddress 4 is located at 03C4 (hex) in the 1K x 16 RAM. The 16-bit contents of location 03C4 (hex) point to the memory location where the first receive message is stored. The Address Field defined as bits 0 through 9 of address 03C4 (hex) contain address information. The Index Field defined as bits 10 through 15 of address 03C4 (hex) contain the message buffer index (i.e., number of messages buffered).

Figure 5 demonstrates the updating of the message pointer as each message is received and stored. The memory storage of these three messages is shown in figure 6. After receiving the third message for Subaddress 4 (i.e., Index Field equals zero) the Address Field of the message pointer is not incremented. If the host does not update the receive message pointer for Subaddress 4 before the next receive command for Subaddress 4 is accepted, the third message will be overwritten.

Figures 7 and 8 show an example of multiple message retrieval from Subaddress 16 upon reception of a MIL-STD-1553B transmit command. The message pointer for transmit Subaddress 16 is located at 03F0 (hex) in the 1K x 16 RAM. The 16-bit contents of location 03F0 (hex) point to the memory location where the first message data words are stored.

Figure 7 demonstrates the updating of the message pointer as each message is received and stored. The data memory for these three messages is shown in figure 8.

Example:
Remote terminal will receive and buffer three MIL-STD-1553 receive commands of various word lengths to Subaddress 4.

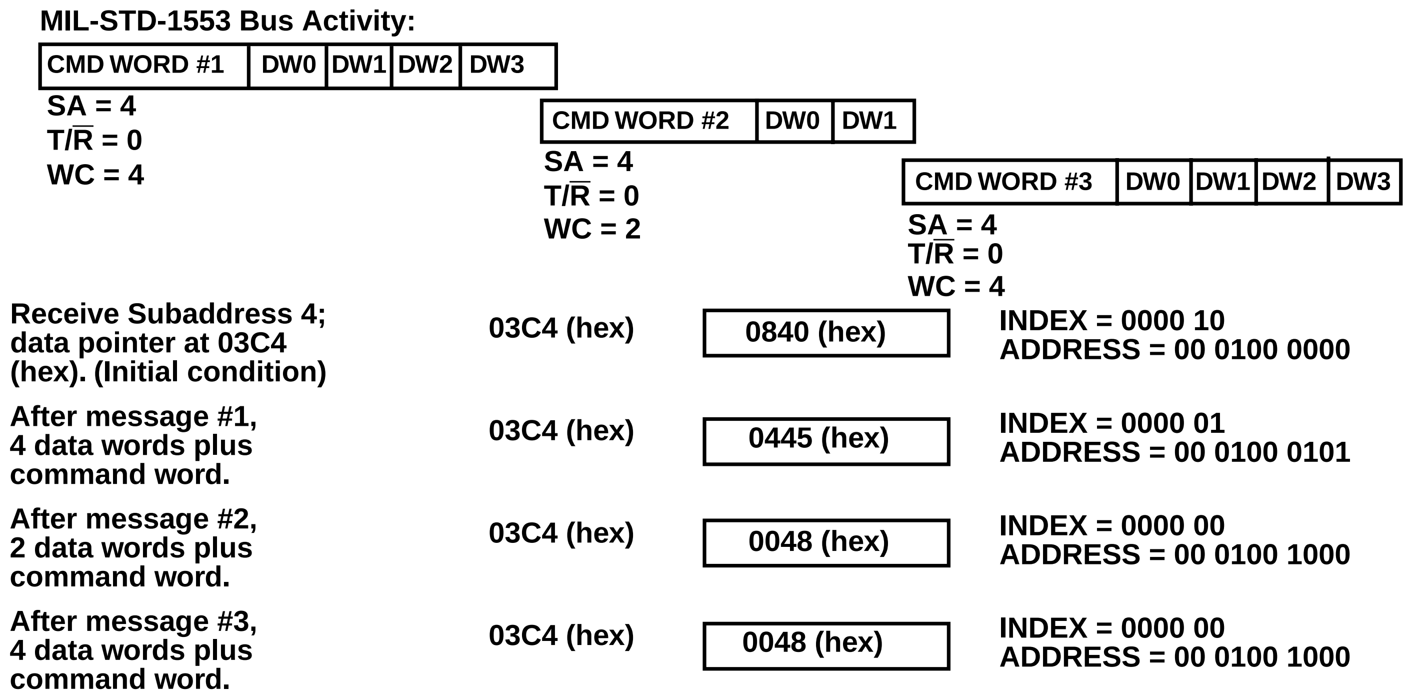


Figure 5. RTS Message Handling

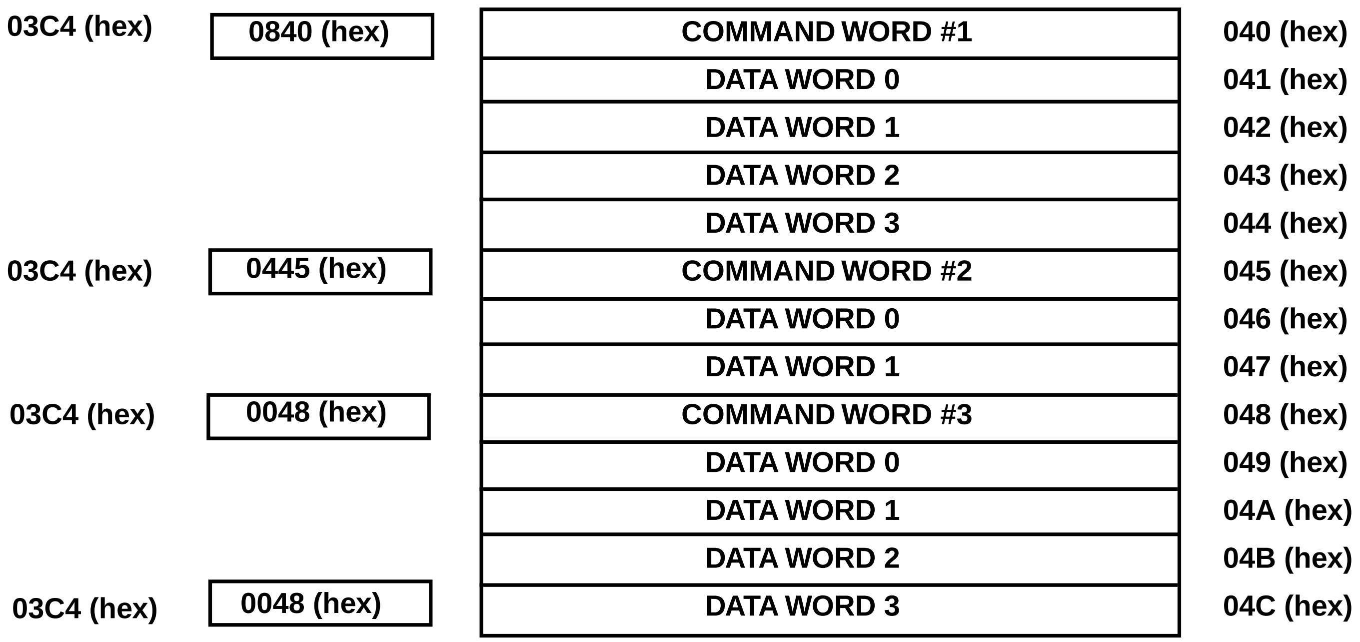


Figure 6. Memory Storage Subaddress 4

Example:
Remote terminal will transmit and buffer three MIL-STD-1553 transmit commands of various word lengths to Subaddress 16.

MIL-STD-1553 Bus Activity:

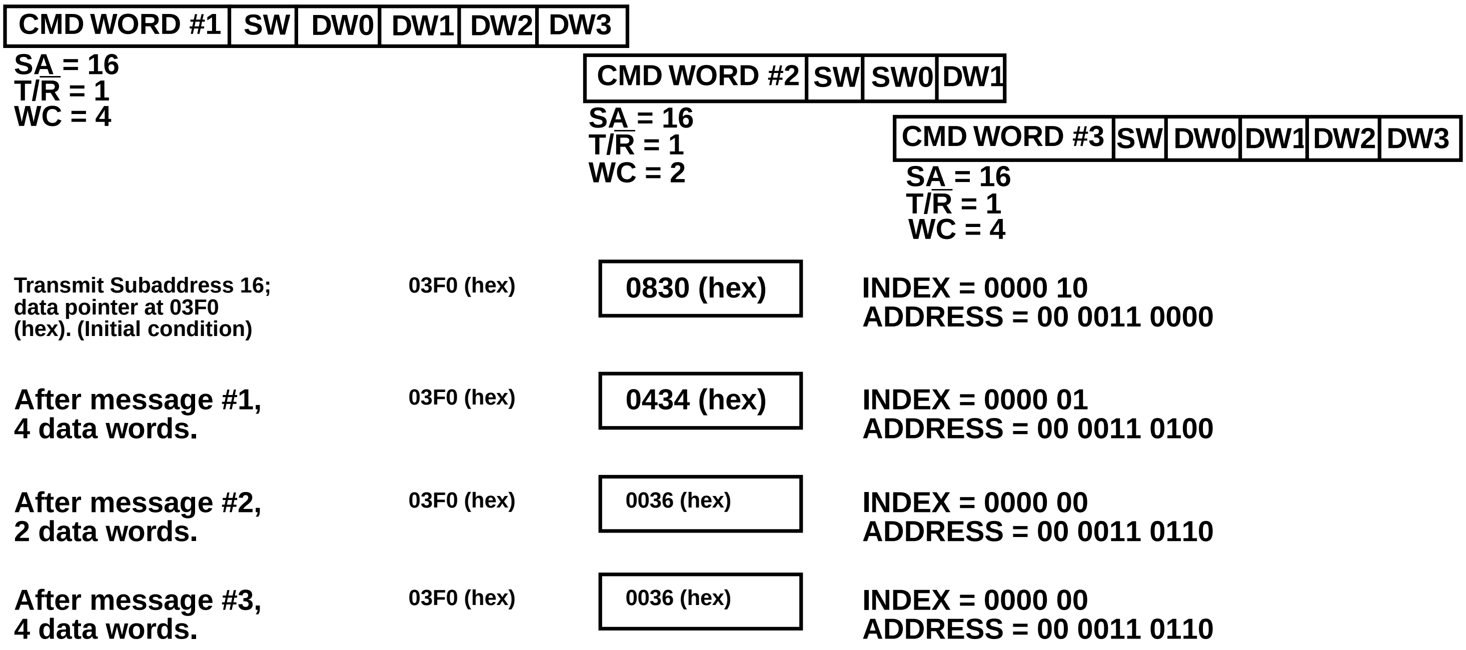
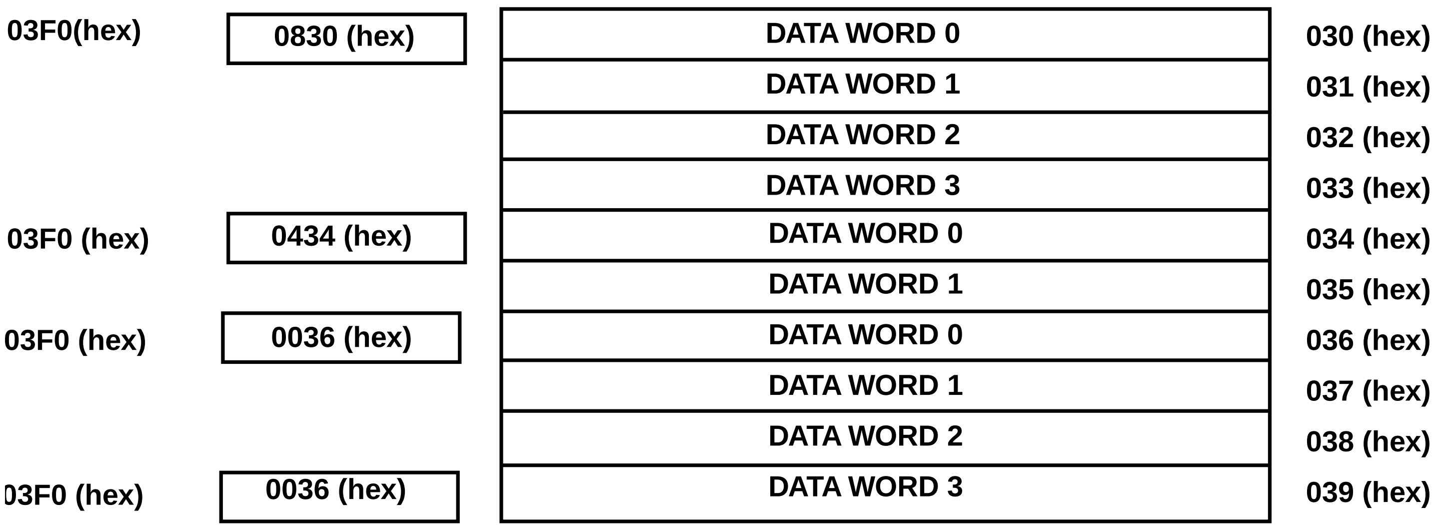


Figure 7. RTS Message Handling



Note:
Example is valid only if message structure is known in advance.

Figure 8. Memory Storage Subaddress 16

3.0 Pin Identification and Description

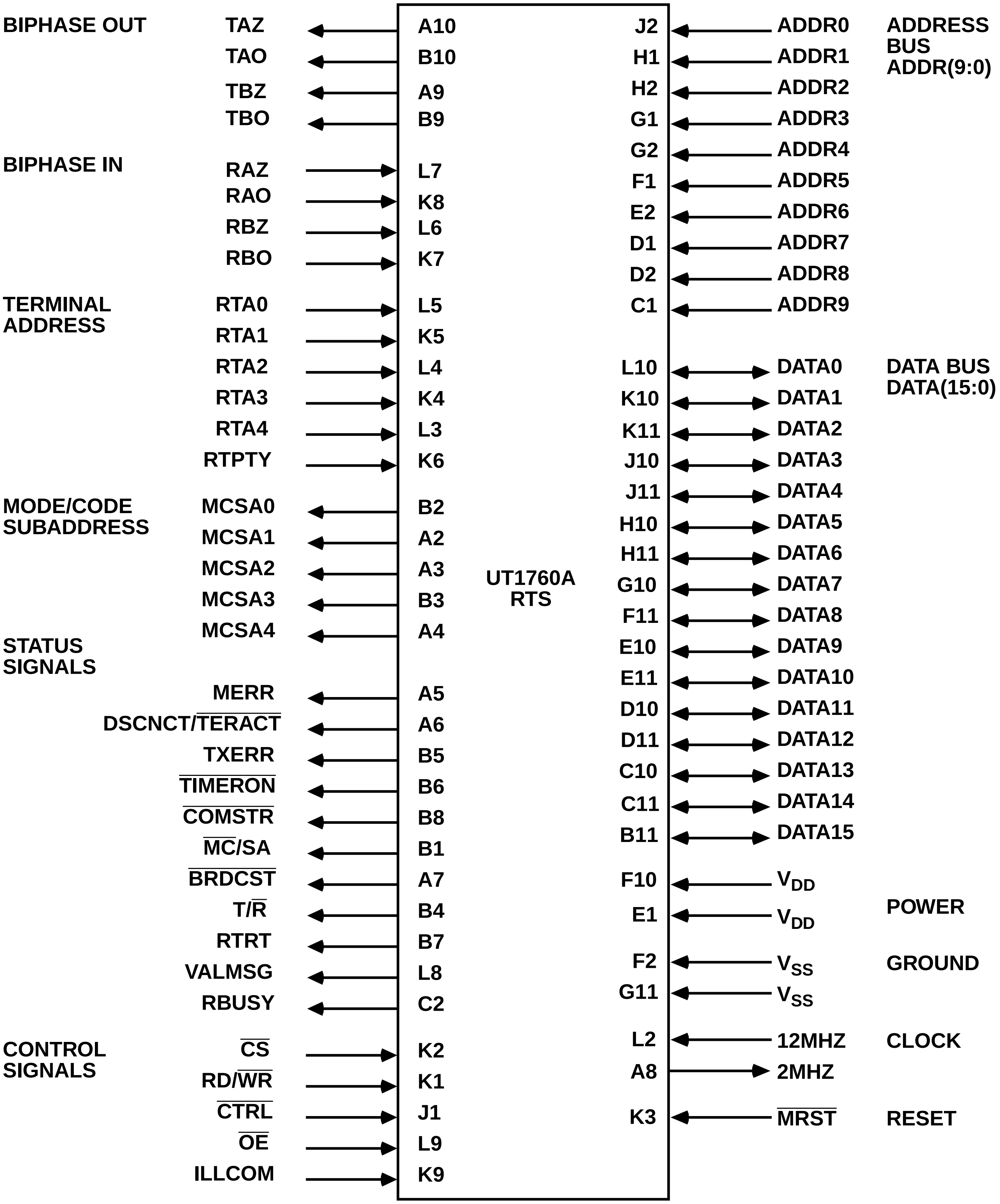


Figure 9. UT1760A RTS Pin Description

Legend for TYPE and ACTIVE Fields:

TI = TTL input
TUI = TTL input (pull-up)
TDI = TTL input (pull-down)
TO = TTL output
TTO = Three-state TTL output
TTB = Three-state TTL bidirectional
AL = Active low
AH = Active high
[] - Value in parentheses indicates initial state of these pins.

DATA BUS

NAME	PIN NUMBER (PGA)	TYPE	ACTIVE	DESCRIPTION
DATA15	B11	TTB	--	Bit 15 (MSB) of the bidirectional Data bus.
DATA14	C11	TTB	--	Bit 14 of the bidirectional Data bus.
DATA13	C10	TTB	--	Bit 13 of the bidirectional Data bus.
DATA12	D11	TTB	--	Bit 12 of the bidirectional Data bus.
DATA11	D10	TTB	--	Bit 11 of the bidirectional Data bus.
DATA10	E11	TTB	--	Bit 10 of the bidirectional Data bus.
DATA9	E10	TTB	--	Bit 9 of the bidirectional Data bus.
DATA8	F11	TTB	--	Bit 8 of the bidirectional Data bus.
DATA7	G10	TTB	--	Bit 7 of the bidirectional Data bus.
DATA6	H11	TTB	--	Bit 6 of the bidirectional Data bus.
DATA5	H10	TTB	--	Bit 5 of the bidirectional Data bus.
DATA4	J11	TTB	--	Bit 4 of the bidirectional Data bus.
DATA3	J10	TTB	--	Bit 3 of the bidirectional Data bus.
DATA2	K11	TTB	--	Bit 2 of the bidirectional Data bus.
DATA1	K10	TTB	--	Bit 1 of the bidirectional Data bus.
DATA0	L10	TTB	--	Bit 0 (LSB) of the bidirectional Data bus.

ADDRESS BUS

NAME	PIN NUMBER (PGA)	TYPE	ACTIVE	DESCRIPTION
ADDR9	C1	TI	--	Bit 9 (MSB) of the Address bus.
ADDR8	D2	TI	--	Bit 8 of the Address bus.
ADDR7	D1	TI	--	Bit 7 of the Address bus.
ADDR6	E2	TI	--	Bit 6 of the Address bus.
ADDR5	F1	TI	--	Bit 5 of the Address bus.
ADDR4	G2	TI	--	Bit 4 of the Address bus.
ADDR3	G1	TI	--	Bit 3 of the Address bus.
ADDR2	H2	TI	--	Bit 2 of the Address bus.
ADDR1	H1	TI	--	Bit 1 of the Address bus.
ADDR0	J2	TI	--	Bit 0 (LSB) of the Address bus.

CONTROL INPUTS

NAME	PIN NUMBER (PGA)	TYPE	ACTIVE	DESCRIPTION
$\overline{CS}$	K2	TI	AL	Chip Select. The host processor uses the $\overline{CS}$ signal for RTS Status Register reads, Control Register writes, or host access to the RTS internal RAM.
RD/$\overline{WR}$	K1	TI	--	Read/Write. The host processor uses a high level on this input in conjunction with $\overline{CS}$ to read the RTS Status Register or the RTS internal RAM. A low level on this input is used in conjunction with $\overline{CS}$ to write to the RTS Control Register or the RTS internal RAM.
$\overline{CTRL}$	J1	TI	AL	Control. The host processor uses the active low $\overline{CTRL}$ input signal in conjunction with $\overline{CS}$ and RD/$\overline{WR}$ to access the RTS registers. A high level on this input means access is to RTS internal RAM only.
$\overline{OE}$	L9	TI	AL	Output Enable. The active low $\overline{OE}$ signal is used to control the direction of data flow from the RTS. For $\overline{OE}$ = 1, the RTS Data bus is three-state; for OE = 0, the RTS Data bus is active.
ILLCOM	K9	TDI	AH	Illegal Command. The host processor uses the ILLCOM input to inform the RTS that the present command is illegal.

STATUS OUTPUTS

NAME	PIN NUMBER (PGA)	TYPE	ACTIVE	DESCRIPTION
MERR [0]	A5	TO	AH	Message Error. The active high MERR output signals that the Message Error bit in the Status Register has been set due to receipt of an illegal command, or an error during message sequence. MERR will reset to logic zero on the receipt of the next valid command.
TXERR [0]	B5	TO	AH	Transmission Error. The active high TXERR output is asserted when the RTS detects an error in the reflected word versus the transmitted word, using the continuous loop-back compare feature. Reset on next $\overline{\text{COMSTR}}$ assertion.
$\overline{\text{TIMERON}}$ [1]	B6	TO	AL	Fail-safe Timer. The $\overline{\text{TIMERON}}$ output pulses low for 760µs when the RTS begins transmitting (i.e., rising edge of VALMSG) to provide a fail-safe timer meeting the requirements of MIL-STD-1553B. This pulse is reset when $\overline{\text{COMSTR}}$ goes low or during a Master Reset.
$\overline{\text{COMSTR}}$ [1]	B8	TO	AL	Command Strobe. $\overline{\text{COMSTR}}$ is an active low output of 500ns duration identifying receipt of a valid command.
$\overline{\text{BRDCST}}$ [1]	A7	TO	AL	Broadcast. $\overline{\text{BRDCST}}$ is an active low output that identifies receipt of a valid broadcast command.
RTRT [0]	B7	TO	AH	Remote Terminal to Remote Terminal. RTRT is an active high output indicating that the RTS is processing a remote terminal to remote terminal command.
DSCNCT or $\overline{\text{TERACT}}$ [X]	A6	TO	--	Disconnect or Terminal Active. Bit 11 of the Control Register selects the mode of this dual-function pin. In the "Disconnect" mode (bit 11 = 1), the active high DSCNCT output is asserted when all six Terminal Address pins (RTA0 - RTA4, RTPTY) go high, indicating a disconnect condition. In the "Terminal Active" mode (bit 11 = 0), the active low $\overline{\text{TERACT}}$ output is asserted at the beginning of the RTS access to internal RAM for a given command and negated after the last access for that command.
VALMSG [0]	L8	TO	AH	Valid Message. VALMSG is an active high output indicating a valid message (including Broadcast) has been received. VALMSG goes high prior to transmitting the 1553 status word and is reset upon receipt of the next command.
RBUSY [0]	C2	TO	AH	RTS Busy. RBUSY is asserted high while the RTS is accessing its own internal RAM either to read or update the pointers or to store or retrieve data words. RBUSY becomes active either 2.7µs or 5.7µs before RTS requires RAM access. This timing is controlled by Control Register bit 12 (see section 1.3).
T/$\overline{\text{R}}$ [0]	B4	TO	--	Transmit/Receive. A high level on this pin indicates a transmit command message transfer is being or was processed, while a low level indicates a receive command message transfer is being or was processed.

MODE CODE/SUBADDRESS OUTPUTS

NAME	PIN NUMBER (PGA)	TYPE	ACTIVE	DESCRIPTION
$\overline{MC}$/SA [0]	B1	TO	--	Mode Code/Subaddress Indicator. If $\overline{MC}$/SA is low, it indicates that the most recent command word is a mode code command. If $\overline{MC}$/SA is high, it indicates that the most recent command word is for a subaddress. This output indicates whether the mode code/subaddress ouputs (i.e., MCSA(4:0)) contain mode code or subaddress information.
MCSA0 [0]	B2	TO	--	Mode Code/Subaddress Output 0. If $\overline{MC}$/SA is low, this pin represents the least significant bit of the most recent command word (the LSB of the mode code). If $\overline{MC}$/SA is high, this pin represents the LSB of the subaddress.
MCSA1 [0]	A2	TO	--	Mode Code/Subaddress Output 1.
MCSA2 [0]	A3	TO	--	Mode Code/Subaddress Output 2.
MCSA3 [0]	B3	TO	--	Mode Code/Subaddress Output 3.
MCSA4 [0]	A4	TO	--	Mode Code/Subaddress Output 4. If $\overline{MC}$/SA is low, this pin represents the most significant bit of the mode code. If $\overline{MC}$/SA is high, this pin represents the MSB of the subaddress.

REMOTE TERMINAL ADDRESS INPUTS

NAME	PIN NUMBER (PGA)	TYPE	ACTIVE	DESCRIPTION
RTA4	L3	TUI	--	Remote Terminal Address bit 4 (MSB).
RTA3	K4	TUI	--	Remote Terminal Address bit 3.
RTA2	L4	TUI	--	Remote Terminal Address bit 2.
RTA1	K5	TUI	--	Remote Terminal Address bit 1.
RTA0	L5	TUI	--	Remote Terminal Address bit 0 (LSB).
RTPTY	K6	TUI	--	Remote Terminal Address Parity. This input must provide odd parity for the Remote Terminal Address.

BIPHASE INPUTS [1]

NAME	PIN NUMBER (PGA)	TYPE	ACTIVE	DESCRIPTION
RAZ	L7	TI	--	Receiver - Channel A, Zero Input. Idle low Manchester input form the 1553 bus receiver.
RAO	K8	TI	--	Receiver - Channel A, One Input. This input is the complement of RAZ.
RBZ	L6	TI	--	Receiver - Channel B, Zero Input. Idle low Manchester input from the 1553 bus receiver.
RBO	K7	TI	--	Receiver - Channel B, One Input. This input is the complement of RBZ.

Note:
1. For uniphase operation, tie RAZ (or RBZ) to V_{DD} and apply true uniphase input signal to RAO (or RBO).

BIPHASE OUTPUTS

NAME	PIN NUMBER (PGA)	TYPE	ACTIVE	DESCRIPTION
TAZ [0]	A10	TO	--	Transmitter - Channel A, Zero Output. This Manchester encoded data output is connected to the 1553 bus transmitter input. The output is idle low.
TAO [0]	B10	TO	--	Transmitter - Channel A, One Output. This output is the complement of TAZ. The output is idle low.
TBZ [0]	A9	TO	--	Transmitter - Channel B, Zero Output. This Manchester encoded data output is connected to the 1553 bus transmitter input. The output is idle low.
TBO [0]	B9	TO	--	Transmitter - Channel B, One Output. This output is the complement of TBZ. The output is idle low.

MASTER RESET AND CLOCK

NAME	PIN NUMBER (PGA)	TYPE	ACTIVE	DESCRIPTION
MRST	K3	TUI	AL	Master Reset. Initializes all internal functions of the RTS. $\overline{\text{MRST}}$ must be asserted 500ns before normal RTS operation (500ns minimum). Does not reset RAM.
12MHz	L2	TI	--	12 MHz Input Clock. This is the RTS system clock that requires an accuracy greater than 0.01% with a duty cycle of 50% ± 10%.
2MHz	A8	TO	--	2MHz Clock Output. This is a 2MHz clock output generated by the 12MHz input clock. This clock is stopped when $\overline{\text{MRST}}$ is low.

POWER AND GROUND

NAME	PIN NUMBER (PGA)	TYPE	ACTIVE	DESCRIPTION
V_{DD}	F10 E1	PWR PWR	-- --	+5 V_{DC} Power. Power supply must be +5 V_{DC} ± 10%.
V_{SS}	F2 G11	GND GND	-- --	Reference ground. Zero V_{DC} logic ground.

4.0 OPERATING CONDITIONS

ABSOLUTE MAXIMUM RATINGS*

(referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS	UNIT
V_{DD}	DC supply voltage	-0.3 to +7.0	V
V_{IO}	Voltage on any pin	-0.3 to V_{DD}+0.3	V
I_I	DC input current	±10	mA
T_{STG}	Storage temperature	-65 to +150	°C
P_D	Maximum power dissipation [1]	300	mW
T_J	Maximum junction temperature	+175	°C
Θ_{JC}	Thermal resistance, junction-to-case	20	°C/W

Note:

1. Does not reflect the added P_D due to an output short-circuited.

* Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS	UNIT
V_{DD}	DC supply voltage	4.5 to 5.5	V
V_{IN}	DC input voltage	0 to V_{DD}	V
T_C	Temperature range	-55 to +125	°C
F_O	Operating frequency	12 ±.01%	MHz

5.0 DC ELECTRICAL CHARACTERISTICS

V_{DD} = 5.0V ± 10%; -55°C < T_C <+125°C)

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V_{IL}	Low-level input voltage			0.8	V
V_{IH}	High-level input voltage		2.0		V
I_{IN}	Input leakage current TTL inputs Inputs with pull-down resistors Inputs with pull-up resistors	 $V_{IN} = V_{DD}$ or V_{SS} $V_{IN} = V_{DD}$ $V_{IN} = V_{SS}$	 -1 110 -2000	 1 2000 -110	 µA µA µA
V_{OL}	Low-level output voltage	I_{OL} = 3.2µA		0.4	V
V_{OH}	High-level output voltage	I_{OH} = -400µA	2.4		V
I_{OZ}	Three-state output leakage current	$V_O = V_{DD}$ or V_{SS}	-10	+10	µA
I_{OS}	Short-circuit output current [1, 2]	V_{DD} = 5.5V, $V_O = V_{DD}$ V_{DD} = 5.5V, V_O = 0V	 -90	90	mA mA
C_{IN}	Input capacitance [3]	*f* = 1MHz @ 0V		10	pF
C_{OUT}	Output capacitance [3]	*f* = 1MHz @ 0V		15	pF
C_{IO}	Bidirect I/O capacitance [3]	*f* = 1MHz @ 0V		20	pF
I_{DD}	Average operating current [1, 4]	*f* = 12MHz, CL = 50pF		50	mA
QI_{DD}	Quiescent current	Note 5		1.5	mA

Notes:
1. Supplied as a design limit but not guaranteed or tested.
2. Not more than one output may be shorted at a time for a maximum duration of one second.
3. Measured only for initial qualification, and after process or design changes that could affect input/output capacitance.
4. Includes current through input pull-ups. Instantaneous surge currents on the order of 1 ampere can occur during output switching. Voltage supply should be adequately sized and decoupled to handle a large surge current.
5. All inputs with internal pull-ups or pull-downs should be left open circuit. All other inputs tied high or low.

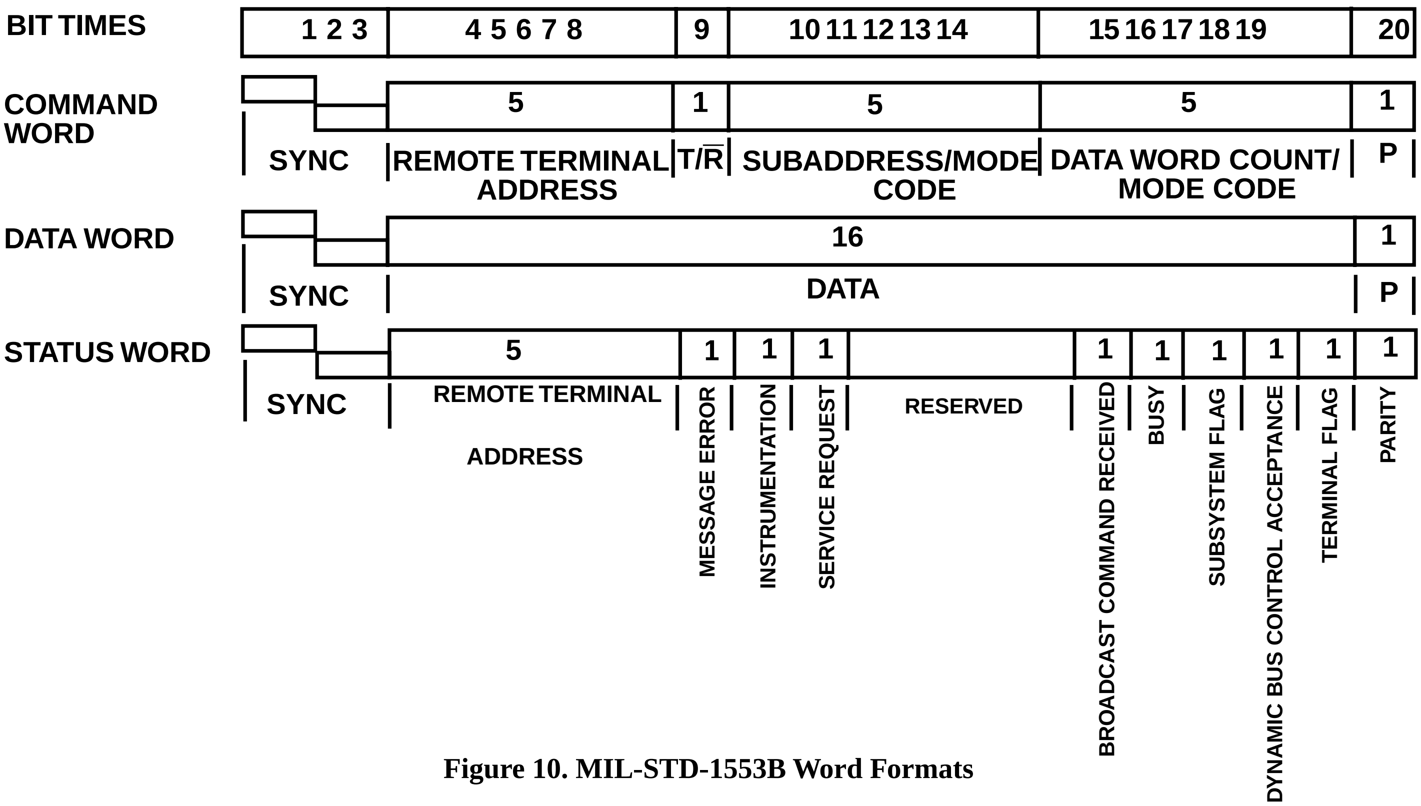
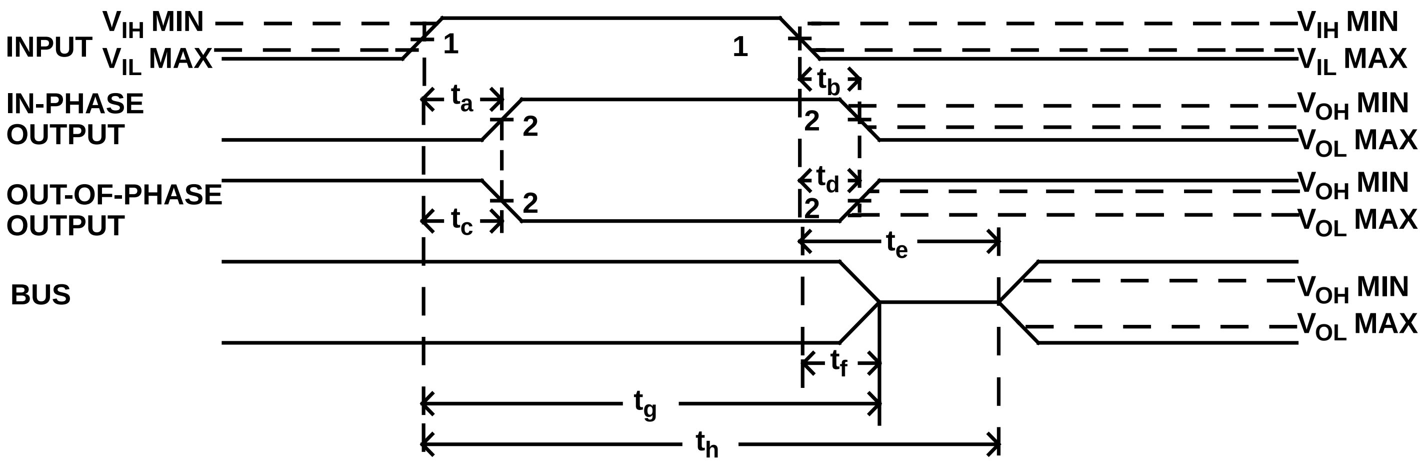


Figure 10. MIL-STD-1553B Word Formats

6.0 AC Electrical Characteristics

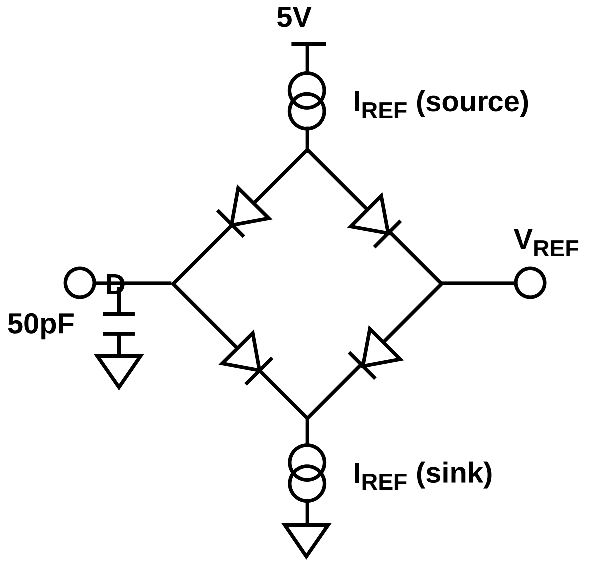
(Over recommended operating conditions)



SYMBOL	PARAMETER
t_a	INPUT↑ to response ↑
t_b	INPUT↓ to response ↓
t_c	INPUT↑ to response ↓
t_d	INPUT↓ to response ↑
t_e	INPUT↓ to data valid
t_f	INPUT↓ to high Z
t_g	INPUT↑ to high Z
t_h	INPUT↑ to data valid

Notes:
1. Timing measurements made at (V_{IH} MIN + V_{IL} MAX)/2.
2. Timing measurements made at (V_{OL} MAX + V_{OH} MIN)/2.
3. Based on 50pf load.
4. Unless otherwise noted, all AC electrical characteristics are guaranteed by design or characterization.

Figure 11a. Typical Timing Measurements



Note:
50pF including scope probe and test socket

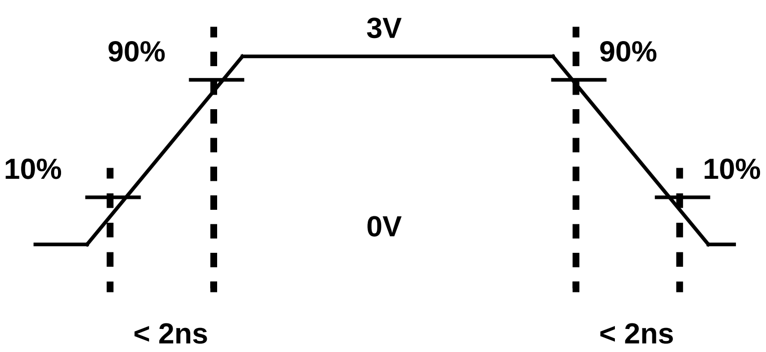


Figure 11b. AC Test Loads and Input Waveforms

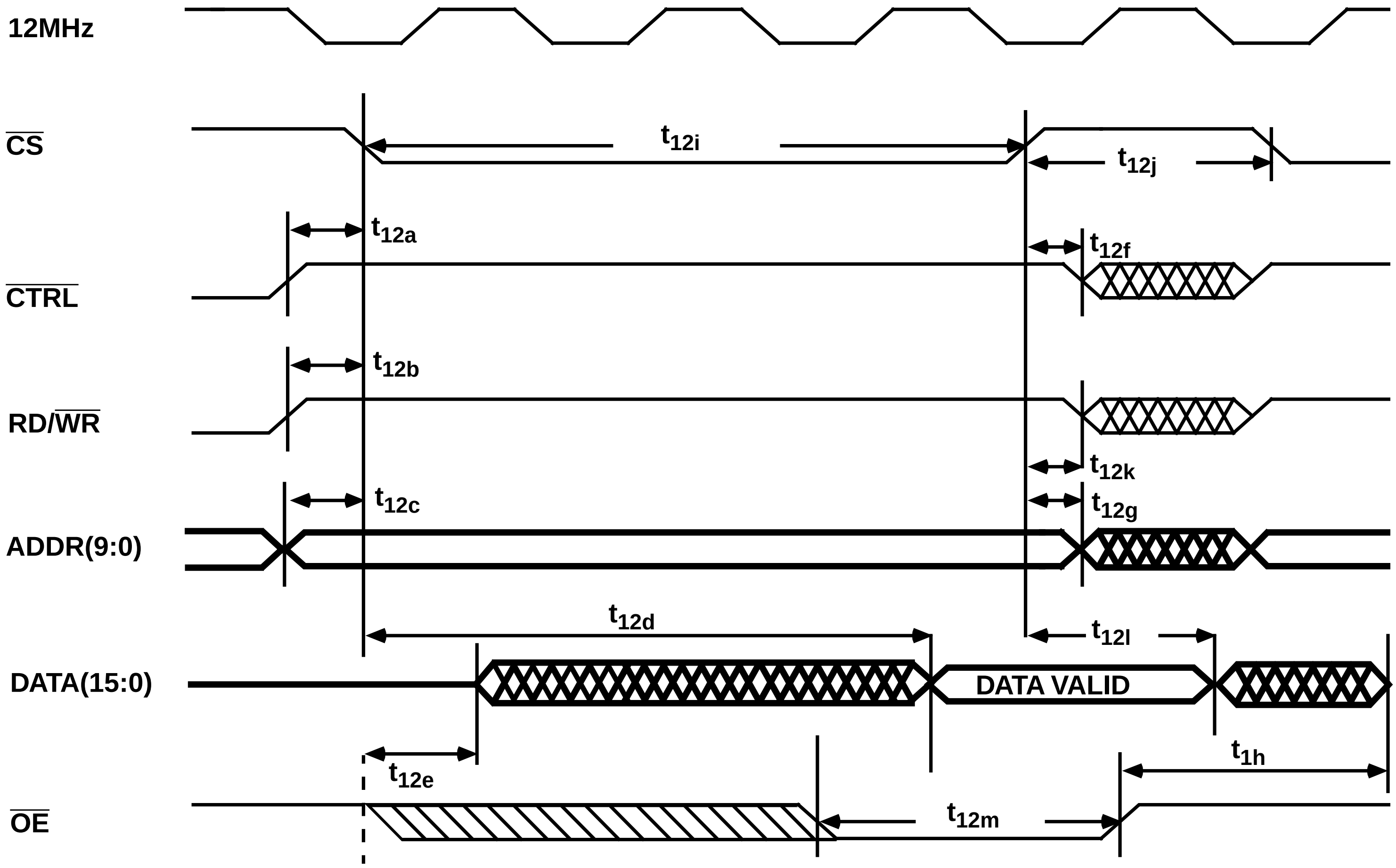


Figure 12. Microprocessor RAM Read

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{12a}	$\overline{CTRL}$↑ set up wrt $\overline{CS}$↓ [1]	10	--	ns
t_{12b}	RD/$\overline{WR}$ ↑ set up wrt $\overline{CS}$↓	10	--	ns
t_{12c}	ADDR(9:0) Valid to $\overline{CS}$↓ (Address Set up)	10	--	ns
t_{12d}	$\overline{CS}$↓ to DATA(15:0) Valid	--	155	ns
t_{12e}	$\overline{OE}$↓ to DATA(15:0) Don't Care (Active)	--	65	ns
t_{12f}	$\overline{CS}$↑ to $\overline{CTRL}$ Don't Care	0	--	ns
t_{12g}	$\overline{CS}$↑ to ADDR(9:0) Don't Care	0	--	ns
t_{12h}	$\overline{OE}$↑ to DATA(15:0) High Impedance	--	40	ns
t_{12i}	$\overline{CS}$↓ to $\overline{CS}$↑ [2]	220	5500	ns
t_{12j}	$\overline{CS}$↑ to $\overline{CS}$↓	85	--	ns
t_{12k}	$\overline{CS}$↑ to RD/$\overline{WR}$ Don't Care	0	--	ns
t_{12l}	$\overline{CS}$↑ to DATA(15:0) Invalid [3]	25	--	ns
t_{12m}	$\overline{OE}$↓ to $\overline{OE}$↑	65	--	ns

Notes:

1. "wrt" defined as "with respect to."
2. The maximum amount of time that $\overline{CS}$ can be held low is 5500ns if the user has selected the 5.7µs RBUSY option. For the 2.7µs RBUSY option, the maximum $\overline{CS}$ low time is 2500ns.
3. Assumes $\overline{OE}$ is asserted.

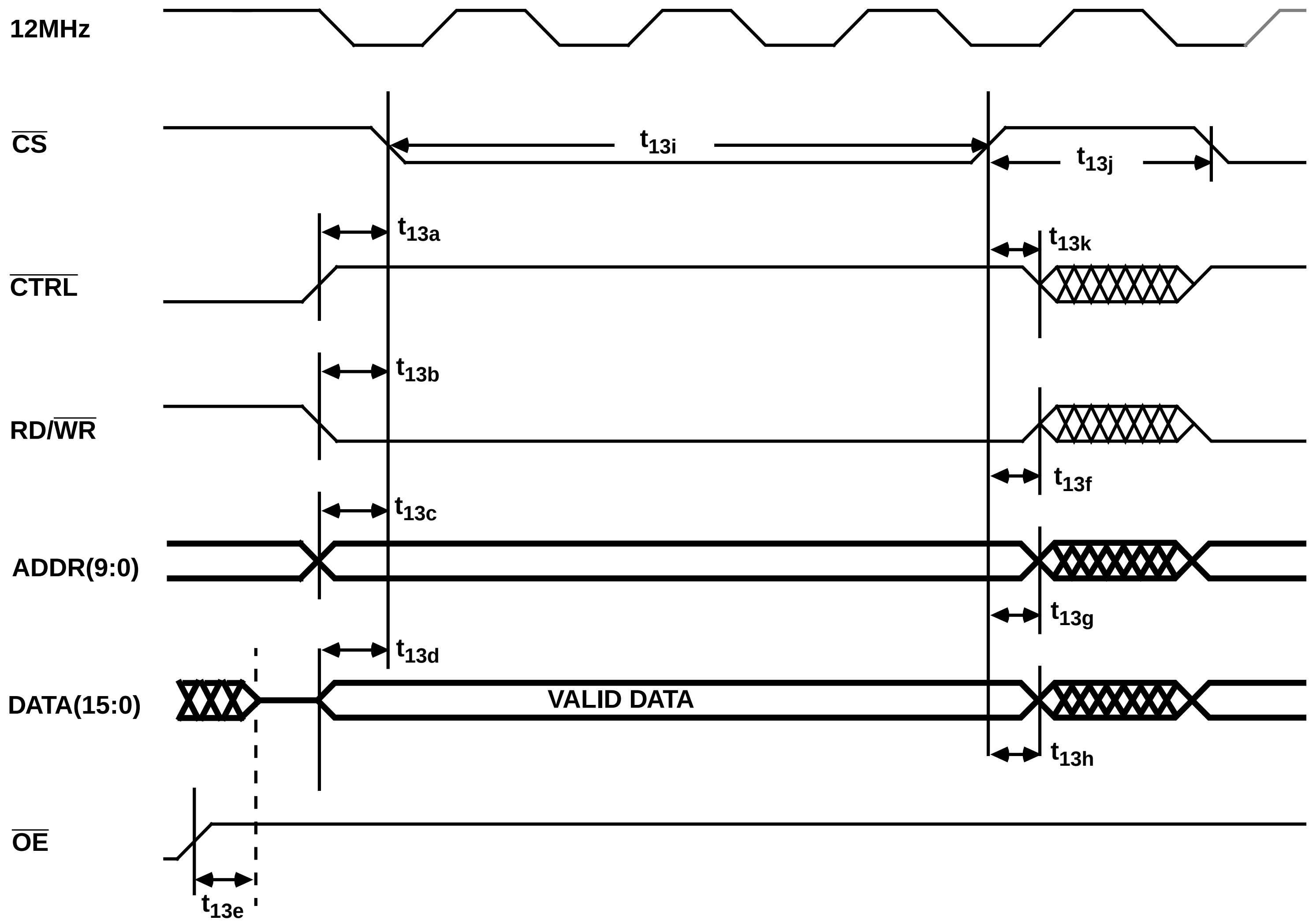


Figure 13. Microprocessor RAM Write

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{13a}	$\overline{\text{CTRL}}$↑ set up wrt $\overline{\text{CS}}$↓	10	--	ns
t_{13b}	RD/$\overline{\text{WR}}$ ↑ set up wrt $\overline{\text{CS}}$↓	10	--	ns
t_{13c}	ADDR(9:0) Valid to $\overline{\text{CS}}$↓ (Address set up)	10	--	ns
t_{13d}	$\overline{\text{CS}}$↓ to DATA(15:0) Valid $\overline{\text{CS}}$↓(DATA set up)	0	--	ns
t_{13e}	$\overline{\text{OE}}$↓ to DATA(15:0) High Impedance	40	--	ns
t_{13f}	$\overline{\text{CS}}$↑ to RD/$\overline{\text{WR}}$ Don't Care	0	--	ns
t_{13g}	$\overline{\text{CS}}$↑ to ADDR(9:0) Don't Care	0	--	ns
t_{13h}	$\overline{\text{CS}}$↑ to DATA(15:0) Don't Care (Hold-time)	20	--	ns
t_{13i}	$\overline{\text{CS}}$↓ to $\overline{\text{CS}}$↑ [1]	180	5500	ns
t_{13j}	$\overline{\text{CS}}$↑ to $\overline{\text{CS}}$↓	85	--	ns
t_{13k}	$\overline{\text{CS}}$↑ to $\overline{\text{CTRL}}$ Don't Care	0	--	ns

Note:

1. The maximum amount of time that $\overline{\text{CS}}$ can be held low is 5500ns if the user has selected the 5.7µs RBUSY option. For the 2.7µs RBUSY option, the maximum $\overline{\text{CS}}$ low time is 2500ns.

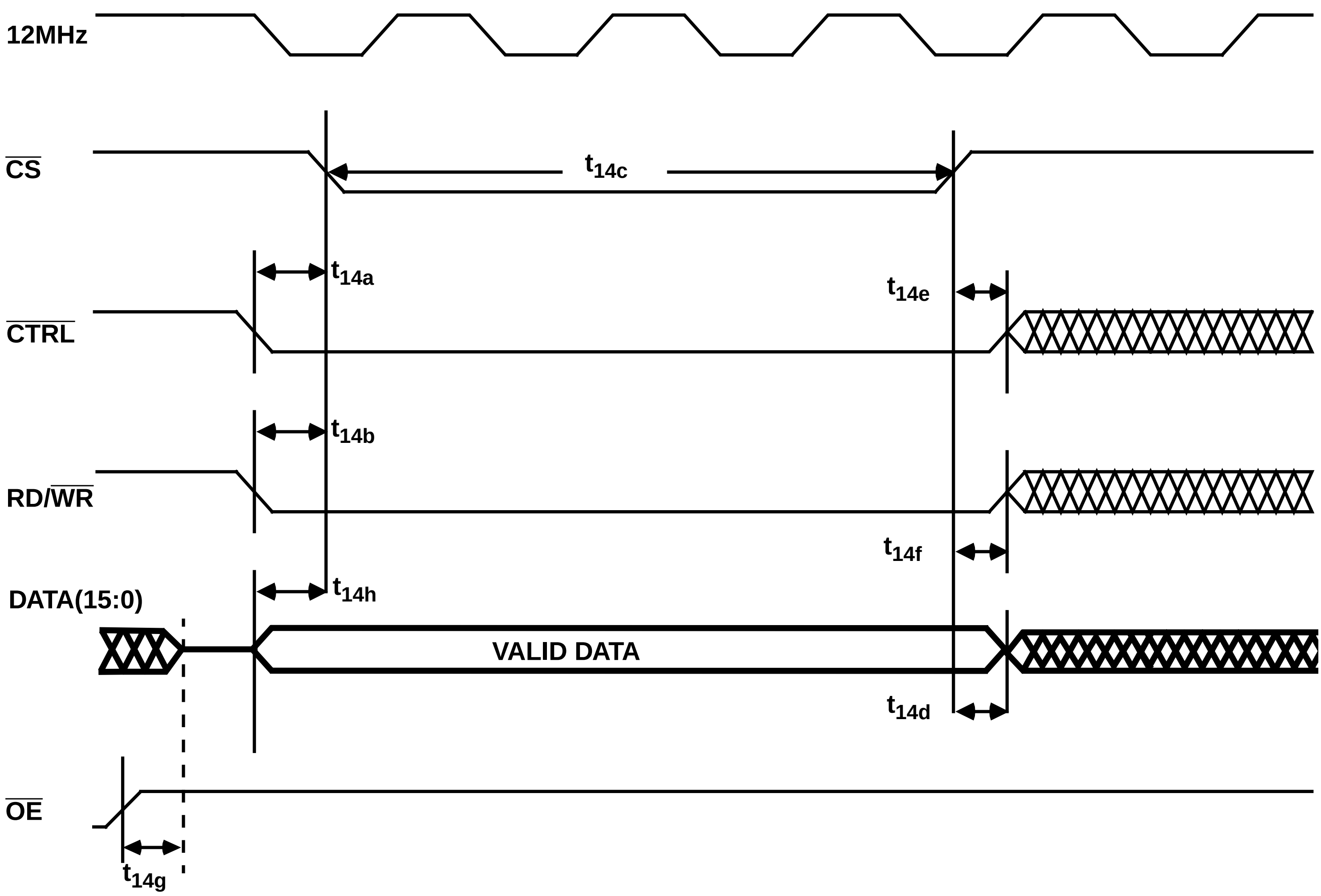


Figure 14. Control Register Write

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{14a}	CTRL↓ set up wrt CS↓	0	--	ns
t_{14b}	RD/WR ↓ set up wrt CS↓	0	--	ns
t_{14c}	CS↓ to CS↑ [1]	50	5500	ns
t_{14d}	CS↑ to DATA(15:0) Don't Care (Hold-time)	0	--	ns
t_{14e}	CS↑ to CTRL Don't Care	0	--	ns
t_{14f}	CS↑ to RD/WR Don't Care	0	--	ns
t_{14g}	OE↑ to Data(15:0) High Impedance	40	--	ns
t_{14h}	DATA (15:0) Valid to CS↓ (DATA set up)	0	--	ns

Note:

1. The maximum amount of time that CS can be held low is 5500ns if the user has selected the 5.7µs RBUSY option. For the 2.7µs RBUSY option, the maximum CS low time is 2500ns.

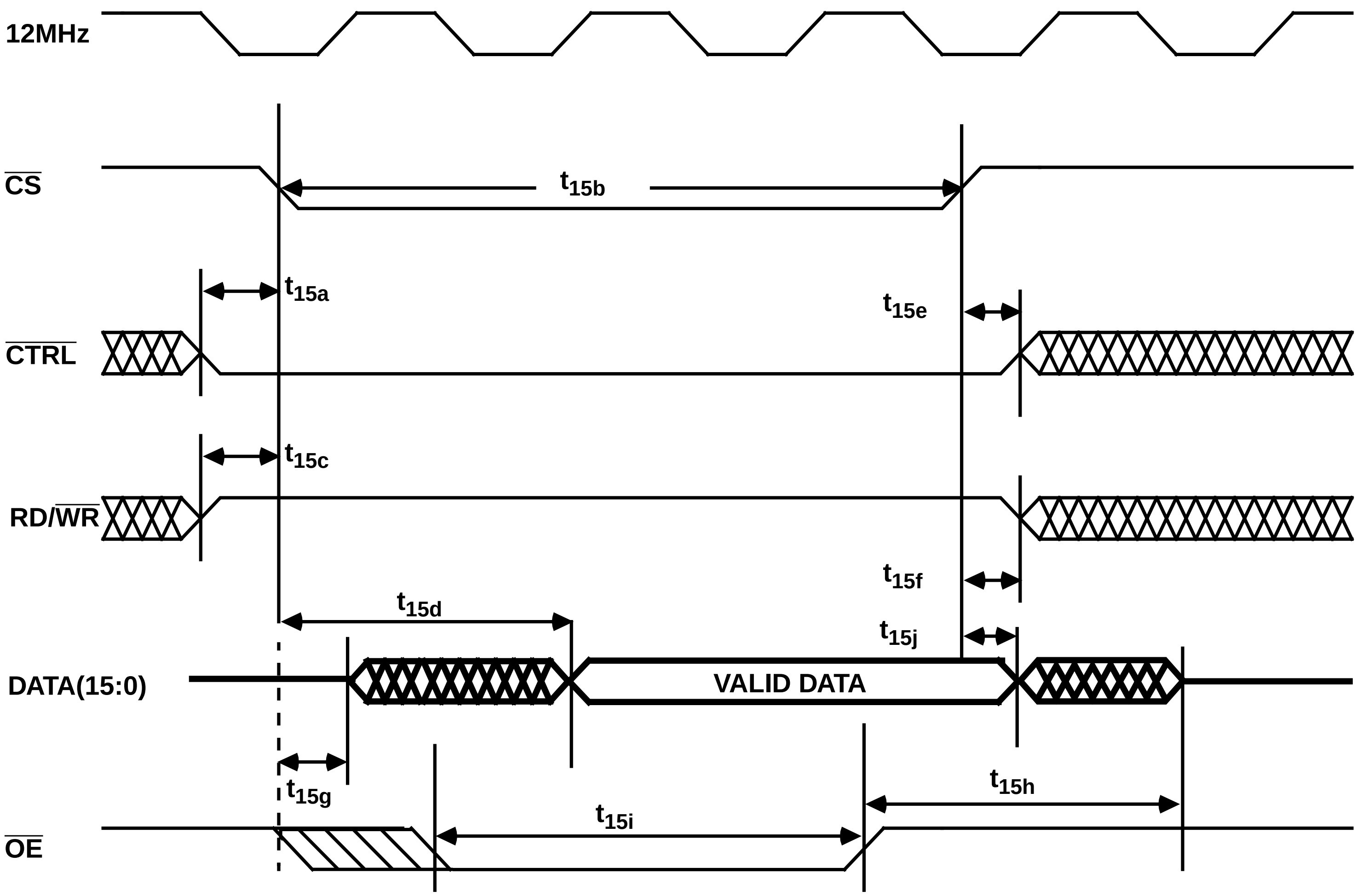


Figure 15. Status Register Read

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{15a}	CTRL↓ set up wrt CS↓	0	--	ns
t_{15b}	CS↓ to CS↑[1]	65	5500	ns
t_{15c}	RD/WR↑ set up wrt CS↓	0	--	ns
t_{15d}	CS↓ to DATA(15:0) Valid	--	65	ns
t_{15e}	CS↑ to CTRL Don't Care	5	--	ns
t_{15f}	CS↑ to RD/WR Don't Care	5	--	ns
t_{15g}	OE↓ to DATA(15:0) Don't Care (Active)	--	65	ns
t_{15h}	OE↑ to DATA(15:0) High Impedance	--	40	ns
t_{15i}	OE↓ to OE↑	65	--	ns
t_{15j}	CS↓ to DATA(15:0) Don't Care (Active)	25	--	ns

Note:

1. The maximum amount of time that CS can be held low is 5500ns if the user has selected the 5.7µs RBUSY option. For the 2.7µs RBUSY option, the maximum CS low time is 2500ns.

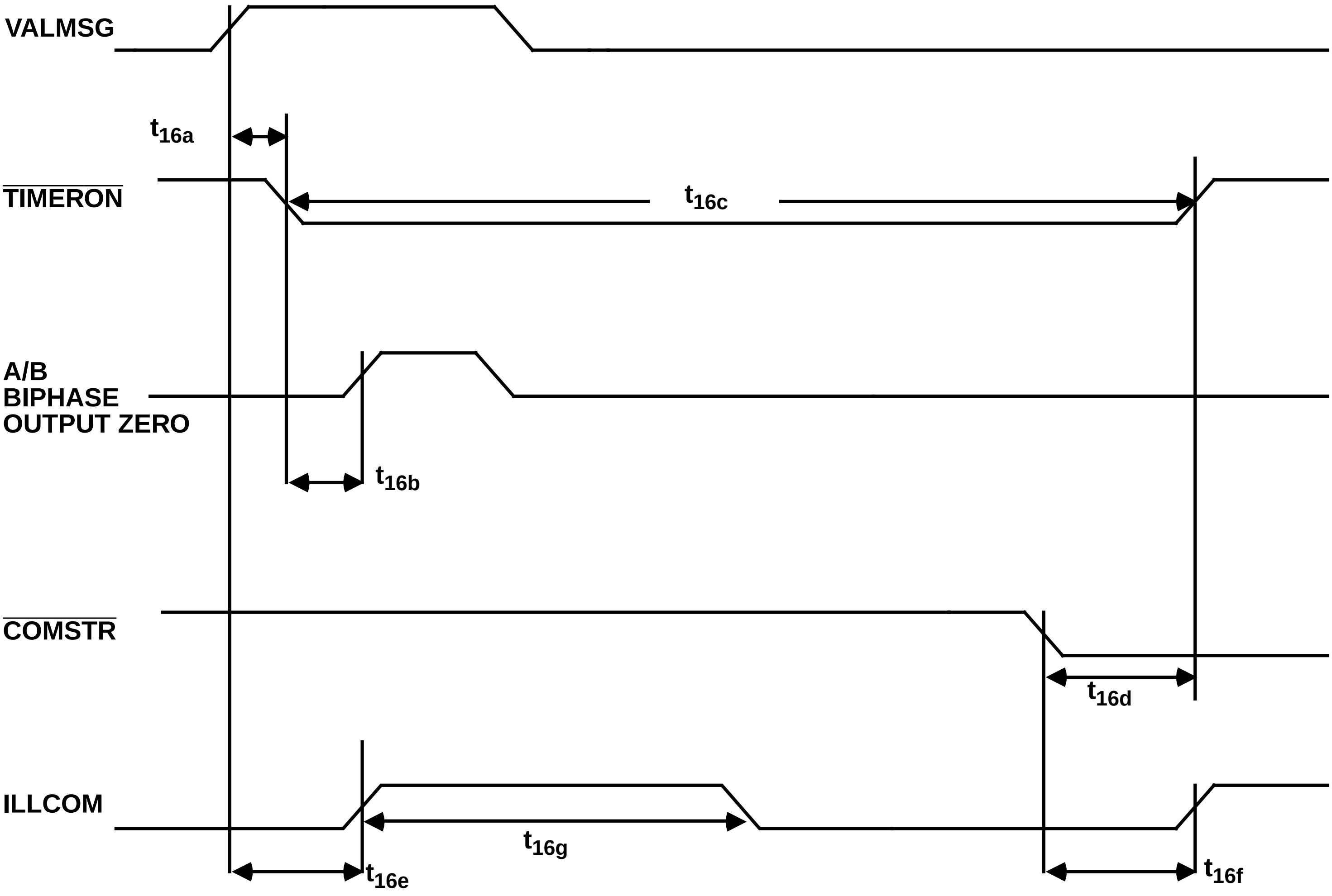
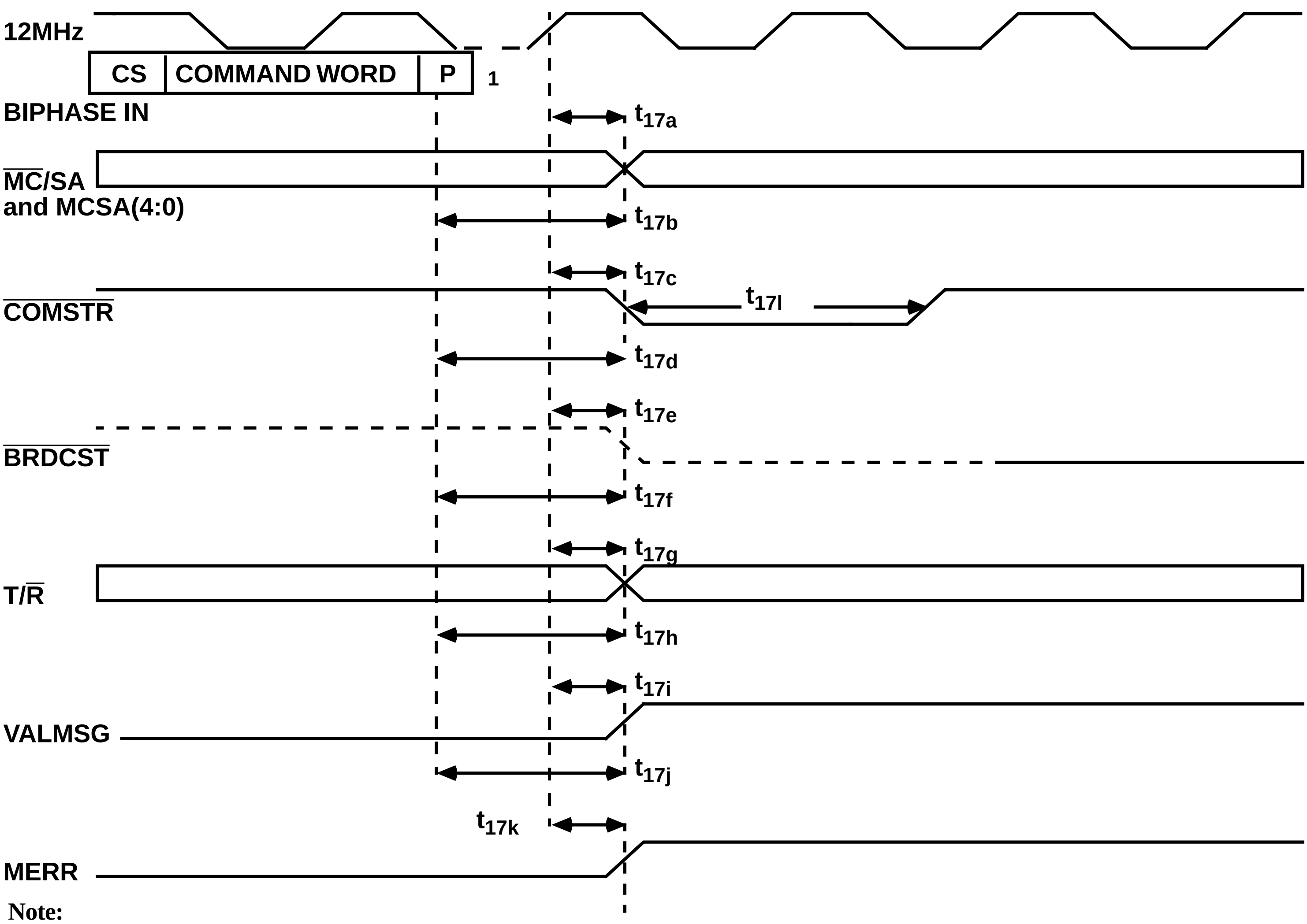


Figure 16. RT Fail-Safe Timer Signal Relationships

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{16a}	VALMSG↑ before $\overline{\text{TIMERON}}$↓	0	35	ns
t_{16b}	$\overline{\text{TIMERON}}$↓ before first BIPHASE OUT O↑	1.2	--	µs
t_{16c}	$\overline{\text{TIMERON}}$ low pulse width (time-out)	727.3	727.4	µs
t_{16d}	$\overline{\text{COMSTR}}$↓ to $\overline{\text{TIMERON}}$↑	--	25	ns
t_{16e}	VALMSG↑ to ILLCOM↑	--	3.3	µs
t_{16f}	$\overline{\text{COMSTR}}$↓ to ILLCOM↑ [1]	--	664	ns
t_{16f}	$\overline{\text{COMSTR}}$↓ to ILLCOM↑ [2]	--	18.2	µs
t_{16g}	ILLCOM↑ to ILLCOM↓ [3]	500	--	ns

Notes:
1. Mode code 2, 4, 5, 6, 7, or 18 received.
2. To suppress data word storage.
3. For transmit command illegalization.



Note:

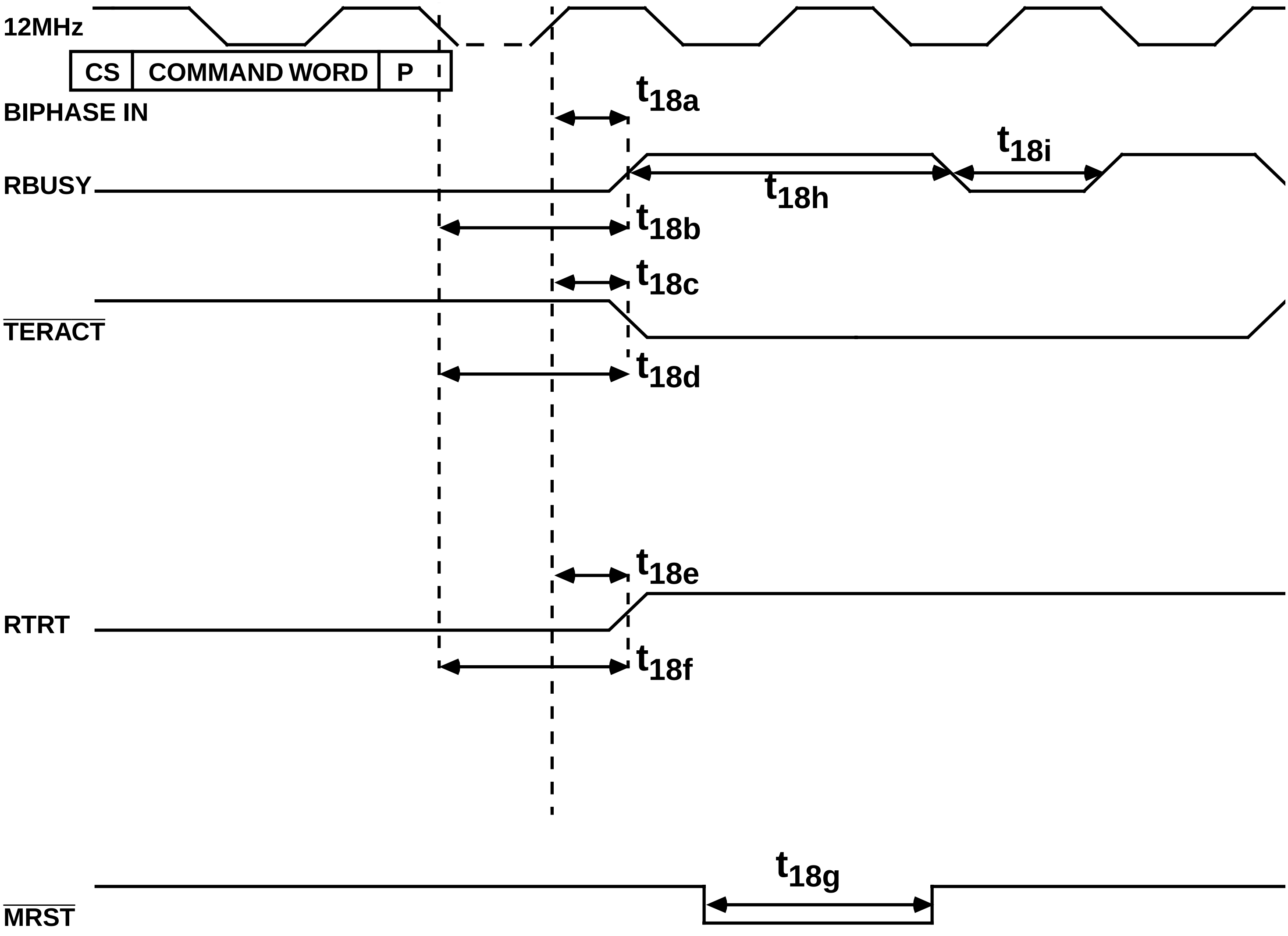
1. Measured from the mid-bit parity crossing.

Figure 17. Status Output Timing

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{17a} [4]	12Mhz↑ to $\overline{MC}$/SA Valid	0	14	ns
t_{17b}	Command Word to $\overline{MC}$/SA Valid[3]	2.1	2.8	µs
t_{17c} [4]	12MHz↑ to $\overline{COMSTR}$↓	0	17	ns
t_{17d}	Command Word to $\overline{COMSTR}$↓[3]	3.2	3.7	µs
t_{17e} [4]	12MHz↑ to $\overline{BRDCST}$↓	0	32	ns
t_{17f}	Command Word to $\overline{BRDCST}$↓[3]	2.6	3.2	µs
t_{17g} [4]	12MHz↑ to T/$\overline{R}$ Valid	0	57	ns
t_{17h}	Command Word toT/$\overline{R}$ Valid[3]	2.2	2.7	µs
t_{17i} [4]	12MHz↑ to VALMSG↑	0	32	ns
t_{17j}	Command Word toVALMSG↑ [1,2,3]	6.2	6.7	µs
t_{17k} [4]	12MHz↑ to MERR↑	0	37	ns
t_{17l}	$\overline{COMSTR}$↓ TO $\overline{COMSTR}$↑	485	500	ns

Notes:

1. Receive last data word to Valid Message active (VALMSG↑).
2. Transmit command word to Valid Message active (VALMSG↑).
3. Command word measured from mid-bit crossing.
4. Guaranteed by test.

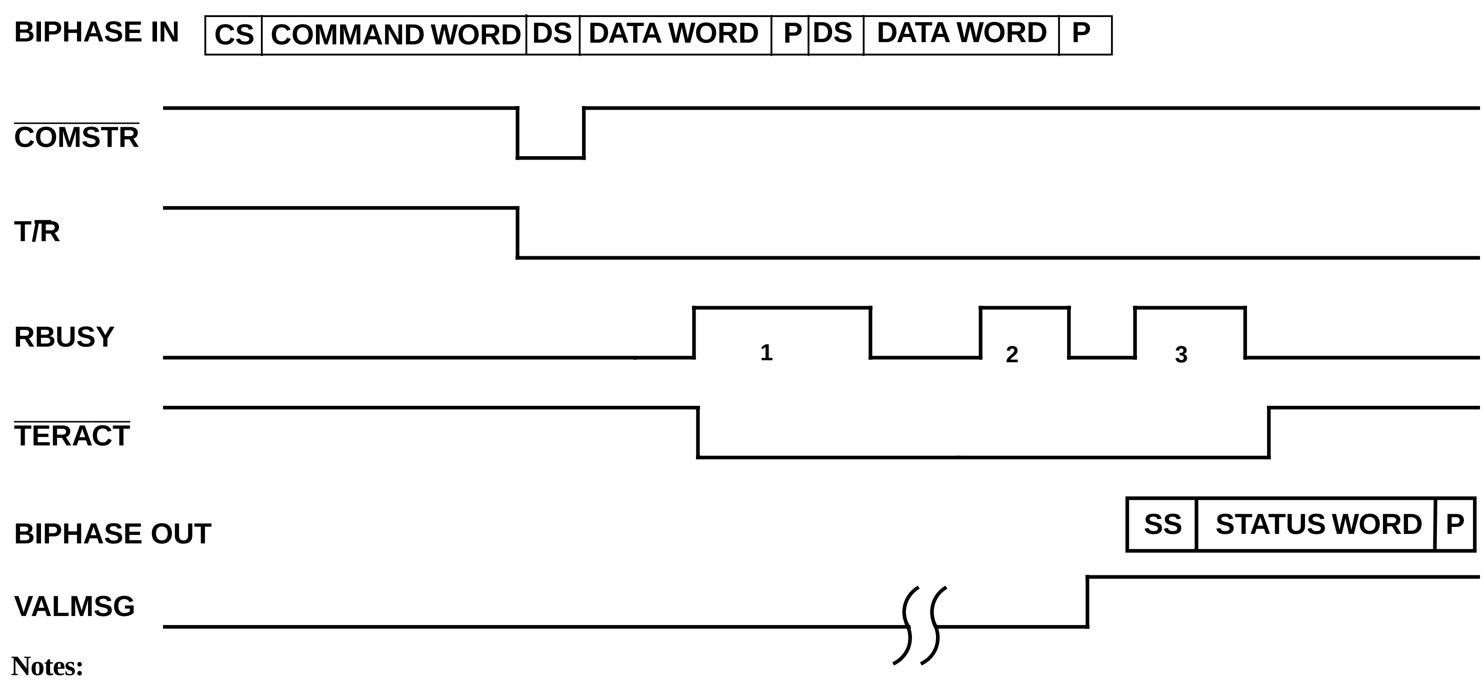


Note:
1. Measured from mid-bit parity crossing.

Figure 18. Status Output Timing

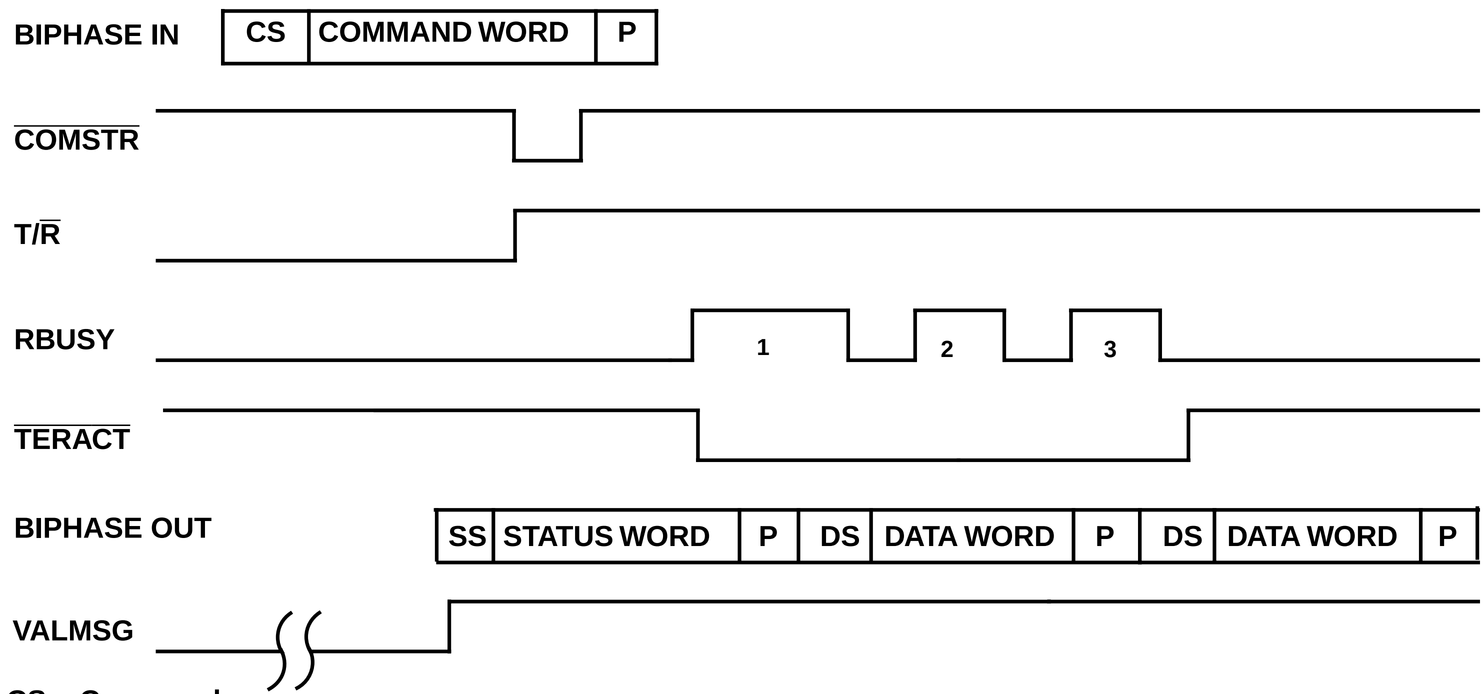
SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{18a}	12MHz↑ to RBUSY↑	--	37	ns
t_{18b}	Command Word toRBUSY↑ [3]	3.2	3.8	µs
t_{18c} [2]	12MHz↑ to $\overline{\text{TERACT}}$↓	0	37	ns
t_{18d}	Command Word to $\overline{\text{TERACT}}$↓ [1,3]	3.1	3.7	µs
t_{18e} 2	12MHz↑ to RTRT↑	0	32	ns
t_{18f}	Command Word to RTRT↑ [3]	21.0	22	µs
t_{18g}	MRST↓ to $\overline{\text{MRST}}$↑	500	--	ns
t_{18h}	RBUSY↑ to RBUSY↓ (2.7µs) (5.7µs)	-- --	5.5 8.5	µs µs
t_{18i}	RBUSY↓ to RBUSY↑ (2.7µs) (5.7µs)	3.10 240	-- --	µs ns

Notes:
1. $\overline{\text{TERACT}}$ enabled via Control Register.
2. Guaranteed by test.
3. Command word measured from mid-bit crossing



Notes:
1. Burst of 5 DMAs: read command pointer, store command word, update command pointer, read data word pointer, store command word.
2. Burst of 1 DMA: store data word.
3. Burst of 2 DMAs: store data word, update data word pointer.
4. Approximately 560ns per DMA access.

Figure 19a. Receive Command with Two Data Words



CS = Command sync
SS = Status sync
DS = Data sync
P = Parity

Notes:
1. Burst of 4 DMAs: read command pointer, store command word, update command pointer, read data word pointer.
2. Burst of 1 DMA: read data word.
3. Burst of 2 DMAs: read data word, update data word pointer.
4. Approximately 560ns per DMA access.

Figure 19b. Transmit Command with Two Data Words

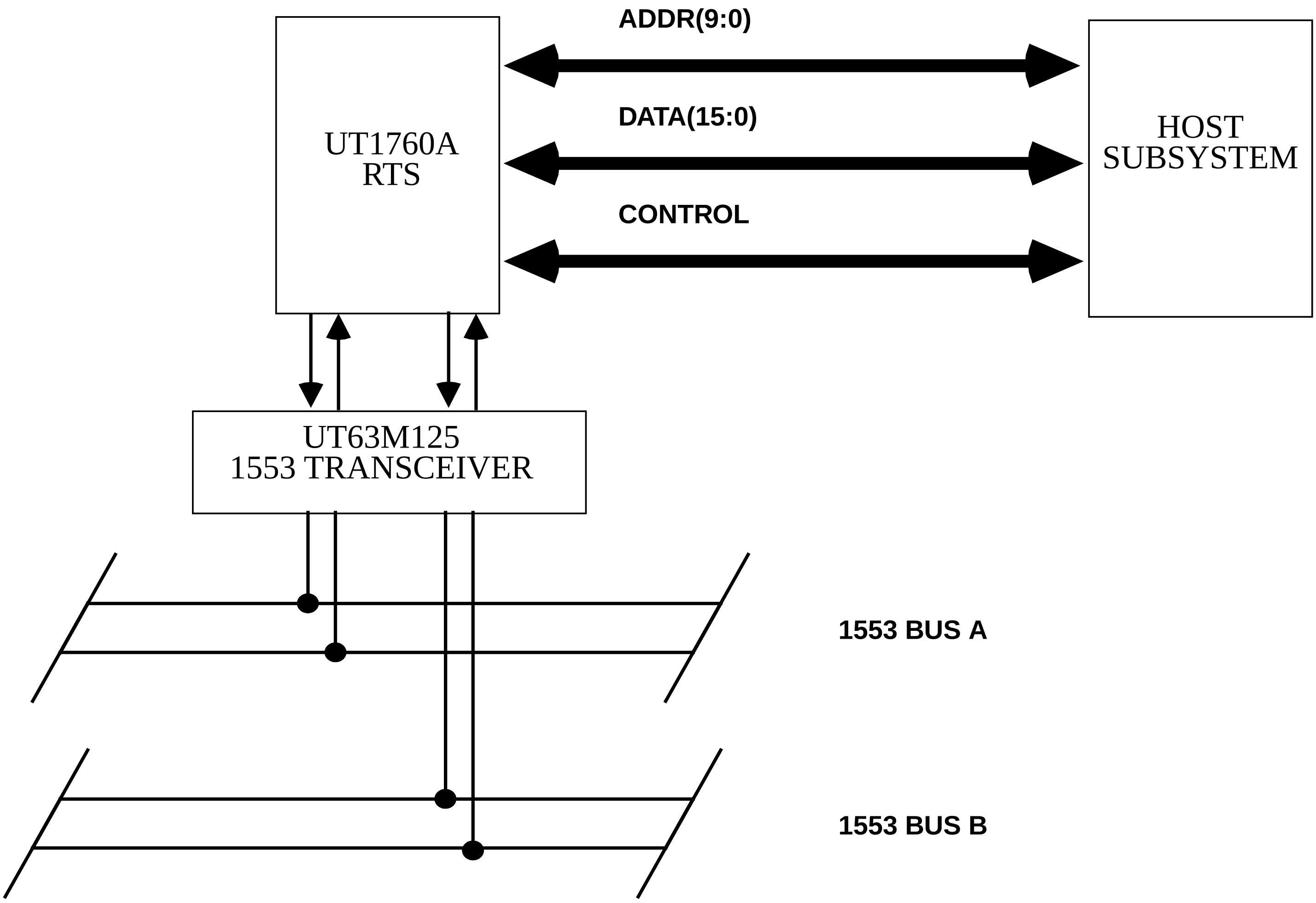


Figure 20a. RTS General System Diagram (Idle low interface)

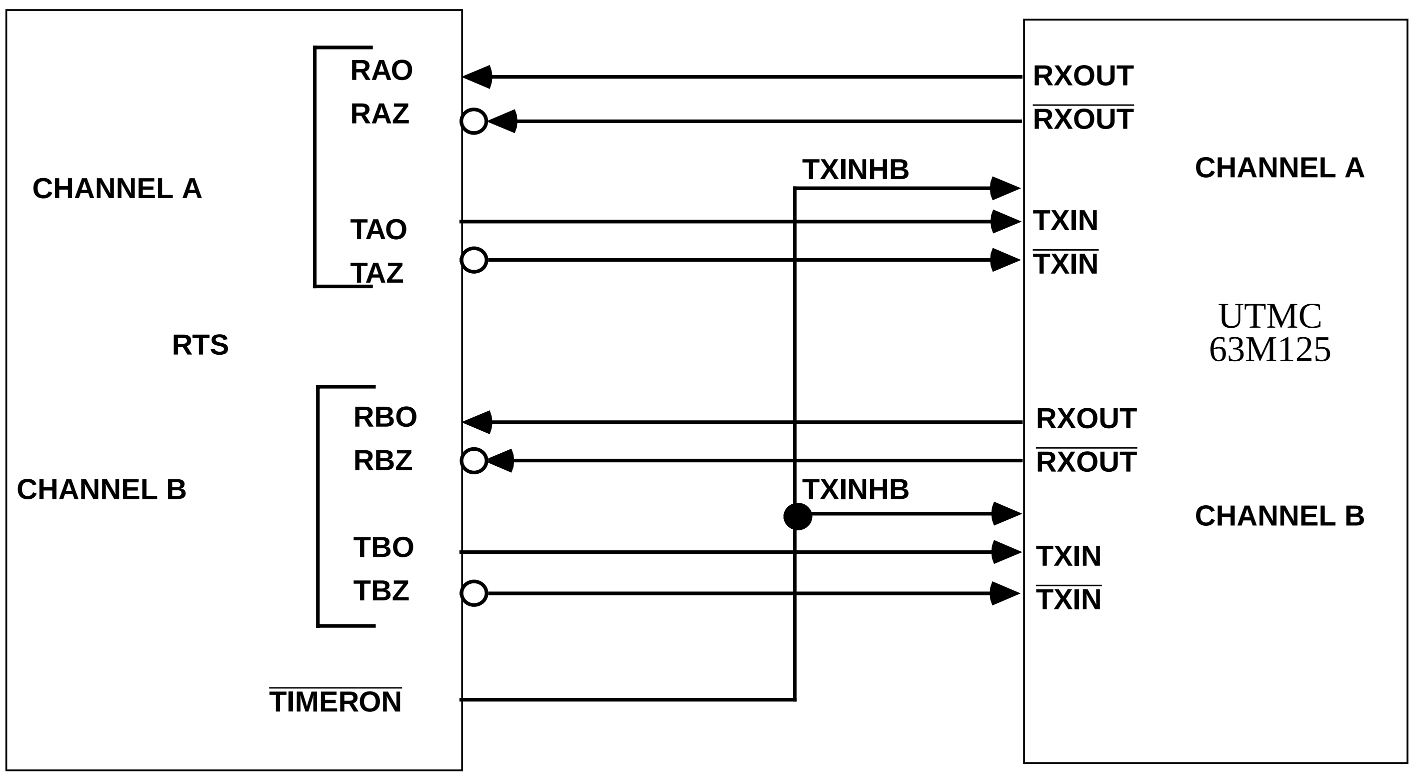


Figure 20b. RTS Transceiver Interface Diagram

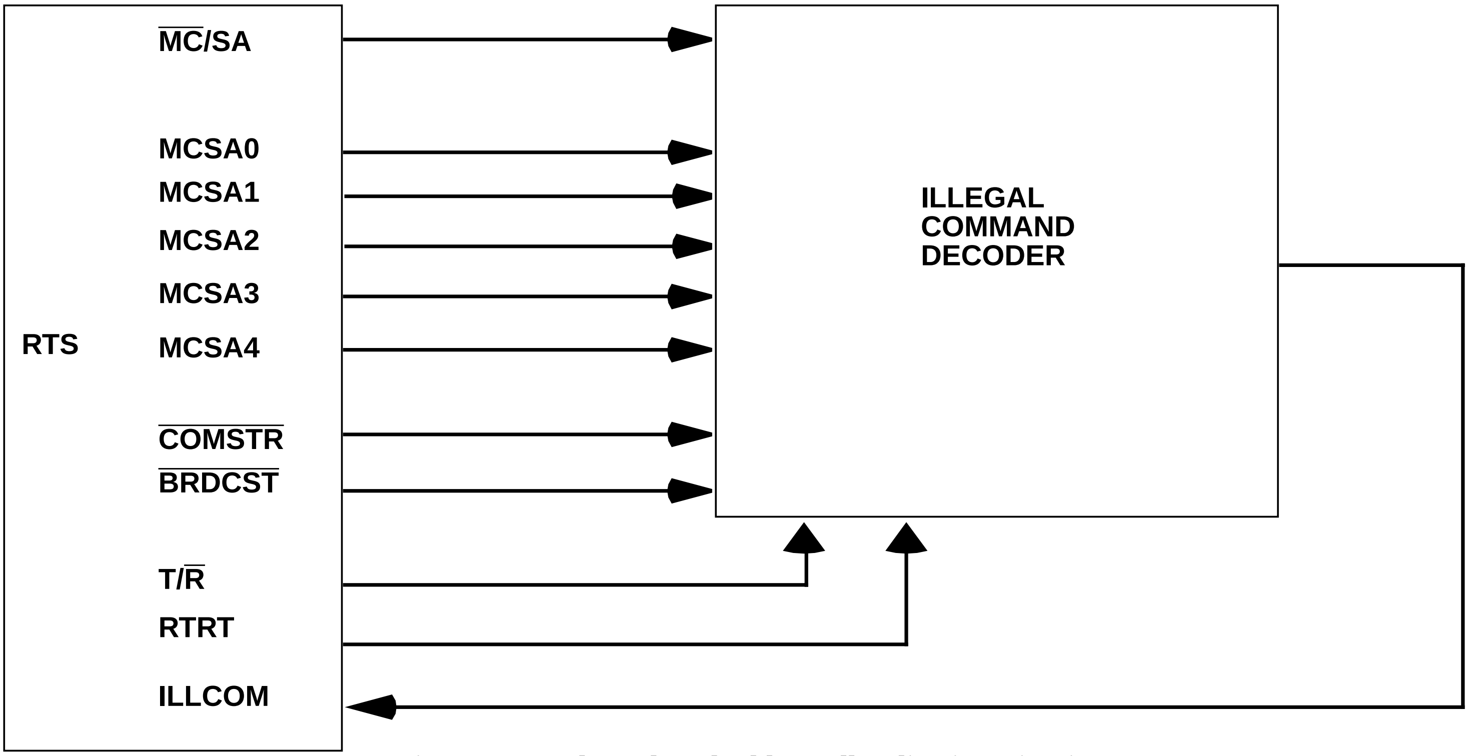
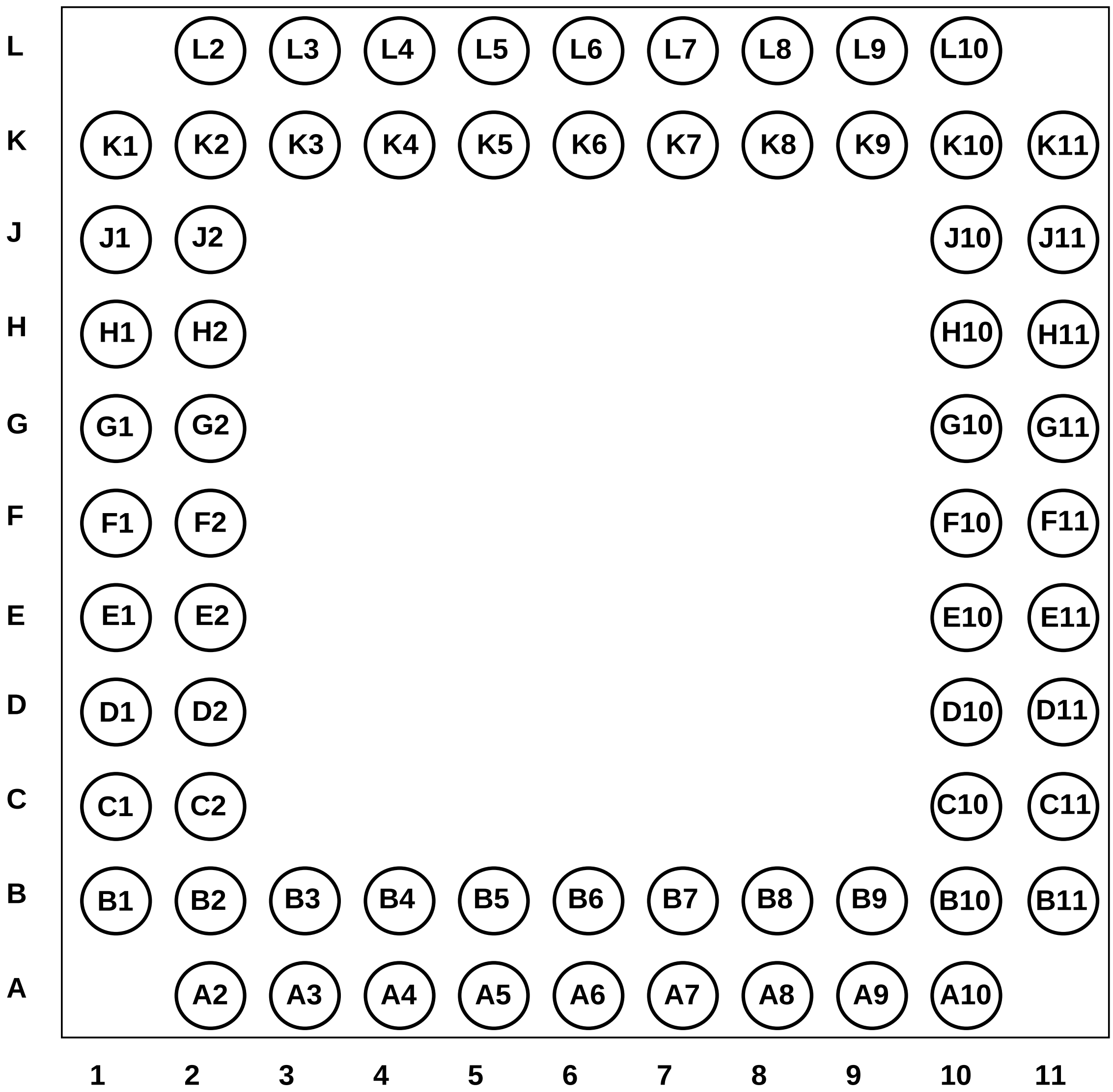


Figure 21. Mode Code/Subaddress Illegalization Circuit

7.0 Package Outline Drawing



Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A2	MCSA1	C1	ADDR9	G1	ADDR3	K1	RD/$\overline{WR}$
A3	MCSA2	C2	RBUSY	G2	ADDR4	K2	$\overline{CS}$
A4	MCSA4	C10	DATA13	G10	DATA7	K3	$\overline{MRST}$
A5	MERR	C11	DATA14	G11	V_{SS}	K4	RTA3
A6	$\overline{TERACT}$ or DSCNCT	D1	ADDR7	H1	ADDR1	K5	RTA1
A7	$\overline{BRDCST}$	D2	ADDR8	H2	ADDR2	K6	RTPTY
A8	2MHz	D10	DATA11	H10	DATA5	K7	RBO
A9	TBZ	D11	DATA12	H11	DATA6	K8	RAO
A10	TAZ	E1	V_{DD}	J1	$\overline{CTRL}$	K9	ILLCOM
B1	$\overline{MC}$/SA	E2	ADDR6	J2	ADDR0	K10	DATA1
B2	MCSA0	E10	DATA9			K11	DATA2
B3	MCSA3	E11	DATA10			L2	12MHz
B4	T/$\overline{R}$	F1	ADDR5			L3	RTA4
B5	TXERR					L4	RTA2
B6	$\overline{TIMERON}$					L5	RTA0
B7	RTRT					L6	RBZ
B8	$\overline{COMSTR}$					L7	RAZ
						L8	VALMSG

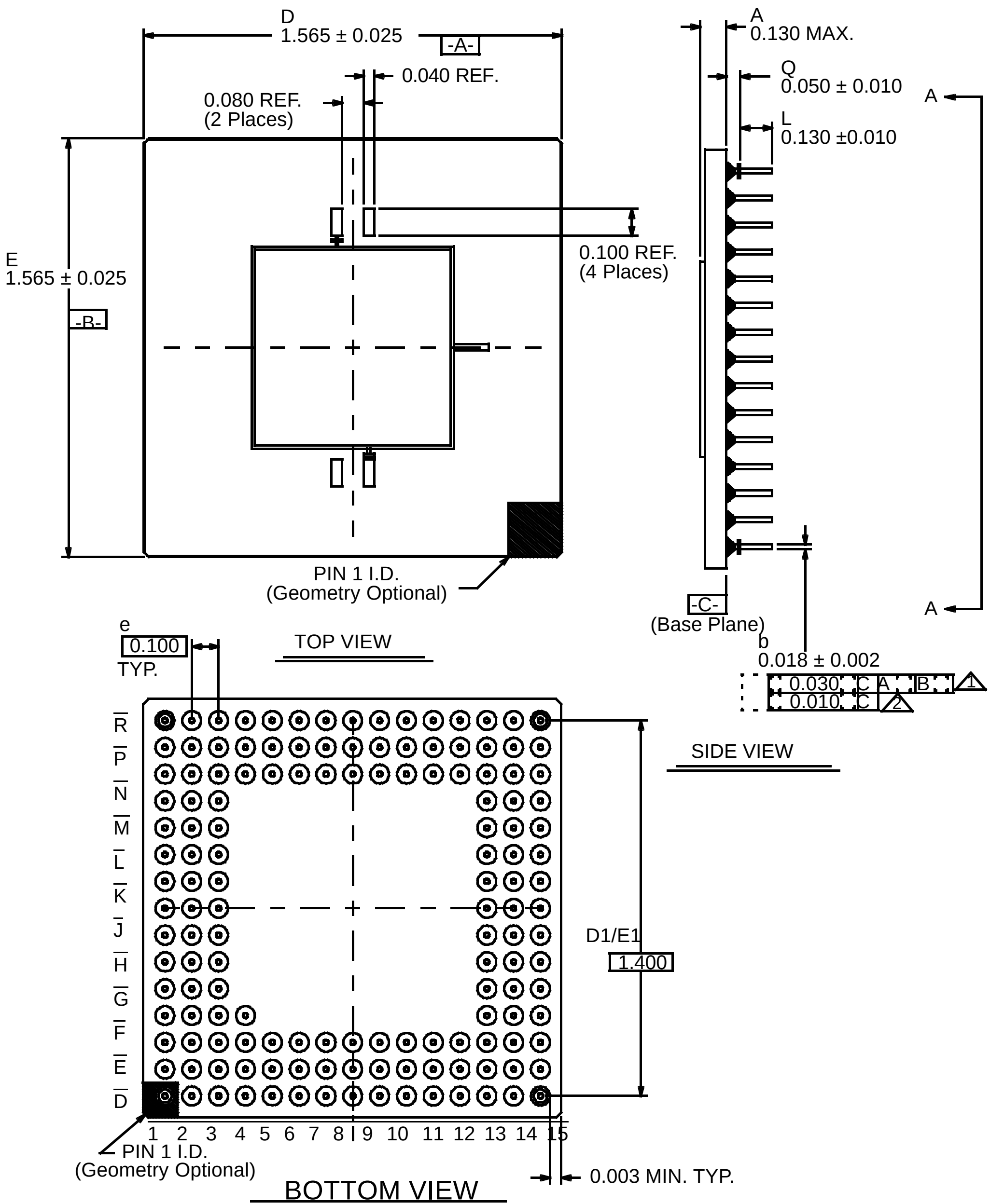
Figure 22. UT1760A RTS Pingrid Array Configuration (Bottom View)

Package Selection Guide

Product								
	RTI	RTMP	RTR	BCRT	BCRTM	BCRTMP	RTS	XCVR
24-pin DIP (single cavity)								X
36-pin DIP (dual cavity)								X
68-pin PGA			X				X	
84-pin PGA	X	X		X	X[1]			
144-pin PGA						X		
84-lead LCC		X		X	X[1]			
36-lead FP (dual cavity) (50-mil ctr)								X
84-lead FP				X	X			
132-lead FP				X		X		

NOTE:

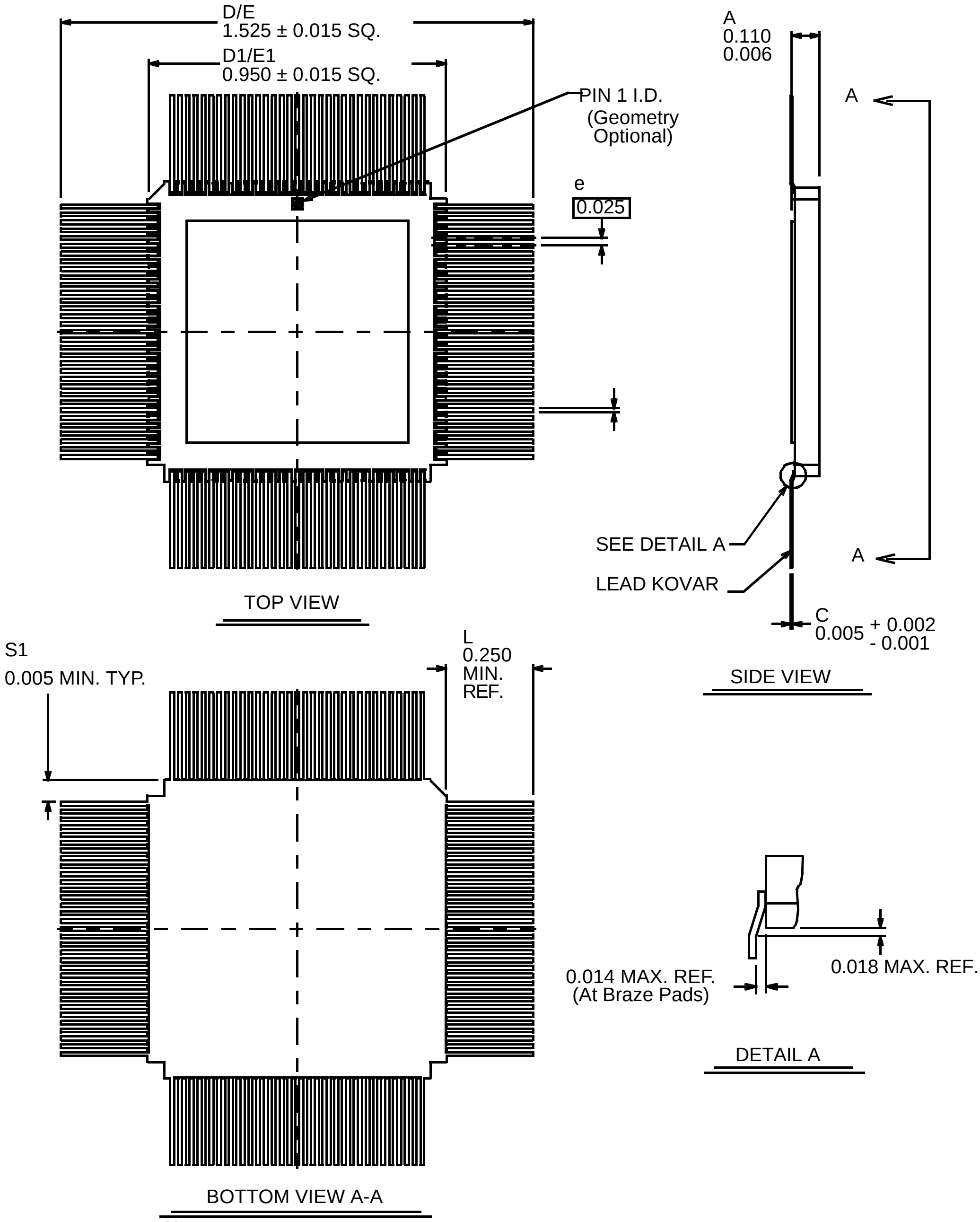
1. 84LCC package is not available radiation-hardened.



Notes:

1. True position applies to pins at base plane (datum C).
2. True position applies at pin tips.
3. All package finishes are per MIL-M-38510.
4. Letter designations are for cross-reference to MIL-M-38510.

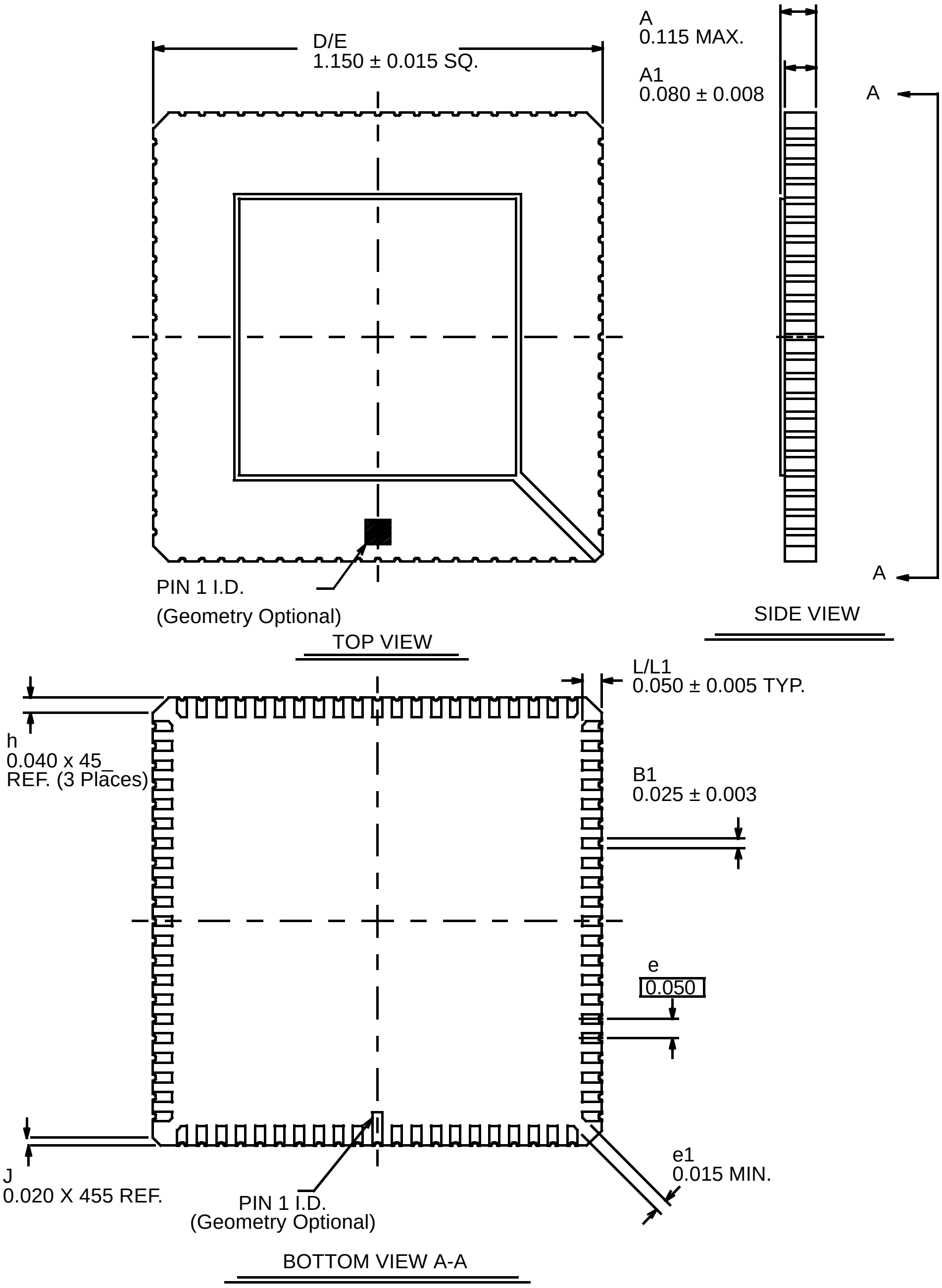
144-Pin Pingrid Array



Notes:

1. All package finishes are per MIL-M-38510.
2. Letter designations are for cross-reference to MIL-M-38510.

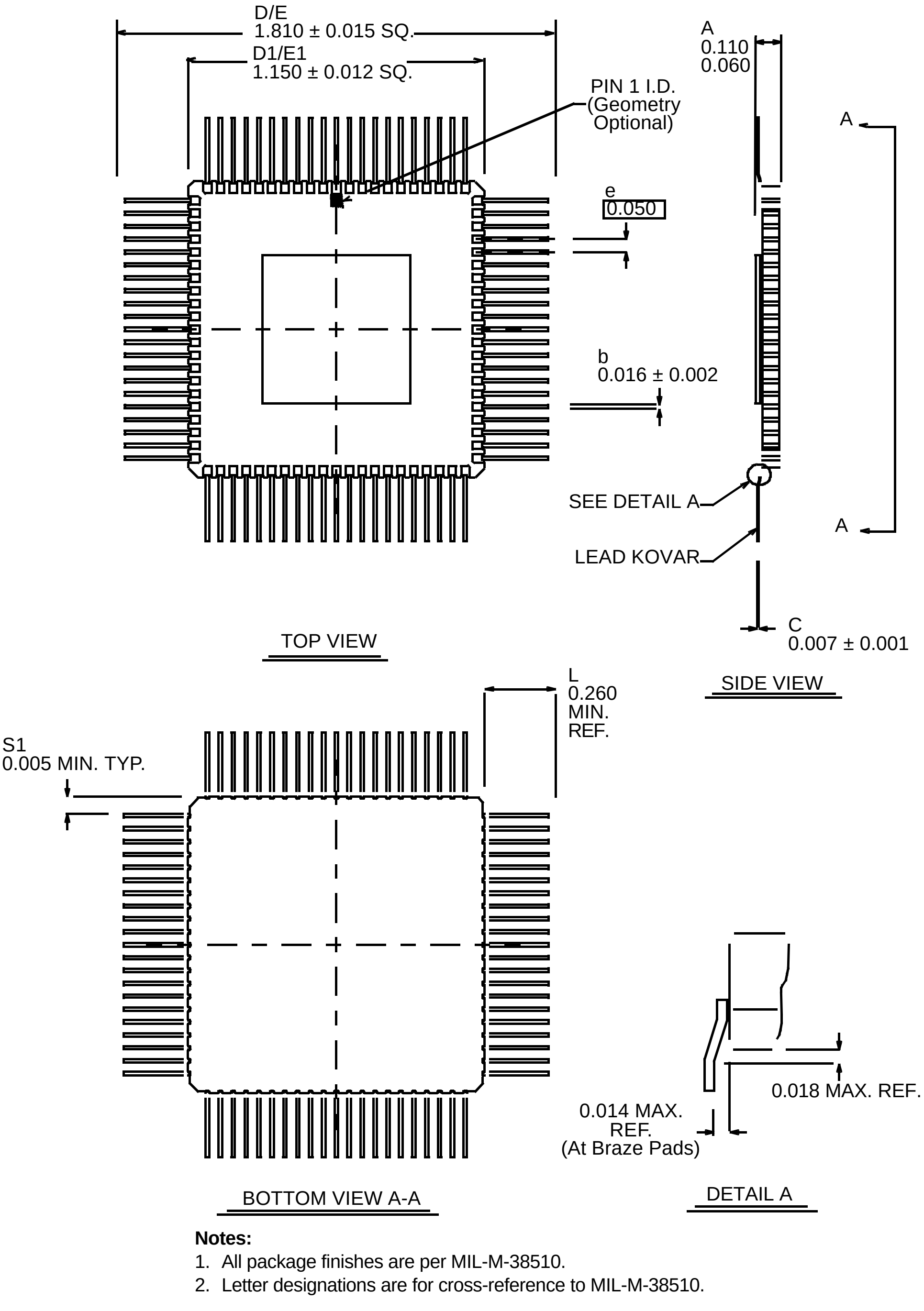
132-Lead Flatpack (25-MIL Lead Spacing)



Notes:

1. All package finishes are per MIL-M-38510.
2. Letter designations are for cross-reference to MIL-M-38510.

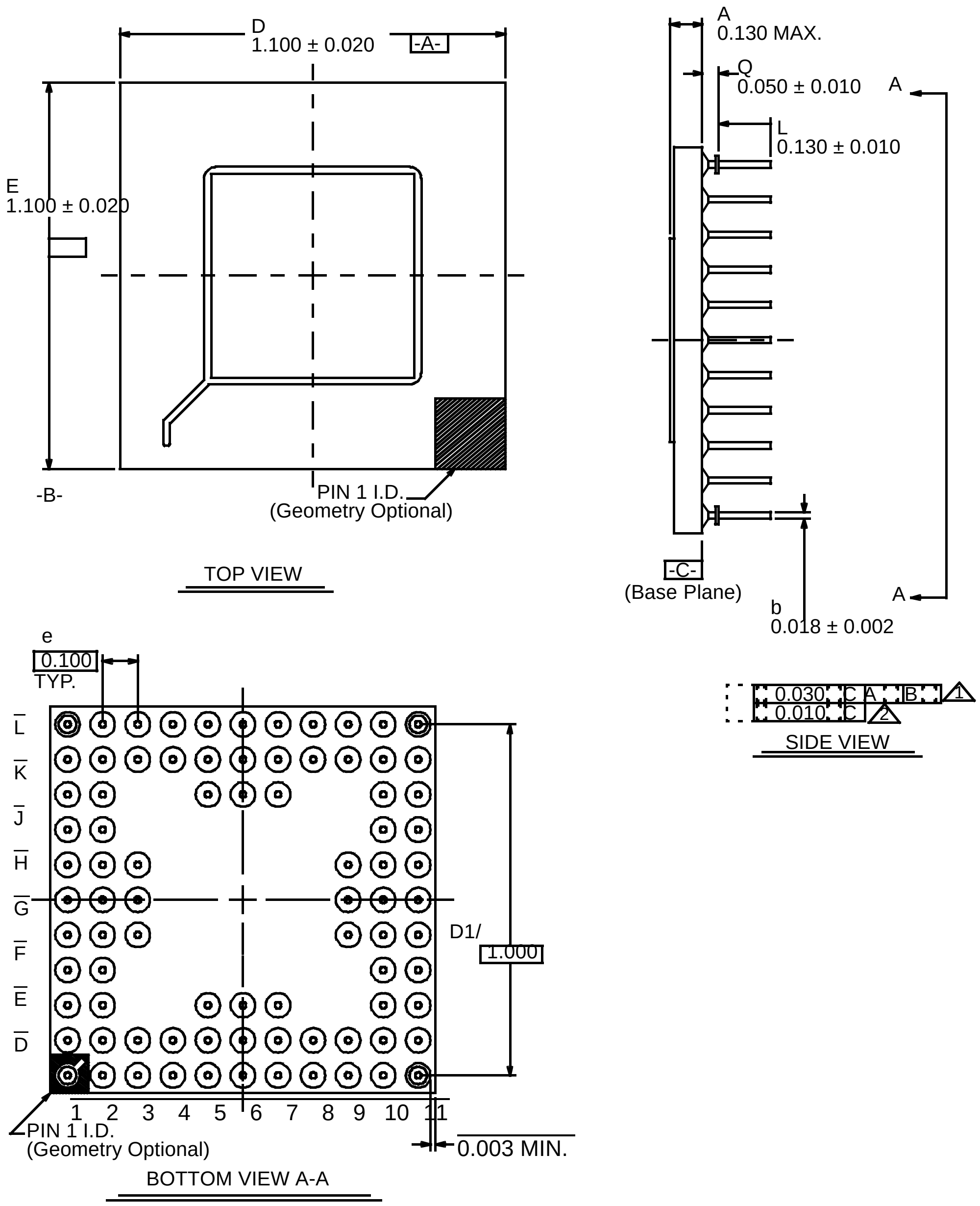
84-LCC



Notes:

1. All package finishes are per MIL-M-38510.
2. Letter designations are for cross-reference to MIL-M-38510.

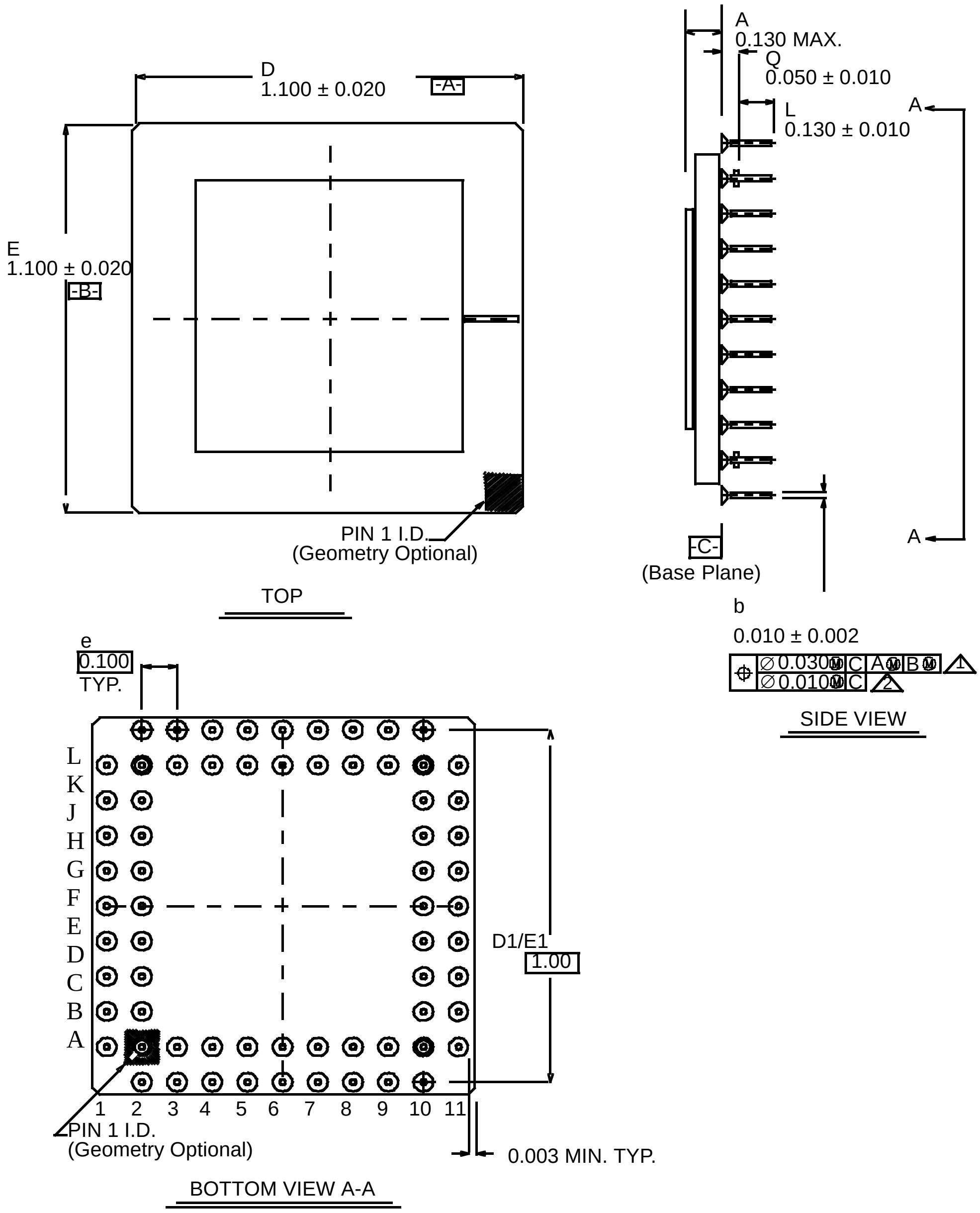
84-Lead Flatpack (50-MIL Lead Spacing)



Notes:

1. True position applies to pins at base plane (datum C).
2. True position applies at pin tips.
3. All packages finishes are per MIL-M-38510.
4. Letter designations are for cross-reference to MIL-M-38510.

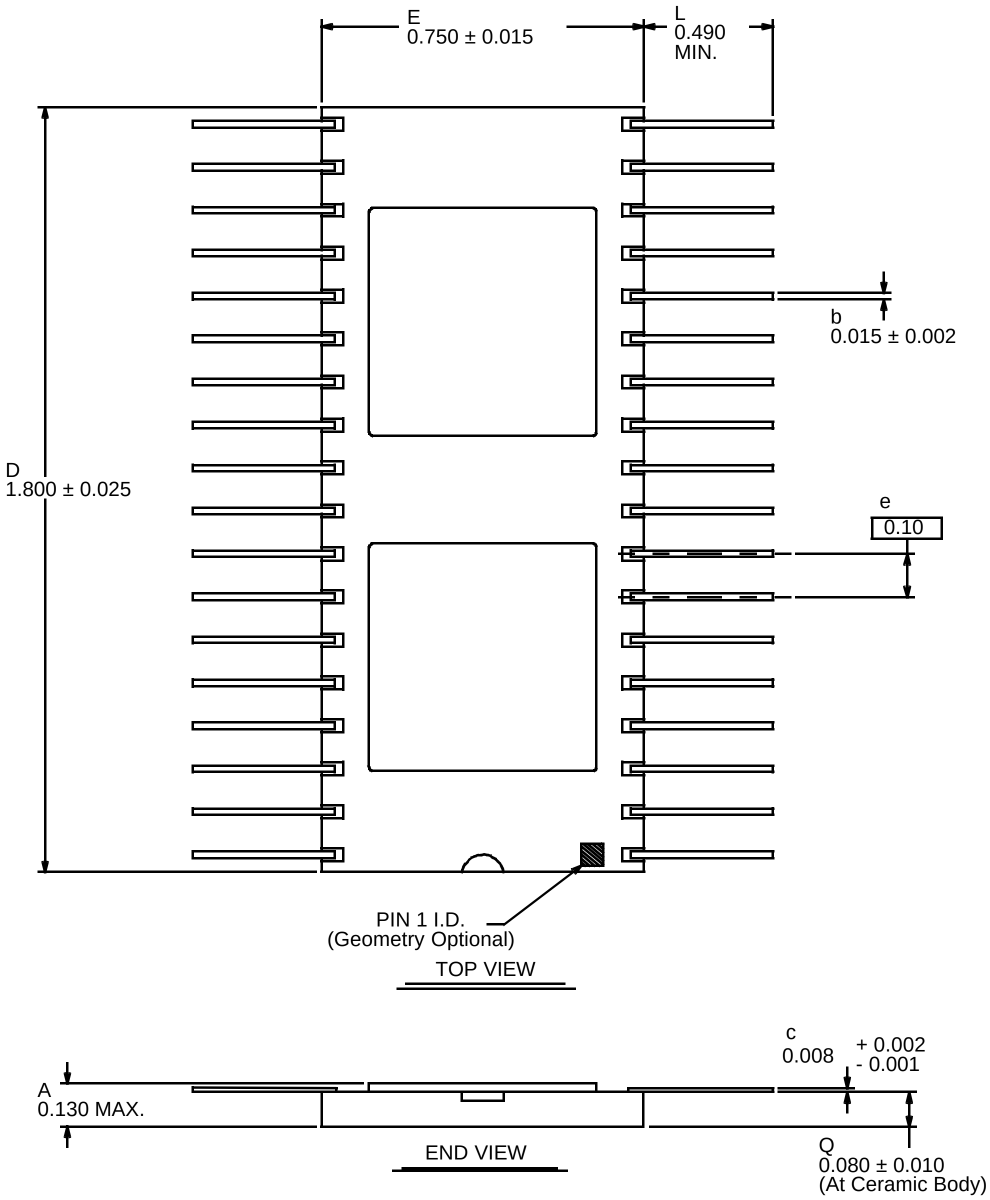
84-Pin Pingrid Array



Notes:

1. True position applies to pins at base plane (datum C).
2. True position applies at pin tips.
3. All packages finishes are per MIL-M-38510.
4. Letter designations are for cross-reference to MIL-M-38510.

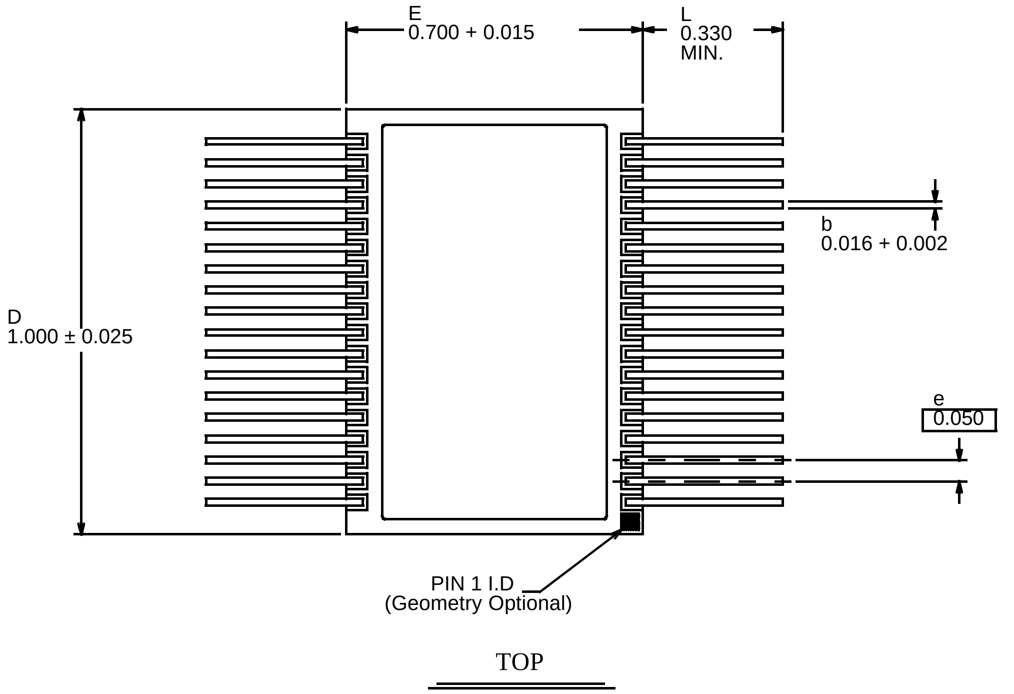
68-Pin Pingrid Array

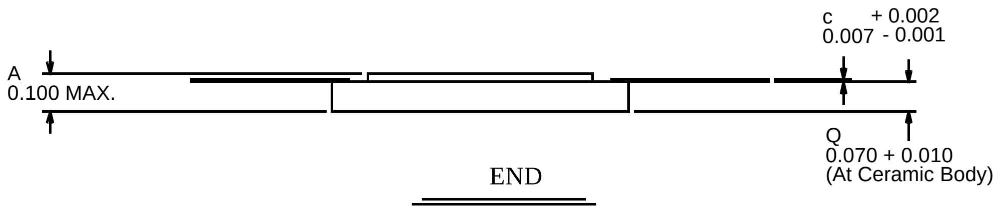


Notes:

1 All package finishes are per MIL-M-38510.
2. It is recommended that package ceramic be mounted to a heat removal rail located on the printed circuit board. A thermally conductive material such as MERECO XLN-589 or equivalent should be used.
3. Letter designations are for cross-reference to MIL-M-38510.

36-Lead Flatpack, Dual Cavity (100-MIL Lead Spacing)

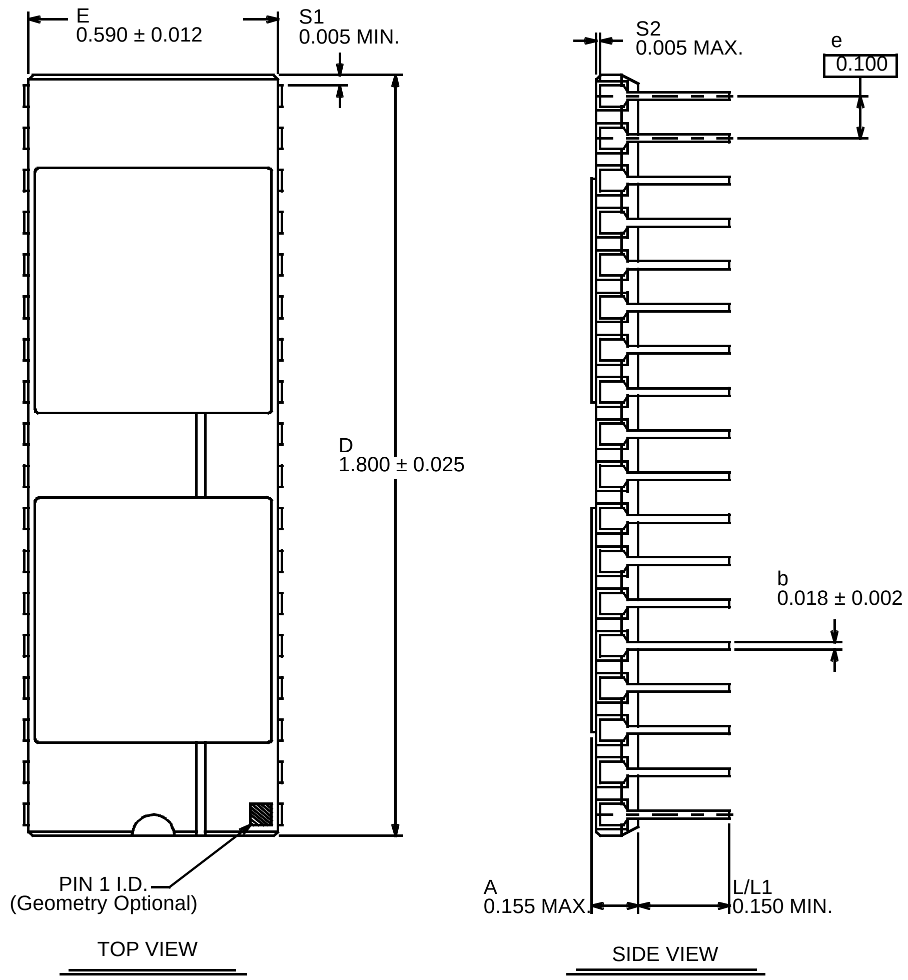


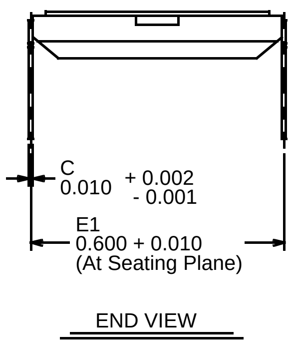


Notes:

1. All package finishes are per MIL-M-38510.
2. It is recommended that package ceramic be mounted to a heat removal rail located on the printed circuit board. A thermally conductive material such as MERECO XLN-589 or equivalent should be used.
3. Letter designations are for cross-reference to MIL-M-38510.

36-Lead Flatpack, Dual Cavity (50-MIL Lead Spacing)

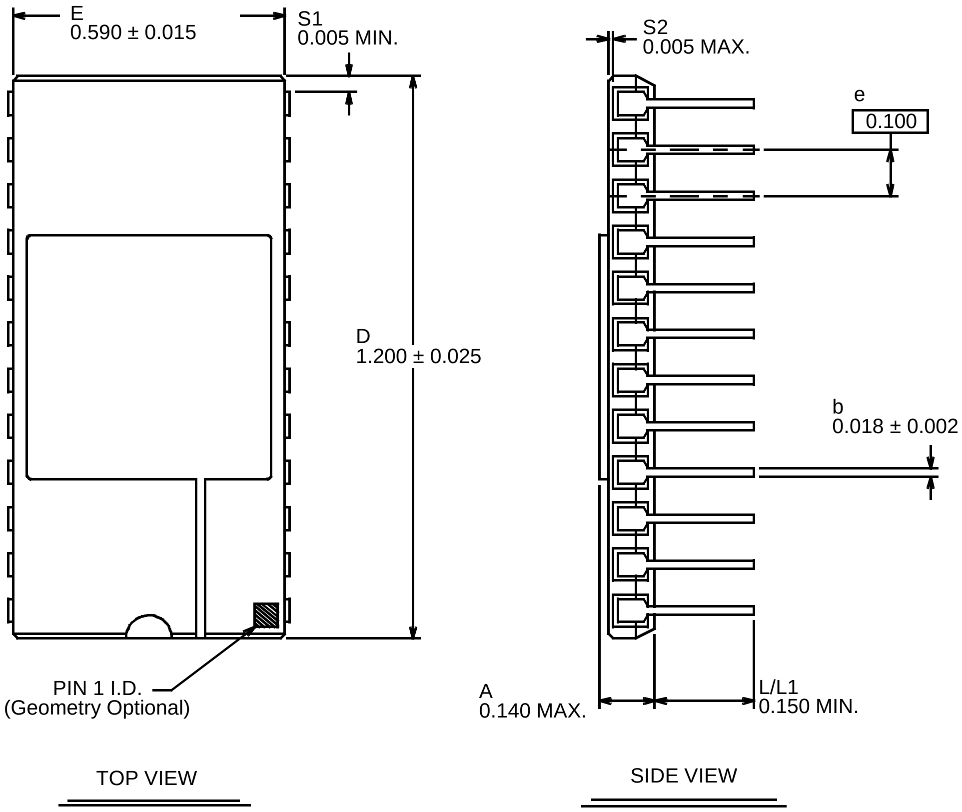


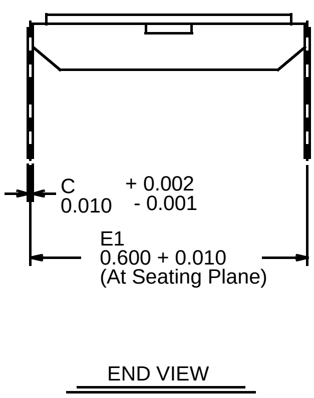


Notes:

1. All package finishes are per MIL-M-38510.
2. It is recommended that package ceramic be mounted to a heat removal rail located on the printed circuit board. A thermally conductive material such as MERECO XLN-589 or equivalent should be used.
3. Letter designations are for cross-reference to MIL-M-38510.

36-Lead Side-Brazed DIP, Dual Cavity





Notes:

1. All package finishes are per MIL-M-38510.
2. It is recommended that package ceramic be mounted to a heat removal rail located on the printed circuit board. A thermally conductive material such as MERECO XLN-589 or equivalent should be used.
3. Letter designations are for cross-reference to MIL-M-38510.

24-Lead Side-Brazed DIP, Single Cavity

ORDERING INFORMATION

UT1553B RTS Remote Terminal for Stores: S

5962 - * * * * *

- Lead Finish:
  - (A) = Solder
  - (C) = Gold
  - (X) = Optional
- Case Outline:
  - (X) = 68 pin PGA
- Class Designator:
  - (-) = Blank or No field is QML Q
- Drawing Number: 8957501
- Total Dose:
  - (-) = None
- Federal Stock Class Designator: No options

Notes:

1. Lead finish (A, C, or X) must be specified.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. For QML Q product, the Q designator is intentionally left blank in the SMD number (e.g. 5962-8957501XC).

UT1553B RTS Remote Terminal for Stores

No UT Part Number- * *

Lead Finish:
(A) = Solder
(C) = Gold
(X) = Optional

Package Type:
(G) = 68 pin PGA

UTMC Core Part Number

Notes:
1. Lead finish (A, C, or X) must be specified.
2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).