

# UT0.25 $\mu$ CRH Commercial RadHard™ Structured Array

Preliminary Data Sheet



April 2003

## FEATURES

- ❑ Up to 3,000,000 usable equivalent gates using structured array architecture
- ❑ Toggle rates up to 1.6 GHz
- ❑ Advanced 0.25 $\mu$  silicon gate CMOS processed in a commercial fab
- ❑ Operating voltage of 3.3V and 2.5V
- ❑ I/O buffers are 5-volt compliant
- ❑ Multiple product assurance levels available, QML Q and V, military, industrial
- ❑ Radiation hardened from 100Krad(Si) to 1 Megarad total dose available using Aeroflex UTMC's RadHard techniques
- ❑ SEU-immune to less than 1.0E-10 errors/bits-day available using special library cells
- ❑ Robust Aeroflex UTMC Design Library of cells and macros
- ❑ Design support for Mentor Graphics®, Synopsys™, in Verilog and VHDL design languages on Sun and Linux workstations
- ❑ Full complement of industry standard IP cores
- ❑ Configurable RAM compilers
- ❑ Supports cold sparing for power down applications
- ❑ Power dissipation of 0.04 $\mu$ W/MHz/gate at  $V_{DDCORE}$  2.5V and 20% duty cycle

## PRODUCT DESCRIPTION

The high-performance UT0.25 $\mu$  Commercial RadHard™ ASIC structured array family features densities up to 3,000,000 equivalent gates and is available in multiple quality assurance levels such as MIL-PRF-38535, QML Q and V, military and industrial grades and non-RadHard versions.

For those designs requiring stringent radiation hardness, Aeroflex UTMC's 0.25 $\mu$  deep sub-micron process employs a special technique that enhances the total dose radiation hardness from 100Krad(Si) to 1 Megarad while maintaining circuit density and reliability. In addition, for both greater transient radiation hardness and latch-up immunity, the deep submicron process is built on epitaxial wafers.

Developed from Aeroflex UTMC's patented architectures, the deep submicron ASIC family uses a highly efficient structured array architecture for the internal cell instantiation. Combined with state-of-the-art placement and routing tools, the area utilization and signal interconnect of transistors is maximized using five levels of metal interconnect.

The UT0.25 $\mu$ CRH ASIC family is supported by an extensive cell library that includes SSI, MSI, and 54XX equivalent functions, as well as configurable RAM and cores. Aeroflex UTMC's core library includes the following functions:

- Intel 80C31® equivalent
- Intel 80C196® equivalent
- MIL-STD-1553 functions (BRCTM, RTI, RTMP)
- MIL-STD-1750 microprocessor
- RISC microcontroller
- Configurable RAM

**Table 1. Gate Densities**

<b>DIE SIZE (Mils estimate)</b>	<b>EQUIVALENT USABLE GATES<sup>1</sup></b>	<b>SIGNAL I/O<sup>2</sup></b>	<b>POWER &amp; GROUND PADS</b>
245	276,890	160	48
313	501,760	216	64
374	757,350	265	79
426	1,024,000	308	92
510	1,524,122	376	112
578	2,007,040	431	129
642	2,524,058	484	144
699	3,029,402	530	158

**Notes:**

1. Based on NAND2 equivalents plus 20% routing overhead. Actual usable gate count is design-dependent.
2. Includes five pins that may or may not be reserved for JTAG boundary-scan, depending on user requirements.

**Low-noise Device and Package Solutions**

Separate on-chip power and ground buses are provided for internal cells and output drivers which further isolate internal design circuitry from switching noise.

In addition, Aeroflex UTMC offers advanced low-noise package technology with multi-layer, co-fired ceramic construction featuring built-in isolated power and ground planes (see Table 2). These planes provide lower overall resistance/inductance through power and ground paths which minimize voltage drops during periods of heavy switching. These isolated planes also

help sustain supply voltage during dose rate events, thus preventing rail span collapse.

Flatpacks are available with up to 352 leads; PGAs are available with up to 299 pins and LGAs to 472 pins. Aeroflex UTMC's flatpacks feature a non-conductive tie bar that helps maintain lead integrity through test and handling operations. In addition to the packages listed in Table 2, Aeroflex UTMC offers custom package development and package tooling modification services for individual requirements.

**Table 2. Packages**

<b>Type</b>	<b>Package</b>
Flatpack	68, 84, 132, 172, 196, 256, 304, 340, 352
PGA	281, 299
LGA	472

**Notes:**

1. The number of device I/O pads available may be restricted by the selected package.
2. PGA packages have one additional non-connected index pin (i.e., 84 + 1 index pin = 85 total package pins for the 85 PGA). Contact Aeroflex UTMC for specific package drawings.

### Extensive Cell Library

The UT0.25 $\mu$ CRH family of gate arrays is supported by an extensive cell library that includes SSI, MSI, and 54XX-equivalent functions, as well as RAM and other library functions. User-selectable options for cell configurations include scan for all register elements, as well as output drive strength. Aeroflex UTMC's core library includes the following functions:

- Intel® 80C31 equivalent
- Intel® 80C196 equivalent
- MIL-STD-1553 functions (BCRTM, RTI, RTMP)
- MIL-STD-1750 microprocessor
- Standard microprocessor peripheral functions
- Configurable RAM (SRAM, DPsRAM)
- RISC Microcontroller
- USART (82C51)
- EDAC

Refer to Aeroflex UTMC's UT0.25 $\mu$ CRH Design Manual for complete cell listing and details.

### I/O Buffers

The UT0.25 $\mu$ CRH gate array family offers up to 530 signal I/O locations (note: device signal I/O availability is affected by package selection and pinout.) The I/O cells can be configured by the user to serve as input, output, bidirectional, three-state, or additional power and ground pads. Output drive options range from 2 to 12mA. To drive larger off-chip loads, output drivers may be combined in parallel to provide additional drive up to 24mA.

Other I/O buffer features and options include:

- Pull-up and pull-down resistors
- Schmitt trigger
- LVDS
- PCI
- Cold Sparing

### JTAG Boundary-Scan

The UT0.25 $\mu$ CRH arrays provide for a test access port and boundary-scan that conforms to the IEEE Standard 1149.1 (JTAG). Some of the benefits of this capability are:

- Easy test of complex assembled printed circuit boards
- Gain access to and control of internal scan paths
- Initiation of Built-In Self Test

### Clock Driver Distribution

Aeroflex UTMC design tools provide methods for balanced clock distribution that maximize drive capability and minimize relative clock skew between clocked devices.

### Speed and Performance

Aeroflex UTMC specializes in high-performance circuits designed to operate in harsh military and radiation environments. Table 3 presents a sampling of typical cell delays.

Note that the propagation delay for a CMOS device is a function of its fanout loading, input slew, supply voltage, operating temperature, and processing radiation tolerance. In a radiation environment, additional performance variances must be considered. The UT0.25 $\mu$ CRH array family simulation models account for all of these effects to accurately determine circuit performance for its particular set of use conditions.

### Power Dissipation

Each internal gate or I/O driver has an average power consumption based on its switching frequency and capacitive loading. Radiation-tolerant processes exhibit power dissipation that is typical of CMOS processes. For a rigorous power estimating methodology, refer to the Aeroflex UTMC UT0.25 $\mu$ CRH Design Manual or consult with a Aeroflex UTMC Applications Engineer.

### Typical Power Dissipation

0.04 $\mu$ W/Gate-MHz@2.5V	20% duty cycle
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**Table 3. Typical Cell Delays**

<b>CELL</b>	<b>OUTPUT TRANSITION</b>	<b>PROPAGATION DELAY <sup>1</sup></b>
<b>Internal Gates</b>		<b>V<sub>DD</sub> = 2.5V</b>
INV1, Inverter	HL	.068
	LH	.090
INV4, Inverter 4X	HL	.035
	LH	.050
NAND2, 2-Input NAND	HL	.102
	LH	.103
NOR2, 2-Input NOR	HL	.080
	LH	.148
DFF - CLK to Q	HL	.391
	LH	.394
LDL - CLK to Q	HL	.474
	LH	.352
<b>Output Buffers</b>		
OC3325N4_C, CMOS	HL	4.599
	LH	6.578
OC3325N12_C, CMOS	HL	3.060
	LH	3.758
<b>Input Buffers</b>		
IC3325_C, CMOS	HL	.468
	LH	.313

**Note:**

1. All specifications in ns (typical). Output load capacitance is 50pF. Fanout loading for input buffers and gates is the equivalent of two gate input loads.

**ASIC DESIGN SOFTWARE**

Using a combination of state-of-the-art third-party and proprietary design tools, Aeroflex UTMC delivers the CAE support and capability to handle complex, high-performance ASIC designs from design concept through design verification and test.

Aeroflex UTMC’s flexible circuit creation methodology supports high level design by providing UT0.25µCRH libraries for Mentor Graphics and Synopsys synthesis tools. Design verification is performed in any VHDL or Verilog simulator or the Mentor Graphics environment, using Aeroflex UTMC’s robust libraries. Aeroflex UTMC also supports Automatic Test Program Generation to improve design testing.

**Aeroflex UTMC HDL DESIGN SYSTEMS**

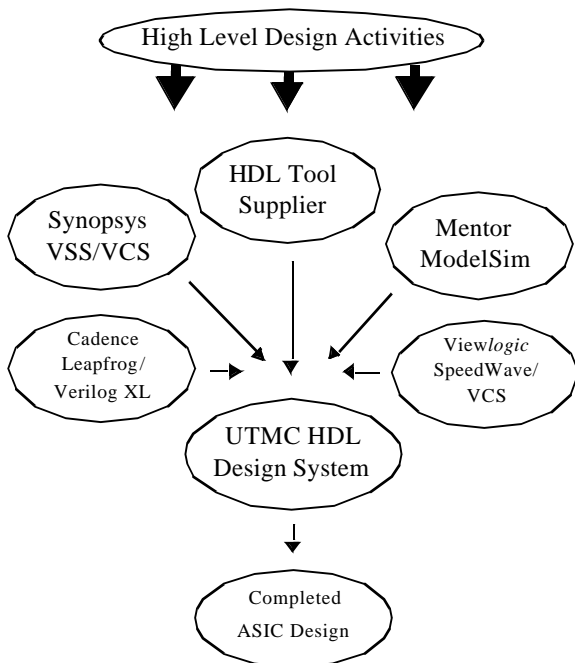
Aeroflex UTMC offers a Hardware Description Language (HDL) design system supporting VHDL and Verilog. Both the VHDL and Verilog libraries provide sign-off quality models and robust tools.

The VHDL libraries are VITAL 3.0 compliant, and the Verilog libraries are OVI 1.0 compliant. With the library capabilities Aeroflex UTMC provides, you can use High Level Design methods to synthesize your design for simulation. Aeroflex UTMC also provides tools to verify that your HDL design will result in working ASIC devices.

Either of Aeroflex UTMC’s HDL design system lets you easily access Aeroflex UTMC’s RadHard capabilities.

**ADVANTAGES OF THE AEROFLEX UTMC HDL DESIGN SYSTEMS**

- The Aeroflex UTMC HDL Design System gives you the freedom to use tools from Synopsys, Mentor Graphics, Cadence, Viewlogic, and other vendors to help you synthesize and verify a design.
- Aeroflex UTMC’s Logic Rules Checker and Tester Rules Checker allow you to verify partial or complete designs for compliance with Aeroflex UTMC design rules.
- Aeroflex UTMC HDL Design System accepts back-annotation of timing information through SDF.
- Your design stays entirely within the language in which you started (VHDL or Verilog) preventing conversion headaches.



Aeroflex UTMC HDL Design Flow

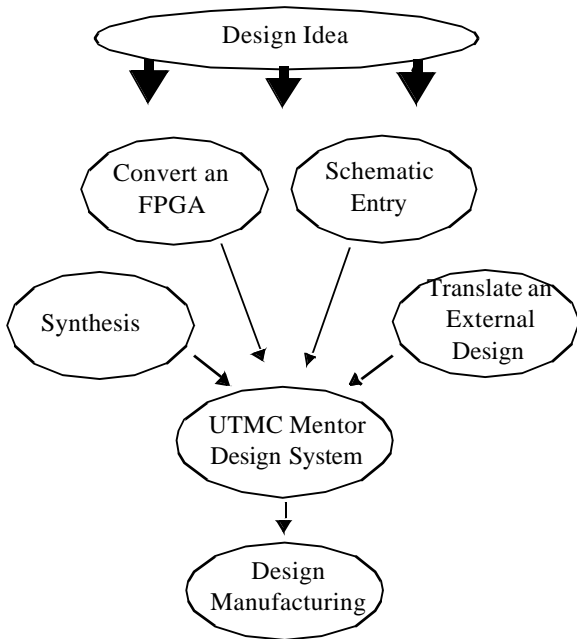
**XDT<sup>sm</sup> (eXternal Design Translation)**

Through Aeroflex UTMC’s XDT services, customers can convert an existing non-Aeroflex UTMC design to Aeroflex UTMC’s processes. The XDT tool is particularly useful for converting an FPGA to an Aeroflex UTMC radiation-tolerant gate array. The XDT translation tools convert industry standard netlist formats and vendor libraries to Aeroflex UTMC formats and libraries. Industry standard netlist formats supported by Aeroflex UTMC include:

- VHDL
- Verilog HDL™
- FPGA source files (Actel, Altera, Xilinx)
- EDIF
- Third-party netlists supported by Synopsys

## AEROFLEX UTMC MENTOR GRAPHICS DESIGN SYSTEM

The Aeroflex UTMC Mentor Graphics Design System software is fully integrated into the Mentor Graphics design environment, making it familiar and easy to use. Aeroflex UTMC tools support Mentor functions such as cross-highlighting, graphical menus, and design navigation.



Aeroflex UTMC Mentor Graphics Design

After creating a design in the Mentor Graphics environment, you can easily verify the design for electrical rules compliance with the Aeroflex UTMC Logic Rules Checker. Testability can be verified with the Aeroflex UTMC Tester Rules Checker. Both of these tools are fully integrated into the Mentor Graphics Environment.

When you have completed all design activities, Aeroflex UTMC's Design Transfer tool captures all the required files and prepares them for easy transfer to Aeroflex UTMC. Aeroflex UTMC uses this data to convert your design into a packaged and tested device.

## ADVANTAGES OF THE AEROFLEX UTMC MENTOR DESIGN SYSTEM

- Aeroflex UTMC customers have successfully used the Aeroflex UTMC Mentor Graphics Design System for over a decade.
- Aeroflex UTMC's Logic and Tester Rules Checker tools allow you to verify partial or complete designs for compliance with Aeroflex UTMC manufacturing practices and procedures.
- The Design System accepts pre-and post-layout timing information to ensure your design results in devices that meet your specifications.
- The Design System supports Leonardo, and database transfer between Synopsys and Mentor.
- The Design System supports powerful Mentor Graphics ATPG capabilities.

## TOOLS SUPPORTED BY AEROFLEX UTMC

Aeroflex UTMC supports libraries for:

- Mentor Graphics
  - ModelSim
- Synopsys
  - Design Compiler
  - PrimeTime
  - Formality
  - TetraMax
- VITAL-compliant VHDL Tools
- OVI-compliant Verilog Tools

## TRAINING AND SUPPORT

Aeroflex UTMC personnel conduct training classes tailored to meet individual needs. These classes can address a wide mix of engineering backgrounds and specific customer concerns. Applications assistance is also available through all phases of ASIC Design.

**PHYSICAL DESIGN**

Using five layers of metal interconnect, Aeroflex UTMC achieves optimized layouts that maximize speed of critical nets, overall chip performance, and design density up to 3,000,000 equivalent gates.

**Test Capability**

Aeroflex UTMC supports all phases of test development from test stimulus generation through high-speed production test. This support includes ATPG, fault simulation, and fault grading. Scan design options are available on all UT0.25μCRH storage elements. Automatic test program development capabilities handle large vector sets for use with Aeroflex UTMC’s LTX/Trillium MicroMasters, supporting high-speed testing (up to 80MHz with pin multiplexing).

**Unparalleled Quality and Reliability**

Aeroflex UTMC is dedicated to meeting the stringent performance requirements of aerospace and defense systems suppliers. AeroflexUTMC maintains the highest level of quality and reliability through our Quality Management Program under MIL-PRF-38535 and ISO-9001. In 1988, we were the first gate array manufacturer to achieve QPL certification and qualification of our technology families. Our product assurance program has kept pace with the demands of certification and qualification.

Our quality management plan includes the following activities and initiatives.

- Quality improvement plan
- Failure analysis program
- SPC plan
- Corrective action plan
- Change control program
- Standard Evaluation Circuit (SEC) and Technology Characterization Vehicle (TCV) assessment program
- Certification and qualification program

Because of numerous product variations permitted with customer specific designs, much of the reliability testing is performed using a Standard Evaluation Circuit (SEC) and Technology Characterization Vehicle (TCV). Aeroflex UTMC utilizes the

wafer foundry’s data from TCV test structures to evaluate hot carrier aging, electromigration, and time dependent test samples for reliability testing. Data from the wafer-level testing can provide rapid feedback to the fabrication process, as well as establish the reliability performance of the product before it is packaged and shipped.

**Radiation Tolerance**

Aeroflex UTMC incorporates radiation-tolerance techniques in process design, design rules, array design, power distribution, and library element design. All key radiation-tolerance process parameters are controlled and monitored using statistical methods and in-line testing.

PARAMETER	RADIATION TOLERANCE	NOTES
Total dose	1.0E5 rad(SiO <sub>2</sub> )	1
	3.0E5 rad(SiO <sub>2</sub> )	2
Dose rate upset	1.0E8 rad(Si)/sec	3
Dose rate survivability	1.0E11 rad(Si)/sec	4
SEU	<2.0E-10 errors per cell-day	4, 5
Projected neutron fluence	1.0E14 n/sq cm	
Latchup	Latchup-immune over specified use conditions	

**Notes:**

1. Total dose Co-60 testing is in accordance with MIL-STD-883, Method 1019. Data sheet electrical characteristics guaranteed to 1.0E5 rads(SiO<sub>2</sub>). All post-radiation values measured at 25°C.
2. Total dose Co-60 testing is in accordance with MIL-STD-883, Method 1019 at dose rates >1 rad(SiO<sub>2</sub>)/s.
3. Short pulse 20ns FWHM (full width, half maximum).
4. Is design dependent; SEU limit based on standard evaluation circuit at 4.5V worst case condition.
5. SEU-hard flip-flop cell. Non-hard flip-flop typical is 4E-8.

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(Referenced to  $V_{SS}$ )

SYMBOL	PARAMETER	LIMITS
$V_{DD}^{2/}$	I/O DC Supply Voltage	-0.3V to 4.0V
$V_{DDCORE}^{2/}$	Core DC Supply Voltage	0.3 to 2.8V
$V_{DD} - V_{DDCORE}$	Max Voltage Difference	4.3V
$V_{DDCORE} - V_{DD}$	Max Voltage Difference	3.1V
$T_{STG}$	Storage temperature	-65 to +150°C
$T_J$	Maximum junction temperature	+175°C
$I_{LU}$	Latchup immunity	$\pm 150$ mA
$I_I$	DC input current	$\pm 10$ mA
$T_{LS}$	Lead temperature (solder 5 sec)	+300°C

**Note:**

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The recommended "power-on" sequence is  $V_{DDCORE}$  voltage supply applied first, followed by the  $V_{DD}$  voltage supply. The recommended "power-off" sequence is the reverse. Remove  $V_{DD}$  voltage supply, followed by removing  $V_{DDCORE}$  voltage supply.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
$V_{DD}$	I/O DC Supply Voltage	$3.3 \pm 0.3$ V
$V_{DDCORE}$	Core DC Supply Voltage	$2.5 \pm 0.25$ V

**Note:**

3.  $V_{DD}$  must be maintained at a voltage greater than  $V_{DDCORE}$  by 0.25V.



### DC ELECTRICAL CHARACTERISTICS

( $V_{DD} = 3.3V \pm 0.3$ ;  $V_{DDCORE} = 2.5V \pm 0.25$ ;  $-55^{\circ}C < T_C < +125^{\circ}C$ )

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
$V_{IL}$	Low-level input voltage <sup>1</sup> CMOS, OSC inputs	$-55^{\circ}C \leq T_C \leq +125^{\circ}C$ $V_{DD} = 3.3V \pm 0.3V$ $V_{DDCORE} = 2.5V \pm 0.25V$			$0.3V_{DD}$	V
$V_{IH}$	High-level input voltage <sup>1</sup> CMOS inputs	$-55^{\circ}C \leq T_C \leq +125^{\circ}C$ $V_{DD} = 3.3V \pm 0.3$ $V_{DDCORE} = 2.5V \pm 0.25$	$0.7V_{DD}$			V
$V_{T+}$	Schmitt Trigger, positive going threshold <sup>1</sup>	$-55^{\circ}C \leq T_C \leq +125^{\circ}C$ $V_{DD} = 3.3V \pm 0.3$ $V_{DDCORE} = 2.5V \pm 0.25$			$0.7V_{DD}$	V
$V_{T-}$	Schmitt Trigger, negative going threshold <sup>1</sup>	$-55^{\circ}C \leq T_C \leq +125^{\circ}C$ $V_{DD} = 3.3V \pm 0.3$ $V_{DDCORE} = 2.5V \pm 0.25$	$0.3V_{DD}$			V
$V_H$	Schmitt Trigger, typical range of hysteresis <sup>2</sup>		0.6			V
$I_{IN}$	Input leakage current CMOS and Schmitt inputs Inputs with pull-down resistors Inputs with pull-down resistors Inputs with pull-up resistors Inputs with pull-up resistors Cold Spare Inputs - Off  Cold Spare Inputs - On	$V_{IN} = V_{DD}$ or $V_{SS}$ $V_{IN} = V_{DD}$ $V_{IN} = V_{SS}$ $V_{IN} = V_{SS}$ $V_{IN} = V_{DD}$ $V_{IN} = V_{DD}$ $V_{IN} = 0$ to $3.6V$  $V_{IN} = V_{DD}$ or $V_{SS}$	-1 20 -5 -225 -5 -5		1 225 5 20 5 5	$\mu A$

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
$V_{OL}$	Low-level output voltage <sup>3</sup> CMOS/TTL 4.0mA buffer CMOS/TTL 8.0mA buffer CMOS/TTL 12.0mA buffer CMOS outputs (optional) CMOS outputs (optional)	$I_{OL} = 4.0\text{mA}$ $I_{OL} = 8.0\text{mA}$ $I_{OL} = 12.0\text{mA}$ $I_{OL} = 1.0\text{mA}$ $I_{OL} = 100.0\mu\text{A}$			0.4 0.4 0.4 0.05 0.05	V
$V_{OH}$	High-level output voltage <sup>3</sup> CMOS/TTL 4.0mA buffer CMOS/TTL 8.0mA buffer CMOS/TTL 12.0mA buffer CMOS outputs (optional) CMOS outputs (cold spare)	$I_{OH} = -3.0\text{mA}$ $I_{OH} = -5.0\text{mA}$ $I_{OH} = -7.0\text{mA}$ $I_{OH} = -1.0\text{mA}$ $I_{OH} = -100.0\mu\text{A}$	2.4 2.4 2.4 $V_{DD}-0.05$ $V_{DD}-0.10$			V
$I_{OZ}$	Three-state output leakage current CMOS  Cold Spare Inputs - Off Cold Spare Inputs - On	$V_O = V_{DD}$ and $V_{SS}$  $V_{IN} = 0\text{V}$ and $3.6\text{V}$ $V_{DD} = V_{SS} = 0$ $V_{DD} = V_{DD} = V_{SS}$	-5  -10 -10		5  10 +10	$\mu\text{A}$
$I_{OS}$	Short-circuit output current <sup>2,4</sup> CMOS	$V_O = V_{DD}$ and $V_{SS}$	-50		50	mA
$C_{IN}$	Input capacitance <sup>5</sup>	$f = 1\text{MHz}$ @ $0\text{V}$	4		15	pF
$C_{OUT}$	Output capacitance <sup>5</sup> 4.0mA buffer 8.0mA buffer 12.0mA buffer	$f = 1\text{MHz}$ @ $0\text{V}$		15 15 18		pF
$C_{IO}$	Bidirect I/O capacitance <sup>5</sup> 4.0mA buffer 8.0mA buffer 12.0mA buffer	$f = 1\text{MHz}$ @ $0\text{V}$		15 18 25		pF

I <sub>DDQ</sub>	Quiescent Supply Current <sup>b</sup>	V <sub>DD</sub> = 3.6V				μA			
							Group A, subgroups 1,3	200K gates	50
								400K gates	100
								600K gates	150
								800K gates	200
								1000K gates	250
								1500K gates	375
								2000K gates	500
								2500K gates	625
								3000K gates	750
Group A, subgroup 2	V <sub>DD</sub> = 3.6V					mA			
							200K gates	1	
							400K gates	2	
							600K gates	3	
							800K gates	4	
							1000K gates	5	
							1500K gates	7.5	
							2000K gates	10	
							2500K gates	12.5	
							3000K gates	15	
Group A, subgroup 1 RHA Designator: M, D, P, L, R	V <sub>DD</sub> = 3.6V					mA			
							200K gates	4	
							400K gates	6	
							600K gates	8	
							800K gates	10	
							1000K gates	12	
							1500K gates	18	
							2000K gates	24	
							2500K gates	30	
							3000K gates	36	

**Notes:**

\* Contact Aeroflex UPMC prior to usage.

- Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: V<sub>IH</sub> = V<sub>IH</sub>(min) + 20%, - 0%; V<sub>IL</sub> = V<sub>IL</sub>(max) + 0%, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V<sub>IH</sub>(min) and V<sub>IL</sub>(max).
- Supplied as a design limit but not guaranteed or tested.
- Per MIL-PRF-38535, for current density ≤ 5.0E5 amps/cm<sup>2</sup>, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF\*MHz.
- Not more than one output may be shorted at a time for maximum duration of one second.
- Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V<sub>SS</sub> at frequency of 1MHz @0V and a signal amplitude of ≤50mV RMS.
- All inputs with internal pull-ups should be left floating. All other inputs should be tied high or low.

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