Semicustom Products

UT0.6µCRH/SRH Commercial RadHard™ and Strategic RadHard™ Gate Array Family

Data Sheet

May 2002

FEATURES

- Multiple gate array sizes up to 600,000 usable equivalent gates
- Toggle rates up to 150 MHz
- Advanced 0.6µ (0.5µL_{eff}) radiation-tolerant silicon gate CMOS processed in a commercial fab
- Operating voltage of 5V and/or 3.3V
- QML Class Q & V compliant
- Designed specifically for high reliability applications
- Commercial RadHard™ for radiation-tolerant to 300K rads to meet space requirements and SEU-immune to less than 2.0E-10 errors/bit-day
- Strategic RadHard™ for radiation environments to 1 Mega rads to meet space requirements and SEU-immune to less than 2.0E-10 errors/bit-day
- JTAG (IEEE 1149.1) boundary-scan supported
- Low noise package technology for high speed circuits
- Design support using Mentor Graphics® andSynopsys™ in VHDL or Verilog design languages on Sun® and Linux workstations
- Supports cold sparing for power down applications
- Supports voltage translation
  - 5V bus to 3.3V bus
  - 3.3V bus to 5V bus

PRODUCT DESCRIPTION

The high-performance UT0.6µCRH/SRH gate array family features densities up to 600,000 equivalent gates and is available in MIL-PRF-38535 QML Q and V product assurance levels and is radiation-tolerant.

The Commercial RadHard™ and Strategic RadHard™ silicon is fabricated at American Microsystems Incorporated (AMI) using a minimally invasive processing module, developed by UTMC, that enhances the total dose radiation hardness of the field and gate oxides while maintaining circuit density and reliability. In addition, for both greater transient radiation-hardness and latchup immunity, the UTMC 0.6µ process is built on epitaxial substrate wafers.

Developed using UTMC's patented architectures, the UT0.6µCRH/SRH gate array family uses a highly efficient continuous column transistor architecture for the internal cell construction. Combined with state-of-the-art placement and routing tools, the utilization of available transistors is maximized using three levels of metal interconnect.

The UT0.6µCRH/SRH family of gate arrays is supported by an extensive cell library that includes SSI, MSI, and 54XX equivalent functions, as well as configurable RAM and cores. UTMC's core library includes the following functions:

- Intel 80C31® equivalent
- Intel 80C196® equivalent
- MIL-STD-1553 functions (BRCTM, RTI, RTMP)
- MIL-STD-1750 microprocessor
- RISC microcontroller
- Configurable RAM (SRAM, DPSRAM)
- USART (82C51)
- EDAC

Table 1. Gate Densities

DEVICE PART NUMBERS	EQUIVALENT USABLE GATES[1]	SIGNAL I/O[2]	POWER & GROUND PADS[3]
UT06MRA010	10,000	58	6
UT06MRA025	25,000	192	48
UT06MRA050	50,000	192	48
UT06MRA075	75,000	308	76
UT06MRA100	100,000	308	76
UT06MRA150	150,000	308	76
UT06MRA200	200,000	432	96
UT06MRA250	250,000	432	96
UT06MRA300	300,000	432	96
UT06MRA350	350,000	432	96
UT06MRA400	400,000	544	144
UT06MRA450	450,000	544	144
UT06MRA500	500,000	544	144
UT06MRA550	550,000	544	144
UT06MRA600	600,000	544	144

Notes:
1.Based on NAND2 equivalents. Actual usable gate count is design-dependent. Estimates reflect a mix of functions including RAM.
2.Includes five pins that may or may not be reserved for JTAG boundary-scan, depending on user requirements.
3.Reserved for dedicated V_{DD}/V_{SS} and V_{DDQ}/V_{SSQ}.

Low-noise Device and Package Solutions

The UT0.6µCRH/SRH array family's output drivers feature programmable slew rate control for minimizing noise and switching transients. This feature allows the user to optimize edge characteristics to match system requirements. Separate on-chip power and ground buses are provided for internal cells and output drivers which further isolate internal design circuitry from switching noise.

In addition, Aeroflex UTMC offers advanced low-noise package technology with multi-layer, co-fired ceramic construction featuring built-in isolated power and ground planes (see Table 2). These planes provide lower overall resistance/inductance through power and ground paths which minimize voltage drops during periods of heavy switching. These isolated planes also help sustain supply voltage during dose rate events, thus preventing rail span collapse.

Flatpacks are available with up to 352 leads; PGAs are available with up to 299 pins and LGAs to 472 pins. Aeroflex UTMC's flatpacks feature a non-conductive tie bar that helps maintain lead integrity through test and handling operations. In addition to the packages listed in Table 2, Aeroflex UTMC offers custom package development and package tooling modification services for individual requirements.

Table 2. Packages

PACKAGE TYPE/ LEADCOUNT[1]	025	050	075	100	150	200	250	300	350	400	450	500	550	600
Flatpack														
68			X	X	X									
84	X	X												
132	X	X												
172	X	X				X	X	X						
196	X	X				X	X	X						
256						X	X	X	X	X	X	X	X	X
304						X	X	X	X	X	X	X	X	X
340						X	X	X	X	X	X	X	X	X
352										X	X	X	X	X
PGA[2]														
281						X	X	X	X					
299						X	X	X	X					
LGA														
472											X	X	X	X

Notes:
1. The number of device I/O pads available may be restricted by the selected package.
2. PGA packages have one additional non-connected index pin (i.e., 84 + 1 index pin = 85 total package pins for the 85 PGA). Contact Aeroflex UTMC for specific package drawings.

Extensive Cell Library

The UT0.6µCRH/SRH family of gate arrays is supported by an extensive cell library that includes SSI, MSI, and 54XX-equivalent functions, as well as RAM and other library functions. User-selectable options for cell configurations include scan for all register elements, as well as output drive strength. Aeroflex UTMC's core library includes the following functions:

- Intel® 80C31 equivalent
- Intel® 80C196 equivalent
- MIL-STD-1553 functions (BCRTM, RTI, RTMP)
- MIL-STD-1750 microprocessor
- Standard microprocessor peripheral functions
- Configurable RAM (SRAM, DPsRAM)
- RISC Microcontroller
- USART (82C51)
- EDAC

Refer to Aeroflex UTMC's UT0.6µCRH/SRH Design Manual for complete cell listing and details.

I/O Buffers

The UT0.6µCRH/SRH gate array family offers up to 544 signal I/O locations (note: device signal I/O availability is affected by package selection and pinout.) The I/O cells can be configured by the user to serve as input, output, bidirectional, three-state, or additional power and ground pads. Output drive options range from 2 to 12mA. To drive larger off-chip loads, output drivers may be combined in parallel to provide additional drive up to 24mA.

Other I/O buffer features and options include:

- Slew rate control
- Pull-up and pull-down resistors
- TTL, CMOS, and Schmitt levels
- Cold sparing
- Voltage translation
  - 5V bus to 3.3V bus
  - 3.3V bus to 5V bus

JTAG Boundary-Scan

The UT0.6µCRH/SRH arrays provide for a test access port and boundary-scan that conforms to the IEEE Standard 1149.1 (JTAG). Some of the benefits of this capability are:

- Easy test of complex assembled printed circuit boards
- Gain access to and control of internal scan paths
- Initiation of Built-In Self Test

Clock Driver Distribution

Aeroflex UTMC design tools provide methods for balanced clock distribution that maximize drive capability and minimize relative clock skew between clocked devices.

Speed and Performance

Aeroflex UTMC specializes in high-performance circuits designed to operate in harsh military and radiation environments. Table 3 presents a sampling of typical cell delays.

Note that the propagation delay for a CMOS device is a function of its fanout loading, input slew, supply voltage, operating temperature, and processing radiation tolerance. In a radiation environment, additional performance variances must be considered. The UT0.6µCRH/SRH array family simulation models account for all of these effects to accurately determine circuit performance for its particular set of use conditions.

Power Dissipation

Each internal gate or I/O driver has an average power consumption based on its switching frequency and capacitive loading. Radiation-tolerant processes exhibit power dissipation that is typical of CMOS processes. For a rigorous power estimating methodology, refer to the Aeroflex UTMC UT0.6µCRH/SRH Design Manual or consult with a Aeroflex UTMC Applications Engineer.

Typical Power Dissipation

1.1µW/Gate-MHz@5.0V	0.4µW/Gate-MHz@3.3V

Table 3. Typical Cell Delays

CELL	OUTPUT TRANSITION	PROPAGATION DELAY [1]	
Internal Gates		V_{DD} = 5.0V	V_{DD} = 3.3V
INV1, Inverter	HL	.15	.16
	LH	.23	.29
INV4, Inverter 4X	HL	.06	.07
	LH	.10	.16
NAND2, 2-Input NAND	HL	.19	.25
	LH	.22	.33
NOR2, 2-Input NOR	HL	.16	.22
	LH	.32	.45
DFF - CLK to Q	HL	.81	1.12
	LH	.76	1.06
	HL	.75	1.05
	LH	.61	.85
Output Buffers			
OC5050N4, CMOS	HL	3.85	2.15
	LH	4.66	3.76
OT5050N4, TTL, 4mA	HL	5.58	5.49
	LH	2.52	2.93
OT5050N12, TTL, 12mA	HL	2.42	
	LH	1.29	
Input Buffers			
IC5050, CMOS	HL	.81	1.07
	LH	1.16	1.18
IT5050, TTL	HL	1.39	1.12
	LH	1.16	1.30

Note:
1. All specifications in ns (typical). Output load capacitance is 50pF. Fanout loading for input buffers and gates is the equivalent of two gate input loads.

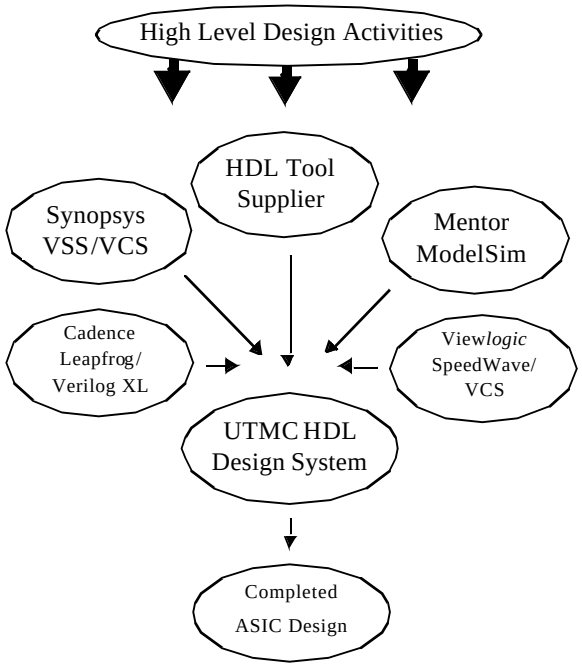
ASIC DESIGN SOFTWARE

Using a combination of state-of-the-art third-party and proprietary design tools, Aeroflex UTMC delivers the CAE support and capability to handle complex, high-performance ASIC designs from design concept through design verification and test.

Aeroflex UTMC's flexible circuit creation methodology supports high level design by providing UT0.6µCRH/SRH libraries for Mentor Graphics and Synopsys synthesis tools. Design verification is performed in any VHDL or Verilog simulator or the Mentor Graphics environment, using Aeroflex UTMC's robust libraries. Aeroflex UTMC also supports Automatic Test Program Generation to improve design testing.

Aeroflex UTMC HDL DESIGN SYSTEMS

Aeroflex UTMC offers a Hardware Description Language (HDL) design system supporting VHDL and Verilog. Both the VHDL and Verilog libraries provide sign-off quality models and robust tools.



Aeroflex UTMC HDL Design Flow

The VHDL libraries are VITAL 3.0 compliant, and the Verilog libraries are OVI 1.0 compliant.With the library capabilities Aeroflex UTMC provides, you can use High Level Design methods to synthesize your design for simulation. Aeroflex UTMC also provides tools to verify that your HDL design will result in working ASIC devices.

Either of Aeroflex UTMC's HDL design system lets you easily access Aeroflex UTMC's RadHard capabilities.

ADVANTAGES OF THE AEROFLEX UTMC HDL DESIGN SYSTEMS

- The Aeroflex UTMC HDL Design System gives you the freedom to use tools from Synopsys, Mentor Graphics, Cadence, View*logic*, and other vendors to help you synthesize and verify a design.
- Aeroflex UTMC's Logic Rules Checker and Tester Rules Checker allow you to verify partial or complete designs for compliance with Aeroflex UTMC design rules.
- Aeroflex UTMC HDL Design System accepts back-annotation of timing information through SDF.
- Your design stays entirely within the language in which you started (VHDL or Verilog) preventing conversion headaches.

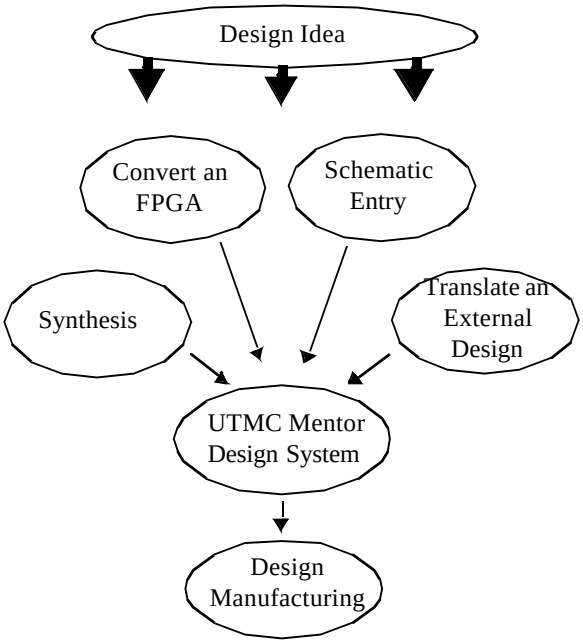
XDT^{sm} (eXternal Design Translation)

Through Aeroflex UTMC's XDT services, customers can convert an existing non-Aeroflex UTMC design to Aeroflex UTMC's processes. The XDT tool is particularly useful for converting an FPGA to a Aeroflex UTMC radiation-tolerant gate array. The XDT translation tools convert industry standard netlist formats and vendor libraries to Aeroflex UTMC formats and libraries. Industry standard netlist formats supported by Aeroflex UTMC include:

- VHDL
- Verilog HDL^{TM}
- FPGA source files (Actel, Altera, Xilinx)
- EDIF
- Third-party netlists supported by Synopsys

AEROFLEX UTMC MENTOR GRAPHICS DESIGN SYSTEM

The Aeroflex UTMC Mentor Graphics Design System software is fully integrated into the Mentor Graphics design environment, making it familiar and easy to use. Aeroflex UTMC tools support Mentor functions such as cross-highlighting, graphical menus, and design navigation.



Aeroflex UTMC Mentor Graphics Design

After creating a design in the Mentor Graphics environment, you can easily verify the design for electrical rules compliance with the Aeroflex UTMC Logic Rules Checker. Testability can be verified with the Aeroflex UTMC Tester Rules Checker. Both of these tools are fully integrated into the Mentor Graphics Environment.

When you have completed all design activities, Aeroflex UTMC's Design Transfer tool captures all the required files and prepares them for easy transfer to Aeroflex UTMC. Aeroflex UTMC uses this data to convert your design into a packaged and tested device.

ADVANTAGES OF THE AEROFLEX UTMC MENTOR DESIGN SYSTEM

- Aeroflex UTMC customers have successfully used the Aeroflex UTMC Mentor Graphics Design System for over a decade.
- Aeroflex UTMC's Logic and Tester Rules Checker tools allow you to verify partial or complete designs for compliance with Aeroflex UTMC manufacturing practices and procedures.
- The Design System accepts pre-and post-layout timing information to ensure your design results in devices that meet your specifications.
- The Design System supports Leonardo, and database transfer between Synopsys and Mentor.
- The Design System supports powerful Mentor Graphics ATPG capabilities.

TOOLS SUPPORTED BY AEROFLEX UTMC

Aeroflex UTMC supports libraries for:

- Mentor Graphics
- ModelSim
- Synopsys
- Design Compiler
- PrimeTime
- Formality
- TetraMax
- VITAL-compliant VHDL Tools
- OVI-compliant Verilog Tools

TRAINING AND SUPPORT

Aeroflex UTMC personnel conduct training classes tailored to meet individual needs. These classes can address a wide mix of engineering backgrounds and specific customer concerns. Applications assistance is also available through all phases of ASIC Design.

PHYSICAL DESIGN

Using three layers of metal interconnect, Aeroflex UTMC achieves optimized layouts that maximize speed of critical nets, overall chip performance, and design density up to 600,000 equivalent gates.

Test Capability

Aeroflex UTMC supports all phases of test development from test stimulus generation through high-speed production test. This support includes ATPG, fault simulation, and fault grading. Scan design options are available on all UT0.6µCRH/SRH storage elements. Automatic test program development capabilities handle large vector sets for use with Aeroflex UTMC's LTX/ Trillium MicroMasters, supporting high-speed testing (up to 80MHz with pin multiplexing).

Unparalleled Quality and Reliability

Aeroflex UTMC is dedicated to meeting the stringent performance requirements of aerospace and defense systems suppliers. Aeroflex UTMC maintains the highest level of quality and reliability through our Quality Management Program under MIL-PRF-38535 and ISO-9001. In 1988, we were the first gate array manufacturer to achieve QPL certification and qualification of our technology families. Our product assurance program has kept pace with the demands of certification and qualification.

Our quality management plan includes the following activities and initiatives.

- Quality improvement plan
- Failure analysis program
- SPC plan
- Corrective action plan
- Change control program
- Standard Evaluation Circuit (SEC) and Technology Characterization Vehicle (TCV) assessment program
- Certification and qualification program

Because of numerous product variations permitted with customer specific designs, much of the reliability testing is performed using a Standard Evaluation Circuit (SEC) and Technology Characterization Vehicle (TCV). The TCV utilizes test structures to evaluate hot carrier aging, electromigration, and time dependent test samples for reliability testing. Data from the wafer-level testing can provide rapid feedback to the fabrication process, as well as establish the reliability performance of the product before it is packaged and shipped.

Radiation Tolerance

Aeroflex UTMC incorporates radiation-tolerance techniques in process design, design rules, array design, power distribution, and library element design. All key radiation-tolerance process parameters are controlled and monitored using statistical methods and in-line testing.

PARAMETER	RADIATION TOLERANCE	NOTES
Total dose	1.0E5 rad(SiO_2) 3.0E5 rad(SiO_2)	1 2
Dose rate upset	1.0E8 rad(Si)/sec	3
Dose rate survivability	1.0E11 rad(Si)/sec	4
SEU	<2.0E-10 errors per cell-day	4, 5
Projected neutron fluence	1.0E14 n/sq cm	
Latchup	Latchup-immune over specified use conditions	

Notes:

1. Total dose Co-60 testing is in accordance with MIL-STD-883, Method 1019. Data sheet electrical characteristics guaranteed to 1.0E5 rads(SiO_2). All post-radiation values measured at 25°C.
2. Total dose Co-60 testing is in accordance with MIL-STD-883, Method 1019 at dose rates <1 rad(SiO_2)/s.
3. Short pulse 20ns FWHM (full width, half maximum).
4. Is design dependent; SEU limit based on standard evaluation circuit at 4.5V worst case condition.
5. SEU-hard flip-flop cell. Non-hard flip-flop typical is 4E-8.

ABSOLUTE MAXIMUM RATINGS [1]
(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{DD}	DC supply voltage	-0.3 to 6.0V
$V_{I/O}$	Voltage on any pin	-0.3V to V_{DD} + 0.3
T_{STG}	Storage temperature	-65 to +150°C
T_J	Maximum junction temperature	+175°C
I_{LU}	Latchup immunity	$\pm$150mA
I_I	DC input current	$\pm$10mA
T_{LS}	Lead temperature (soldering 5 sec)	+300°C

Note:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V_{DD}	Positive supply voltage	3.0 to 5.5V
T_C	Case temperature range	-55 to +125C
V_{IN}	DC input voltage	0V to V_{DD}

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0V $\pm$10%; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage [1] TTL inputs CMOS	V_{DD} = 4.5V and 5.5V			 0.8 $.3V_{DD}$	V
V_{IH}	High-level input voltage [1] TTL inputs CMOS	V_{DD} = 4.5V and 5.5V	 2.2 $.7V_{DD}$			V
V_T+	Schmitt Trigger, positive going [1] threshold	V_{DD} = 4.5V and 5.5V			$.7V_{DD}$	V
V_T-	Schmitt Trigger, negative going [1] threshold	V_{DD} = 4.5V and 5.5V	$.3V_{DD}$			V
V_H	Schmitt Trigger, typical range of hysteresis [2]		0.6			V
I_{IN}	Input leakage current TTL, CMOS, and Schmitt inputs Inputs with pull-down resistors Inputs with pull-down resistors Inputs with pull-up resistors Inputs with pull-up resistors Cold Spare Inputs - Normal Mode Cold Spare Inputs - Cold Spare Mode	V_{DD} = 5.5V V_{IN} = V_{DD} and V_{SS} V_{IN} = V_{DD} V_{IN} = V_{SS} V_{IN} = V_{SS} V_{IN} = V_{DD} V_{IN} = 0 to 5.5V V_{DD} = V_{SS} = 0V V_{IN} = V and 5.5V	 -1 +20 -5 -225 -5 -5 -5		 1 +225 +5 -20 +5 +5 +5	µA
V_{OL}	Low-level output voltage[3] TTL 2.0mA buffer TTL 4.0mA buffer TTL 8.0mA buffer TTL 12.0mA buffer * CMOS outputs CMOS outputs (optional) CMOS outputs (cold spare)	V_{DD} = 4.5V I_{OL} = 2.0mA I_{OL} = 4.0mA I_{OL} = 8.0mA I_{OL} = 12.0mA I_{OL} = 1.0µA I_{OL} = 100µA I_{OL} = 100µA			 0.4 0.4 0.4 0.4 0.05 0.25 0.25	V
V_{OH}	High-level output voltage[3] TTL 2.0mA buffer TTL 4.0mA buffer TTL 8.0mA buffer TTL 12.0mA buffer * CMOS outputs CMOS outputs (optional) CMOS outputs (cold spare)	V_{DD} = 4.5V I_{OH} = -2.0mA I_{OH} = -4.0mA I_{OH} = -8.0mA I_{OH} = -12.0mA I_{OH} = -1.0µA I_{OH} = -100µA I_{OH} = -100µA	 2.4 2.4 2.4 2.4 V_{DD}-0.05 V_{DD}-0.35 V_{DD}-0.35			V

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
I_{OZ}	Three-state output leakage current	V_{DD} = 5.5V				µA
	TTL 2.0mA buffer		-5		5	
	TTL 4.0mA buffer, CMOS		-10		10	
	TTL 8.0mA buffer		-20		20	
	TTL 12.0mA buffer *		-30		30	
	Cold Spare Inputs - normal mode	V_O = 0V and 5.5V	-5		-5	
	Cold Spare Inputs - cold spare mode	$V_{DD} = V_{SS} = 0$ V_{DD} = 0 to 5.5V	-5		-5	
I_{OS}	Short-circuit output current [2,4]	V_O = 0V and 5.5V				mA
	TTL 2.0mA buffer		-50		50	
	TTL 4.0mA buffer, CMOS		-100		100	
	TTL 8.0mA buffer		-200		200	
	TTL 12.0mA buffer *		-300		300	
I_{DDQ}	Quiescent Supply Current [6]					µA
	Group A subgroups 1,3	V_{DD} = 5.5V				
		200K gates			50	
		400K gates			100	
		600K gates			180	
	Group A subgroup 2	V_{DD} = 5.5V				mA
		200K gates			1	
		400K gates			2	
		600K gates			3	
	Group A, subgroup 1	V_{DD} = 5.5V				mA
	RHA Designator: M, D, P, L, R	200K gates			4	
		400K gates			8	
		600K gates			12	
C_{IN}	Input capacitance [5]			17		pF
C_{OUT}	Output capacitance [5]					pF
	TTL 2.0mA buffer			17		
	TTL 4.0mA buffer			17		
	TTL 8.0mA buffer, CMOS			18		
	TTL 12.0mA buffer *			23		
C_{IO}	Bidirect I/O capacitance [5]					pF
	TTL 4.0mA buffer			16		
	TTL 8.0mA buffer, CMOS			19		
	TTL 12.0mA buffer *			23		

Notes:

* Contact Aeroflex UTMC prior to usage.

1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}(min) + 20\%, - 0\%$; $V_{IL} = V_{IL}(max) + 0\%, - 50\%$, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to $V_{IH}(min)$ and $V_{IL}(max)$.
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density $\leq$ 5.0E5 amps/cm ^{2}, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF*MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz @0V and a signal amplitude of $\leq$50mV RMS.
6. All inputs with internal pull-ups should be left floating. All other inputs should be tied high or low.

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V $\pm$.3V; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage [1] CMOS	V_{DD} = 3.0V and 3.6V			$.3V_{DD}$	V
V_{IH}	High-level input voltage [1] CMOS	V_{DD} = 3.0V and 3.6V	$.7V_{DD}$			V
V_T+	Schmitt Trigger, positive going [1] threshold	V_{DD} = 3.0V and 3.6V			$.7V_{DD}$	V
V_T-	Schmitt Trigger, negative going [1] threshold	V_{DD} = 3.0V and 3.6V	$.3V_{DD}$			V
V_H	Schmitt Trigger, typical range of hysteresis [2]		.6			V
I_{IN}	Input leakage current TTL, CMOS, and Schmitt inputs Inputs with pull-down resistors Inputs with pull-down resistors Inputs with pull-up resistors Inputs with pull-up resistors Cold Spare Inputs - normal mode Cold Spare Inputs - cold spare mode	V_{DD} = 3.6V V_{IN} = V_{DD} and V_{SS} V_{IN} = V_{DD} V_{IN} = V_{SS} V_{IN} = V_{SS} V_{IN} = V_{DD} V_{IN} = 0 to 3.6V V_{DD} = V_{SS} = 0V V_{IN} = V and 3.6V	 -1 +10 -5 -225 -5 -5 -5		 1 +225 +5 -10 +5 +5 +5	µA
V_{OL}	Low-level output voltage CMOS outputs CMOS outputs (optional) CMOS outputs (cold spare)	 I_{OL} = 1.0µA I_{OL} = 100µA I_{OL} = 100µA			 0.05 0.25 0.25	V
V_{OH}	High-level output voltage CMOS outputs CMOS outputs (optional) CMOS outputs (cold spare)	 I_{OH} = -1.0µA I_{OH} = -100µA I_{OH} = -100µA	 V_{DD}-0.05 V_{DD}-0.35 V_{DD}-0.35			V

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
I_{OZ}	Three-state output leakage current CMOS	V_{DD} = 3.6V	-20		20	µA
	Cold Spare Inputs - normal mode	$V_O = V_{DD}$ and V_{SS}	-5		5	
	Cold Spare Inputs - cold spare mode	$V_{DD} = V_{SS}$ = 0V V_O = 0V and 3.6V	-5		5	
I_{OS}	Short-circuit output current [2,4] CMOS	$V_O = V_{DD}$ and V_{SS}	-200		200	mA
I_{DDQ}	Quiescent Supply Current [6] Group A subgroups 1,3	V_{DD} = 5.5V 200K gates 400K gates 600K gates			 50 100 180	µA
	Group A subgroup 2	V_{DD} = 5.5V 200K gates 400K gates 600K gates			 1 2 3	mA
	Group A, subgroup 1 RHA designator: M, D, P, L, R	V_{DD} = 5.5V 200K gates 400K gates 600K gates			 4 8 12	mA
C_{IN}	Input capacitance [5]			17		pF
C_{OUT}	Output capacitance [5] CMOS			18		pF
C_{IO}	Bidirect I/O capacitance [5] CMOS			19		pF

Notes:

* Contact Aeroflex UTMC prior to usage.

1. Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions: $V_{IH} = V_{IH}$(min) + 20%, - 0%; $V_{IL} = V_{IL}$(max) + 0%, - 50%, as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to V_{IH}(min) and V_{IL}(max).
2. Supplied as a design limit but not guaranteed or tested.
3. Per MIL-PRF-38535, for current density $\leq$ 5.0E5 amps/cm^2, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765pF*MHz.
4. Not more than one output may be shorted at a time for maximum duration of one second.
5. Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and V_{SS} at frequency of 1MHz @0V and a signal amplitude of $\leq$50mV RMS.
6. All inputs with internal pull-ups should be left floating. All other inputs should be tied high or low.

Notes