FEATURES

- PC100 compliant functionality and performance.
- JEDEC standard 3.3 V ± 10% power supply.
- LVTTL compatible inputs and outputs.
- All inputs are sampled on positive edge of system clock.
- Dual Banks for hidden row access/precharge.
- Internal pipeline operation, column addresses can be changed every cycle.
- DQM for masking.
- MRS cycle with address key programmability for:
  - CAS latency (2 , 3)
  - Burst Length (1 , 2 , 4 , 8 or full page)
  - Burst Type (Sequential & Interleave)
- Auto Precharge and Auto Refresh modes.
- Self Refresh Mode.
- 64ms , 4096 cycle refresh (15.6 us/row)
- 50–pin 400 mil plastic TSOP (type II) package.

GENERAL DESCRIPTION

The UT52L1616 is a high-speed CMOS dynamic random-access memory containing 16,777,216 bits. It is internally configured as a dual memory array (512K x 16) with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the two internal banks is organized with 2,048 rows and with either 256 columns by 16 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command which will then be followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed (A11 selects the bank, A0-10 selects the row). The address bits coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The UT52L1616 uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2n rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high speed, fully random access. Precharging one bank while accessing the alternate bank will hide the precharge cycles and provides seamless high-speed random access operation. The UT52L1616 is designed to comply with the Intel PC (66MHz) and Intel PC/100 (100MHz) specifications.

The UT52L1616 is designed to operate in 3.3V, low-power memory systems. An AUTO REFRESH mode is provided along with a power saving Power-Down mode. All inputs and outputs are LVTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

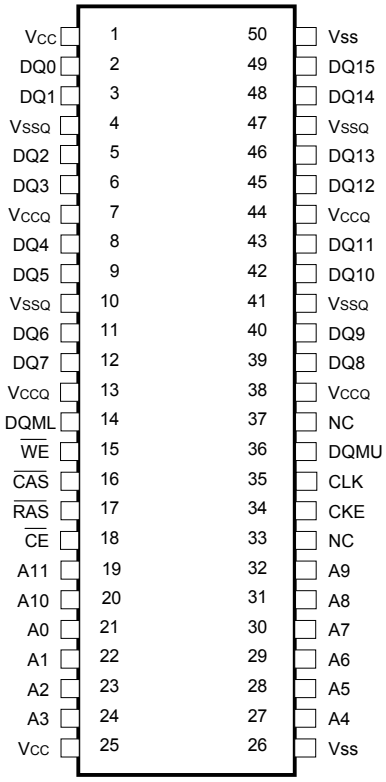
PRODUCT FAMILY

Part NO.	Max Freq.	CL	tAC	Organization	Interface	Package
UT52L1616MC-7	143MHZ	3	5.5ns	2 banks×512K bits×16	LVTTL	400 mil 50pin TSOP II
UT52L1616MC-8	125MHZ	3	6ns			
UT52L1616MC-10	100MHZ	3	7ns			

PIN ASSIGNMENT

UT52L1616

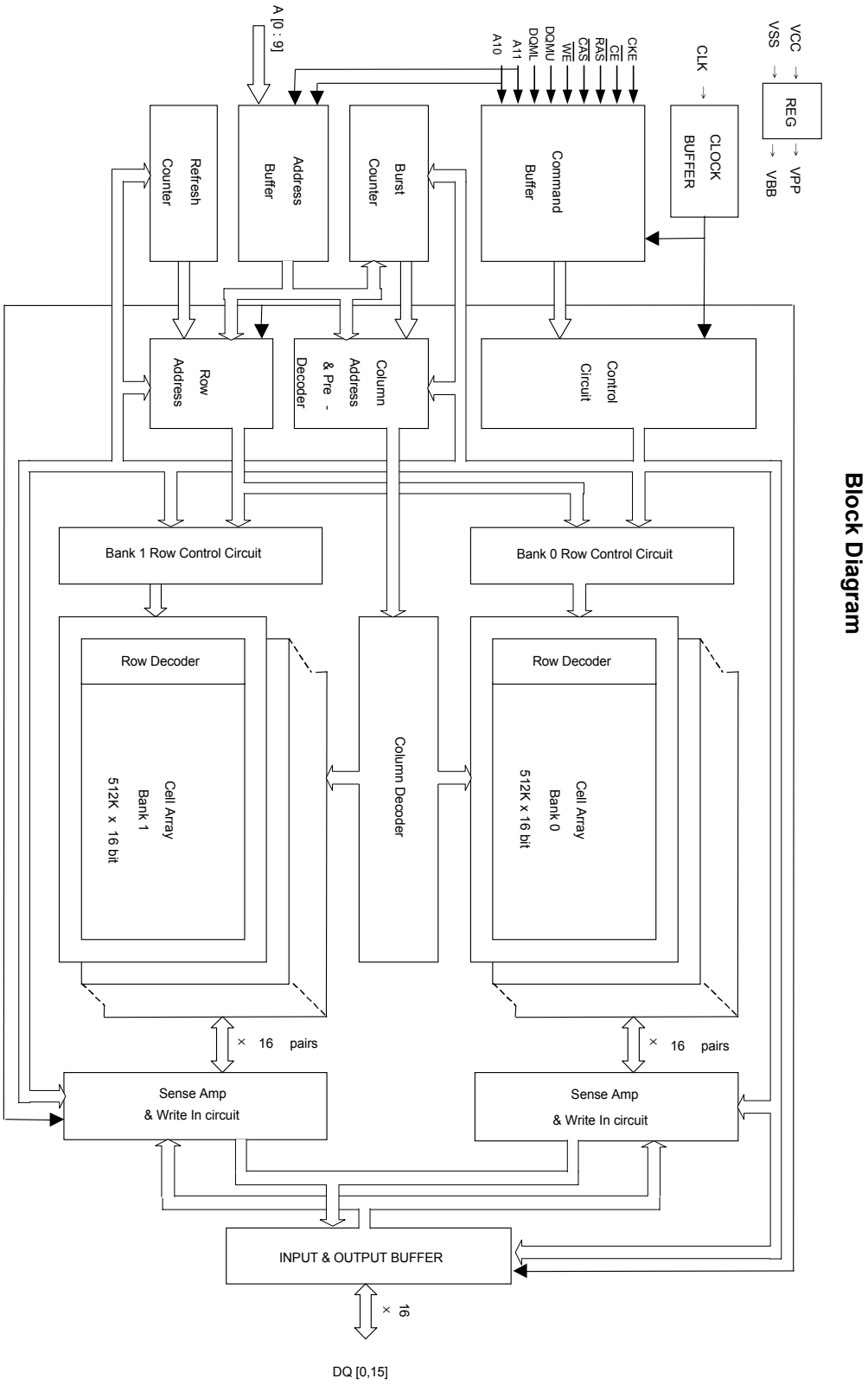
50 pin TSOP II package



PIN DESCRIPTION

Pin name	Function
A0 to A11	Address input ● Row address A0 to A10 ● Column address A0 to A7 ● Bank select address A11
DQ0 to DQ15	Data-input/output
$\overline{CE}$	Chip select
$\overline{CAS}$	Column address strobe command
$\overline{RAS}$	Row address strobe command
$\overline{WE}$	Write enable command
DQMU DQML	Upper byte input/output mask Lower byte input/output mask
CLK	Clock input
CKE	Clock enable
V_{CC}	Power for internal circuit
Vss	Ground for internal circuit
VccQ	Power for I/O circuit
VssQ	Ground for I/O circuit
NC	No connection

FUNCTION BLOCK DIAGRAM



Block Diagram

PIN FUNCTIONS

CLK (input pin): CLK is the master clock input to this pin. The other input signals are referred at CLK rising edge.

$\overline{CE}$ (input pin): When $\overline{CE}$ is Low, the command input cycle becomes valid. When $\overline{CE}$ is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (input pins): Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.

A0 to A10 (input pins): Row address (AX0 to AX10) is determined by A0 to A10 level at the bank active command cycle CLK rising edge. Column address (AY0 to AY7) is determined by A0 to A7 level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by A11 (BS) is precharged.

A11 (input pin): A11 is a bank select signal (BS). The memory array of the UT52L1616 is divided into bank 0 and bank 1, both which contain 512 K x 16 bits. If A11 is Low, bank 0 is selected, and if A11 is High, bank 1 is selected.

CKE (input pin): This pin determines whether or not the next CLK is valid. If CKE is High, the next CLK rising edge is valid. If CKE is Low, the next CLK rising edge is invalid. This pin is used for power down and clock suspend modes.

DQMU/DQML (input pins): DQMU controls upper byte and DQML controls lower byte input/output buffers.

Read operation: If DQMU/DQML is High, the output buffer becomes High-Z. If the DQMU/DQML is Low, the output buffer becomes Low-Z.

Write operation: If DQMU/DQML is High, the previous data is held (the new data is not written).If DQMU/DQML is Low, the data is written.

DQ0 to DQ15 (I/O pins): Data is input to and output from these pins. These pins are the same as those of a conventional DRAM.

Vcc and VccQ (power supply pins): 3.3V is applied. (Vcc is for the internal circuit and VccQ is for the output buffer.)

Vss and VssQ (power supply pins): Ground is connected. (Vss is for the internal circuit and VssQ is for the output buffer.)

COMMAND OPERATION

Command Truth Table

The synchronous DRAM recognizes the following commands specified by the $\overline{CE}$, $\overline{CAS}$, $\overline{RAS}$, $\overline{WE}$ and address pins.

Function	Symbol	CKE n-1	CKe n	$\overline{CE}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10	A0 to A9
Ignore command	DESL	H	x	H	x	x	x	x	x	x
Mode register set	MRS	H	x	L	L	L	L	V	V	V
Refresh	REF/SELF	H	V	L	L	L	H	x	x	x
Precharge select bank	PRE	H	x	L	L	H	L	V	L	x
Precharge all bank	PALL	H	x	L	L	H	L	x	H	x
Bank active	ACT	H	x	L	L	H	H	V	V	V
Column address and write command	WRIT	H	x	L	H	L	L	V	L	V
Write with auto-precharge	WRITA	H	x	L	H	L	L	V	H	V
Column address and read command	READ	H	x	L	H	L	H	V	L	V
Read with auto-precharge	READA	H	x	L	H	L	H	V	H	V
Burst stop in full page	BST	H	x	L	H	H	L	x	x	x
No operation	NOP	H	x	L	H	H	H	x	x	x

Note: H: V_{IH}. L: V_{IL}. x: V_{IH} or V_{IL}. V: Valid address input.

Ignore Command [DESL]: When this command is set ($\overline{CE}$ is High), the synchronous DRAM ignore command input at the clock. However, the internal status is held.

Mode register set [MRS]: Synchronous DRAM has a mode register that defines how it operates. The mode register is specified by the address pins (A0 to A11) at the mode register set cycle. For details, refer to the mode register configuration. After power on, the contents of the mode register are undefined, execute the mode register set command to set up the mode register.

Refresh [REF/SELF]: This command starts the refresh operation. There are two types of refresh operation, the one is auto refresh, and the other is self refresh. For details, refer to the CKE truth table section.

Precharge selected bank [PRE]: This command starts precharge operation for the bank selected by A11. If A11 is Low, bank 0 is selected. If A11 is High, bank 1 is selected.

Precharge all banks [PALL]: This command starts a precharge operation for all banks.

Row address strobe and bank activate [ACT]: This command activates the bank that is selected by A11 (BS) and determines the row address (AX0 to AX10). When A11 is Low, bank 0 is activated. When A11 is High, bank 1 is activated.

Column address strobe and write command [WRIT]: This command starts a write operation. When the burst write mode is selected, the column address (AY0 to AY7) and the bank select address (A11) become the burst write start address. When the single write mode is selected, data is only written to the location specified by the column address (AY0 to AY7) and the bank select address (A11).

Write with auto precharge [WRIT A]: This command automatically performs a precharge operation after a burst write with a length of 1, 2, 4 or 8.

Column address strobe and read command [READ]: This command starts a read operation. In addition, the start address of burst read is determined by the column address (AY0 to AY7) and the bank select address (BS). After the read operation, the output buffer becomes High-Z.

Read with auto precharge [READ A]: This command automatically performs a precharge operation after a burst read with a burst length of 1, 2, 4 or 8.

Burst stop command [BST]: This command stops the current burst operation.

No operation [NOP]: This command is not an execution command. However, the internal operations continue.

DQM Truth Table

Function	Symbol	CKE n - 1	CKE n	DQMU	DQML
Upper byte write enable/output enable	ENBU	H	x	L	x
Lower byte write enable/output enable	ENBL	H	x	x	L
Upper byte write inhibit/output disable	MASKU	H	x	H	x
Lower byte write inhibit/output disable	MASKL	H	x	x	H

Note: H: V_{IH}. L: V_{IL}. x: V_{IH} or V_{IL}.

The UT52L1616 can mask input/output data by means of DQMU and DQML. DQMU masks the upper byte and DQML masks the lower byte.

During reading, the output buffer is set to Low-Z by setting DQMU/DQML to Low, enabling data output. On the other hand, when DQMU/DQML is set to High, the output buffer becomes High-Z, disabling data output.

During writing, data is written by setting DQMU/DQML to Low. When DQMU/DQML is set to High, the previous data is held (the new data is not written). Desired data can be masked during burst read or burst write by setting DQMU/DQML. For details, refer to the DQM control section of the UT52L1616 operating instructions.

CKE Truth Table

Current state	Function	CKE n-1	CKE n	$\overline{CE}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
Active	Clock suspend mode entry	H	L	H	X	X	X	X
Any	Clock suspend	L	L	X	X	X	X	X
Clock suspend	Clock suspend mode exit	L	H	L	H	H	H	X
		L	H	H	X	X	X	X
Idle	Auto-refresh command REF	H	H	L	L	L	H	X
Idle	Self-refresh entry SELF	H	L	L	L	L	H	X
Idle	Power down entry	H	L	L	H	H	H	X
		H	L	H	X	X	X	X
Self refresh	Self refresh exit SELFX	L	H	L	H	H	H	X
		L	H	H	X	X	X	X
Power down	Power down exit	L	H	L	H	H	H	X
		L	H	H	X	X	X	X

Note: H: V_{IH}. L: V_{IL}. x: V_{IH} or V_{IL}.

Clock suspend mode entry: The synchronous DRAM enters clock suspend mode from active mode by setting CKE to Low. The clock suspend mode changes depending on the current status (1 clock before) as shown below.

ACTIVE clock suspend: This suspend mode ignores inputs after the next clock by internally maintaining the bank active status.

READ suspend and READ A suspend: The data being output is held (and continues to be output).

WRITE suspend and WRIT A suspend: In this mode, external signals are not accepted. However, the internal state is held.

Clock suspend mode exit: The synchronous DRAM exits from clock suspend mode by setting CKE to High during the clock suspend state.

IDLE: In this state, all banks are not selected, and completed precharge operation.

Auto refresh command [REF]: When this command is input from the IDLE state, the synchronous DRAM starts auto-refresh operation, (The auto-refresh is the same as the REF refresh of conventional DRAMs.) During the auto-refresh operation, refresh address and bank select address are generated inside the synchronous DRAM. For every auto-refresh cycle, the internal address counter is updated. Accordingly, 2048 times are required to refresh the entire memory. Before executing the auto-refresh command, all the banks must be in the IDLE state. In addition, since the precharge for all banks is automatically performed after auto-refresh, no precharge command is required after auto refresh.

Self refresh entry [SELF]: When this command is input during the IDLE state, the synchronous DRAM starts self refresh operation. After the execution of this command, self refresh continues while CKE is Low. Since self refresh is performed internally and automatically, external refresh operations are unnecessary.

Power down mode entry: When this command is executed during the IDLE state, the synchronous DRAM enters power down mode. In power down mode, power consumption is suppressed by cutting off the initial input circuit.

Self refresh exit: When this command is executed during self refresh mode, the synchronous DRAM can exit from self refresh mode. After exiting from self refresh mode, the synchronous DRAM enters the IDLE state.

Function Truth Table

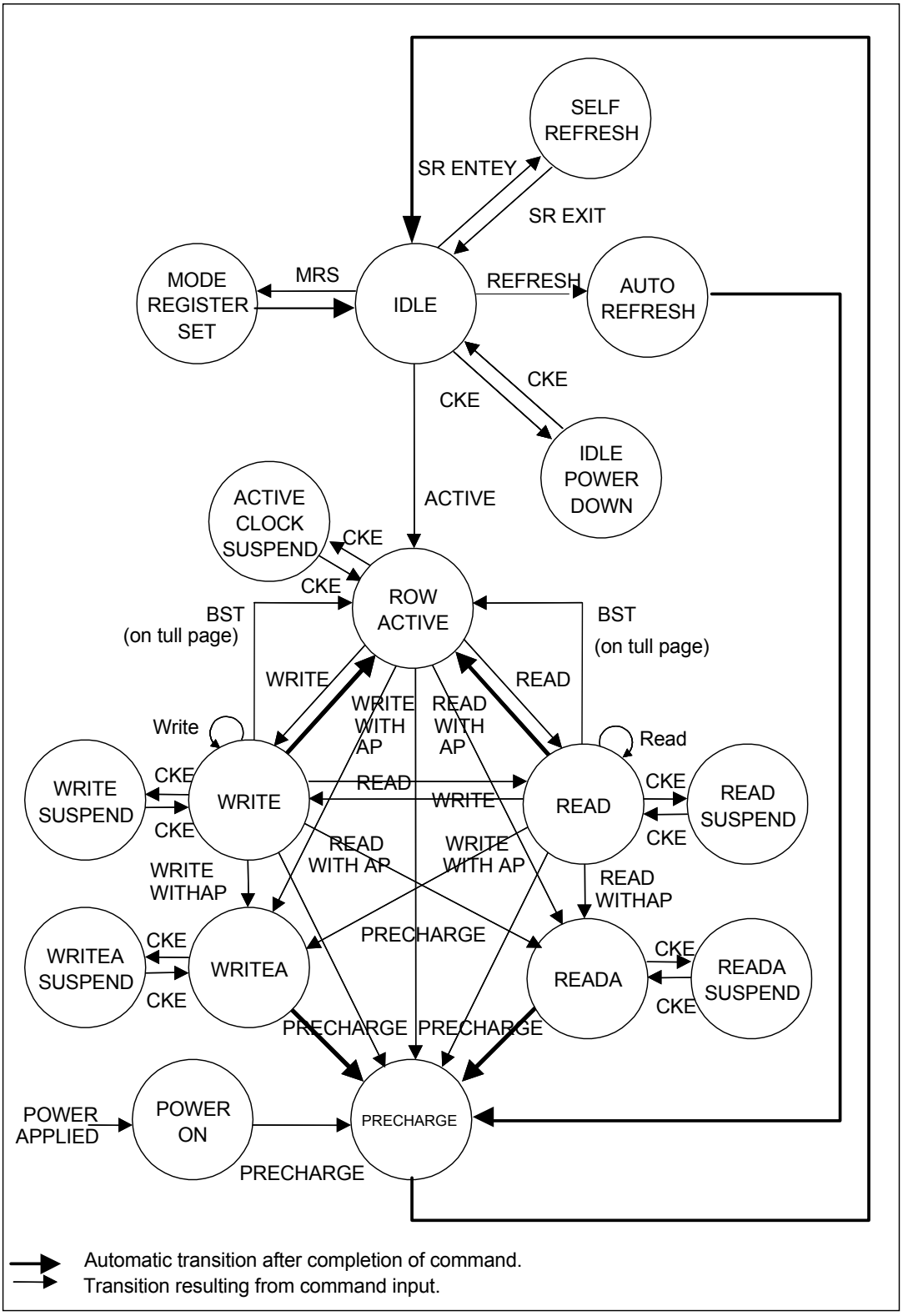
The following table shows the operations that are performed when each command is issued in each mode of the synchronous DRAM.

Current state	$\overline{CE}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Precharge	H	X	X	X	X	DESL	Enter IDLE after t_{RP}
	L	H	H	H	X	NOP	Enter IDLE after t_{RP}
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA,CA,A10	READ/READ A	ILLEGAL
	L	H	L	L	BA,CA,A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA,RA	ACT	ILLEGAL
	L	L	H	L	BA,A10	PRE,PALL	ILLEGAL
	L	L	L	H	X	REF,SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Idle	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA,CA,A10	READ/READ A	ILLEGAL
	L	H	L	L	BA,CA,A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA,RA	ACT	Bank and row active
	L	L	H	L	BA,A10	PRE,PALL	NOP
	L	L	L	H	X	REF,SELF	Refresh
	L	L	L	L	MODE	MRS	Mode register set
Row active	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA,CA,A10	READ/READ A	Begin read
	L	H	L	L	BA,CA,A10	WRIT/WRIT A	Begin write
	L	L	H	H	BA,RA	ACT	Other bank active; ILLEGAL on same bank*3
	L	L	H	L	BA,A10	PRE,PALL	Precharge
	L	L	L	H	X	REF,SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Read	H	X	X	X	X	DESL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Burst stop to full page
	L	H	L	H	BA,CA,A10	READ/READ A	Continue burst read to CAS latency and New read
	L	H	L	L	BA,CA,A10	WRIT/WRIT A	Term burst read/start write
	L	L	H	H	BA,RA	ACT	Other bank active; ILLEGAL on same bank*3
	L	L	H	L	BA,A10	PRE,PALL	Term burst read and Precharge
	L	L	L	H	X	REF,SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Write	H	X	X	X	X	DESL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Burst stop on full page
	L	H	L	H	BA,CA,A10	READ/READ A	Term burst and New read
	L	H	L	L	BA,CA,A10	WRIT/WRIT A	Term burst and New read
	L	L	H	H	BA,RA	ACT	Other bank active; ILLEGAL on same bank*3
	L	L	H	L	BA,A10	PRE,PALL	Term burst write and Precharge*2
	L	L	L	H	X	REF,SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Current state	$\overline{CE}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Write with auto	H	X	X	X	X	DESL	Continue burst to end and precharge
precharge	L	H	H	H	X	NOP	Continue burst to end and precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA,CA,A10	READ/READ A	ILLEGAL
	L	H	L	L	BA,CA,A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA,RA	ACT	Other bank active; ILLEGAL on same bank*3
	L	L	H	L	BA,A10	PRE,PALL	ILLEGAL
	L	L	L	H	X	REF,SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Refresh	H	X	X	X	X	DESL	Enter IDLE after t_{RC}
(auto refresh)	L	H	H	H	X	NOP	Enter IDLE after t_{RC}
	L	H	H	L	X	BST	Enter IDLE after t_{RC}
	L	H	L	H	BA,CA,A10	READ/READ A	ILLEGAL
	L	H	L	L	BA,CA,A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA,RA	ACT	ILLEGAL
	L	L	H	L	BA,A10	PRE,PALL	ILLEGAL
	L	L	L	H	X	REF,SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Notes H: V_{IH}. L: V_{IL}. x:V_{IH} or V_{IL}.
1. The other combinations are inhibit.
2. An interval of t_{RWL} is required between the final valid data input and the precharge command.
3. If t_{RRD} is not satisfied, other bank active command is illegal.

SIMPLIFIED STATE DIAGRAM



DEVICE OPERATION

Power Up Sequence

- Apply power and start clock, attempt to maintain CKE= “H”, DQM= “H”. Other pins are NOP condition at their inputs.
- Maintain stable power, stable clock and NOP input condition for a minimum of 200us.

Initialization Sequence

After the following initialization sequence, the device is ready for full functionality:

- Precharge both banks.
- Issue 2 or more Auto refresh (REF) commands to the device.
- Issue a mode register set (MRS) command to set the device mode of operation.
- After t_{MRD0} (3 clocks) is met. The device is ready for operation.
  ** Step 2 and 3 are interchangeable.

Precharge Select bank (PRE)

The precharge operation will be performed on the active bank when the precharge selected bank command is issued. When the precharge command is issued with address A10 low, A11 selects the bank to be precharged. At the end of the precharge selected bank command the selected bank will be in idle state after the minimum t_{RP} is met.

Precharge All (PALL)

Both banks are precharged at the same time when this command is issued. When the precharge command is issued with address A10 high then all banks will be precharged. At the end of the precharge all command both banks will be in idle state after the minimum t_{RP} is met.

Auto Precharge

AUTO PRECHARGE is a feature which performs the same individual-bank PRECHARGE function described above, but without requiring an explicit command. This is accomplished by using A10 to enable AUTO PRECHARGE in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst, except in the full-page burst mode, where AUTO PRECHARGE does not apply. AUTO PRECHARGE is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command. AUTO PRECHARGE ensures that the PRECHARGE is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (t_{RP}) is completed. This is determined as if an explicit PRECHARGE command was issued at the earliest possible time, as described for each burst type in the Operation section of this data sheet.

Burst Terminate

The BURST TERMINATE command is used to truncate either fixed-length or full-page bursts. The most recently registered READ or WEITE command prior to the BURST TERMINATE command will be truncated as shown in the Operation section of this data sheet.

NOP and Device Deselect (NOP, DESL)

The device is deselected by deactivating the $\overline{CE}$ signal. In this mode the device ignores all the control inputs. The SDRAMs are put in NOP mode when $\overline{CE}$ is active and by deactivating, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$. For both Deselect and NOP the device will finish the current operation when this command is issued.

Row Activate (ACT)
This command is used to select a row in a specified bank of the device. Read and write operation can only be initiated on this activated bank after the minimum t_{RCD} time has elapsed from the activate command.

Read Bank (READ)
This command is issued after the row activate command to initiate the burst read of data. The read command is initiated by activating $\overline{CE}$, $\overline{CAS}$ and deasserting $\overline{WE}$ at the same clock sampling (rising) edge as described in the command truth table. The length of the burst and the $\overline{CAS}$ latency time will be determined by the values programmed during the MRS command.

Write Bank (WRIT)
This command is used after the row activate command to initiate the burst write of data. The write command is initiated by activating $\overline{CE}$, $\overline{CAS}$ and $\overline{WE}$ at the same clock sampling (rising) edge as described in the command truth table. The length of the burst will be determined by the values programmed during the MRS command.

Functionality of SDRAM device:
The following operations are supported by SDRAM:
- Burst Read
- Burst Write
- Multi bank Ping-Pong access
- Burst Read with Autoprecharge
- Burst Write with Autoprecharge
- Burst Read terminated with precharge
- Burst Write terminated with precharge
- Burst Read terminated with another Burst Read/Write
- Burst Write terminated with another Burst Write/Read
- DQM masking
- Fastest command to command delay of 1 clock
- Precharge All command
- Auto Refresh
- CL=2,3
- Burst Length 1,2,4, 8 and full page (256)
- Self Refresh Command
- Power down
- Terminating a read burst
- Terminating a write burst

Mode Register Set (MRS)
This command is used to program the SDRAM for the desired operating mode. This command is normally used after power up as defined in the power up sequence before the actual operation of the SDRAM is initiated. The functionality of the SDRAM device can be altered by re-programming the mode register through the execution of Mode Register Set command. Both banks must be precharged (i.e. in idle state) before the MRS command can be issued.

Mode Register Definition
The mode register is set by the input to the address pins (A0 to A11) during mode register set cycles. The mode register consists of five sections, each of which is assigned to address pins.

A11, A10, A9, A8 : (OP Mode):
The synchronous DRAM has two types of write modes. One is the burst write mode, and the other is the single write mode. These bits specify write mode.

Burst read and burst write:
Burst write is performed for the specified burst length starting from the column address specified in the write cycle.

Burst read and single write:
Data is only written to the column address specified during the write cycle, regardless of the burst length.

A6, A5, A4: (CAS Latency):
These pins specify the CAS latency.

A3: (BT):
A burst type is specified. When full-page burst is performed, only "sequential" can be selected.

A2, A1, A0: (Burst Length):
These pins specify the burst length.

Mode Register Configuration

The mode register is set by the input to the address pins (A0 to A11) during mode register set cycles. The mode register consists of five sections, each of which is assigned to address pins.

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
OPCODE				0	LMODE			BT	BL		

A6	A5	A4	CAS Latency
0	0	0	R
0	0	1	1
0	1	0	2
0	1	1	3
1	-	-	R

A3	Burst Type
0	Sequential
1	Interleave

A2	A1	A0	Burst Length	
			BT=0	BT=1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	R	R
1	0	1	R	R
1	1	0	R	R
1	1	1	F.P.	R

A11	A10	A9	A8	Write mode
0	0	0	0	Burst read and burst write
X	X	0	1	R
0	0	1	0	Burst read and Single wirte
X	X	1	1	R

F.P.= Full Page(256)

R is Reserved (inhibit)

.= 0 or 1

Burst length = 2

Starting Ad.	Addressing (decimal)	
A0	Sequence	Interleave
0	0, 1,	0, 1,
1	1, 0,	1, 0,

Burst length = 4

Starting Ad.		Addressing (decimal)	
A1	A0	Sequence	Interleave
0	0	0, 1, 2, 3,	0, 1, 2, 3,
0	1	1, 2, 3, 0,	1, 0, 3, 2,
1	0	2, 3, 0, 1,	2, 3, 0, 1,
1	1	3, 0, 1, 2,	3, 2, 1, 0,

Burst length = 8

Starting Ad.			Addressing (decimal)	
A2	A1	A0	Sequence	Interleave
0	0	0	0, 1, 2, 3, 4, 5, 6, 7,	0, 1, 2, 3, 4, 5, 6, 7,
0	0	1	1, 2, 3, 4, 5, 6, 7, 0,	1, 0, 3, 2, 5, 4, 7, 6,
0	1	0	2, 3, 4, 5, 6, 7, 0, 1,	2, 3, 0, 1, 6, 7, 4, 5,
0	1	1	3, 4, 5, 6, 7, 0, 1, 2,	3, 2, 1, 0, 7, 6, 5, 4,
1	0	0	4, 5, 6, 7, 0, 1, 2, 3,	4, 5, 6, 7, 0, 1, 2, 3,
1	0	1	5, 6, 7, 0, 1, 2, 3, 4,	5, 4, 7, 6, 1, 0, 3, 2,
1	1	0	6, 7, 0, 1, 2, 3, 4, 5,	6, 7, 4, 5, 2, 3, 0, 1,
1	1	1	7, 0, 1, 2, 3, 4, 5, 6,	7, 6, 5, 4, 3, 2, 1, 0,

Multi-bank ping pong access
Two-bank Ping-Pong accesses are described in the following diagram. Another bank can be activated while the first bank is being accessed as shown. RAS to RAS delay t_{RRD} must be met while activating another bank.

Read and Write with Autoprecharge
Burst reads and writes with auto precharge commands are initiated with Autoprecharge if A10 is at a high state while the read or write commands are issued.

Precharge Termination of Burst
Burst reads and writes without Autoprecharge can be terminated prematurely by a precharge command. If the burst read or write command was issued in auto precharge mode then the commands may not be terminated prematurely for that bank.

Precharge Command After a Burst Read
The earliest a precharge command can be issued after a Read command without the loss of data is CL + BL – 2 clocks. The precharge command can be issued as soon as the t_{RAS} time is met. The earliest time that precharge can be issued is shown for the CAS Latency = 3 device.

Precharge Termination of a Burst Read
Burst Read (with no Autoprecharge) can be terminated earlier using a precharge command along with the DQM . It allows starting the precharge early. The remaining data is undefined. DQM should be used to mask the invalid data.

Precharge Termination of a Burst Write
To terminate Burst Write early with precharge command the DQM signal must be used as shown. Data sampled t_{RDL} clocks before precharge command will be written correctly. Data sampled afterward and before the precharge command is undefined. DQM must be used to prevent the location from being corrupted. DQM must be asserted active to prevent location (A3 and A4 in this case) from being corrupted. DQ(A2) will be written correctly as t_{RDL} is met.

Read Terminated by Read
A Read command will terminate the previous read command and the data will be available after CAS Latency for the new command. Fastest command to command delay is determined by t_{CCD} (1 clock as shown).

Write Terminated by Write
A Write command will terminate the previous write command and the new burst write command will start with the new command as shown. Fastest command to command delay is determined by t_{CCD} (1 clock as shown).

Read Terminated by Write
A Write command terminates the previous read command and the new burst write will start . The minimum command delay for valid operation (i.e. read-modified-write) = CAS Latency + 2. The DQM must be held active for 3 clocks to keep the output buffer in Hi-Z as shown to prevent an internal IO buffer conflict between the read data (in pipe) and the write data driven on the input pins.

SDRAM commands to two banks in consecutive clocks
Given COMMAND1 detected by SDRAM component (to bank(i)), it will handle correctly COMMAND2 (to bank(j)) that is detected in the next clock or later clock.
Also, note that COMMAND1 (or COMMAND2) can be: Precharge-Bank, Internally-Scheduled_Auto-Precharge, Activate, Read or Write. Command1/2 cannot be a Precharge-All. Next command to same bank after Precharge

Write Terminated by Read
A Read command terminates the previous write command and the new burst read will start as shown. In case of t_{CCD}=1, CL=3, and t_{DQZ}=2, there is no loss of data bandwidth even if DQM is activated to mask the write data
.
The Burst Stop Command is defined by having $\overline{RAS}$ and $\overline{CAS}$ high with, $\overline{CAS}$ and $\overline{WE}$ low at the rising edge of the clock. When using the Burst Stop Command during a burst read cycle, it should be issued x cycles before the clock edge at which the last desired data element is valid, where x equals the CAS latency minus one.

When using the Burst Stop Command during a burst write cycle, the input data applied coincident with the Burst Stop Command will be ignored. The last data written (provided that DQM is low at that time) will be the input data applied one clock previous to the Burst Stop Command.

Precharge-Bank
If a Precharge-Bank command (to bank(k)) is detected by SDRAM component in CLK(n), then there can be no commands presented to this bank until CLK(n+t_{RP}).

Precharge-All
If a Precharge-All command is detected by SDRAM component in CLK(n), then there can be no commands presented to this component until CLK(n+t_{RP}).

Read-Auto Precharge
If a Read with Auto-Precharge command (to bank(k)) is detected by SDRAM component in CLK(n), then there can be no commands presented to this bank until CLK(n+CL+BL-2+t_{RP}).

Write-Auto Precharge
If a Write with Auto-Precharge command (to bank(k)) is detected by SDRAM component in CLK(n), then there can be no commands presented to this bank until CLK(n+BL+t_{DAL}-1).

Back to back command with Auto precharge
Read or write burst initiated with auto precharge (A10=high during read or write) will execute the read or write normally with the exception that after the burst operation is over the accessed bank will start precharge. To access the bank again the user must reactivate with an active bank command.
The commands initiated with auto-precharge cannot be terminated with any other commands for that bank.

Auto Refresh (REF) Command
An auto refresh (REF) refreshes the SDRAM array. Refresh addresses are generated internally by the SDRAM device and incremented after each auto refresh automatically. No commands (including another auto refresh) can be issued until a minimum t_{RC} is satisfied.

Self Refresh Entry/Exit
The self refresh mode is entered by holding $\overline{CE}$, $\overline{CAS}$, $\overline{RAS}$,CKE low and $\overline{WE}$ high at the rising edge of the clock. Once the SDRAM enters the Self Refresh mode, all inputs except CKE will be in a don't care state and outputs will be tri-stated. The external clock may be halted while the device is in Self Refresh mode, however, the clock must be restarted 200 cycles before CKE is high. The self refresh command is exited by asserting CKE high. A new command may be given t_{RC} clocks after CKE is high.

Multi-bank Operation
The following table specifies some of the timing parameters used for the timing diagrams. CL, t_{RCD} and t_{RP} can all have values of 2 or 3.

CL	CAS latency	3 clocks
BL	Burst Length	4
t_{RP}	RAS Precharge	3 clocks
t_{RAS}	RAS active time	5 clocks
t_{RCD}	RAS to CAS delay	3 clocks

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-1.0~4.6	V
Voltage on V_{CC} supply relative to V_{SS}	$V_{CC,}$ V_{CCQ}	-1.0~4.6	V
Storage temperature	T_{STG}	-55~+150	℃
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Notes: Permanent device damage may occur if Absolute Maximum Ratings are exceeded.
Functional operation should be restricted to recommended operation condition.
Exposurc to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS (T_A=0℃~+70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	$V_{CC,}$ V_{CCQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{CC}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2+mA
Output logic Low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2+mA
Input leakage current	I_{IL}	-5	-	5	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Notes: 1. V_{IH} (max) =4.6 V AC for pulse width ≤ 10 ns acceptable.
2. V_{IL} (min) = -1.5 V AC for pulse width ≤10 ns acceptable
3.Any input 0V ≤ V_{IN} ≤ V_{CC} + 0.3V. all other pins are not under test=0V.
4.Dout is disabled. 0V ≤ Vout ≤ V_{CC}

CAPACITANCE (V_{CC} =3.3V , T_A = 25°C, F = 1MHZ)

Pin	Symbol	Min	Max	Unit
CLOCK	C_{CLK}	2.5	4.0	pF
$\overline{RAS}$ $\overline{CAS}$ $\overline{WE}$ $\overline{CE}$ CKE, IDQM,UDQM	C_{IN}	2.5	5.0	pF
ADDRESS	C_{ADD}	2.5	5.0	pF
DQ0~DQ15	C_{OUT}	4.0	6.5	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted,T_A = 0 to 70ºC, V_{IH} (min)/ V_{IL} (max) = 2.0V/0.8V)

Parameter	Symbol	Test Condition	CAS Latency	Version -7	Version -8	Version -10	Unit	Note
Operating current (One Bank Active)	ICC1	Burst length =1 $t_{RC} \geq t_{RC}(min), t_{CK} \geq t_{CK}(min), I_{OL}$=0mA		100	80	70	mA	1
Precharge Standby Current in power-down mode	$I_{CC2}P$	CKE= V_{IL}(max), $t_{CK=min}$		3			mA	
	$I_{CC2}PS$	CKE= V_{IL}(max), CLK≤ V_{IL}(max), $t_{CK=}\infty$		2			mA	
Precharge Standby Current in non power-down mode	$I_{CC2}N$	CKE≥ V_{IH}(min), $\overline{CE}$ ≤ V_{IH}(max),t_{CK}=15ns Input signals are changed one time during 30ns		50			mA	
	$I_{CC2}NS$	CKE≥ V_{IH}(min),CLK≤ V_{IL}(max), $t_{CK}=\infty$ Input signals are stable		30			mA	
Active Standby Current in power-down mode	$I_{CC3}P$	CKE = V_{IL}(max), $t_{CK=min}$		5			mA	
	$I_{CC3}PS$	CKE = V_{IL}(max), CLK≤ V_{IL}(max), $t_{CK=}\infty$		3			mA	
Active Standby Current In non power-down mode (One Bank Active)	$I_{CC3}N$	CKE≥ V_{IH}(min), $\overline{CE}$ ≤ V_{IH}(max),t_{CK}=15ns Input signals are changed one time during 30ns		65			mA	
	$I_{CC3}NS$	CKE≥ V_{IH}(min),CLK≤ V_{IL}(max),$t_{CK}=\infty$ Input signals are stable		25			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL}=0mA, Page Burst All Band Activated. $t_{Ck}=t_{Ck}$(min) BL=4		160	150	140	MA	
				160	150	140	mA	1
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		160	150	140	mA	2
Self Refresh Current	I_{CC6}	CKE≤ 0.2V		2			mA	

Notes：1.Measured with outputs open. Addresses are changed only one time during t_{Ck}(min).
2.Refresh period is 32ms. Addresses are changed only time during t_{Ck}(min).

AC OPERAATING TEST CONDITIONS (V_{CC}=3.3V±0.3V,T_A=0 to 70 ℃)

Parameter	Value	Unit
Input levels(Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr / tf=1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig.1	

Ω

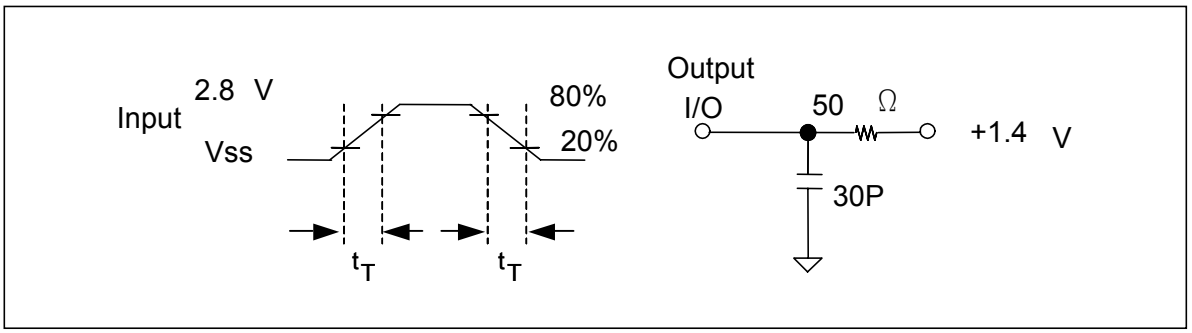


Fig.1

AC TIMEING CHARACTERISTICS (T_A=0℃~+70℃, Vcc=3V~3.6V)

Parameter		Symbol	-7		-8		-10		Unit	Note
			MIN	MAX	MIN	MAX	MIN	MAX		
CK cycle time	CL=3	t_{CK}	7		8	-	10	-	ns	-
	CL=2		12		12		12		ns	
CK high level width		t_{CH}	3	-	3	-	3	-	ns	-
CK low level width		t_{CL}	3	-	3	-	3	-	ns	-
Input setup time		t_{SS}	2	-	2	-	2	-	ns	-
Input hold time		t_{SH}	1	-	1	-	1	-	ns	-
Output valid from clock	CL=3	t_{AC}	-	5.5		6	-	7	ns	-
	CL=2			6		6		9	ns	
Output hold from clock		t_{OH}	2	-	2	-	2	-	ns	-
CAS to CAS delay		t_{CCD}	1	-	1	-	1	-	CLK	-
RAS to RAS bank active delay		t_{RRD}	2	-	2	-	2	-	CLK	-
DQM to input data delay		t_{DQD}	0	-	0	-	0	-	CLK	-
Write command to data-in delay		t_{DWD}	0	-	0	-	0	-	CLK	-
MRS to active delay		t_{MRD}	2	-	2	-	2	-	CLK	-
Precharge to O/P in high Z		t_{ROH}	CL	-	CL	-	CL	-	CLK	1
DQM to data in high Z for read		t_{DQZ}	2	-	2	-	2	-	CLK	-
DQM to data mask for write		t_{DQM}	0	-	0	-	0	-	CLK	-
Data-in to prechange command		t_{RDL}	2	-	2	-	2	-	CLK	-
Power down mode entry		t_{SB}	-	1	-	1	-	1	CLK	-
Self refresh exit time		t_{SRX}	1	-	1	-	1	-	CLK	-
Power down exit time		t_{PDE}	1	-	1	-	1	-	CLK	1

Note:
1. CL=CAS Latency

FREQUENCY vs AC PARAMETERS

UT52L1616-7

FREQUENCY	CL	t_{RC}	t_{RAS}	t_{RP}	t_{RCD}
143MHZ(7ns)	3	10	7	3	3
125MHZ(8ns)	3	9	6	3	3
100MHZ(10ns)	3	7	5	2	2
83MHZ(12ns)	2	6	4	2	2

UT52L1616-8

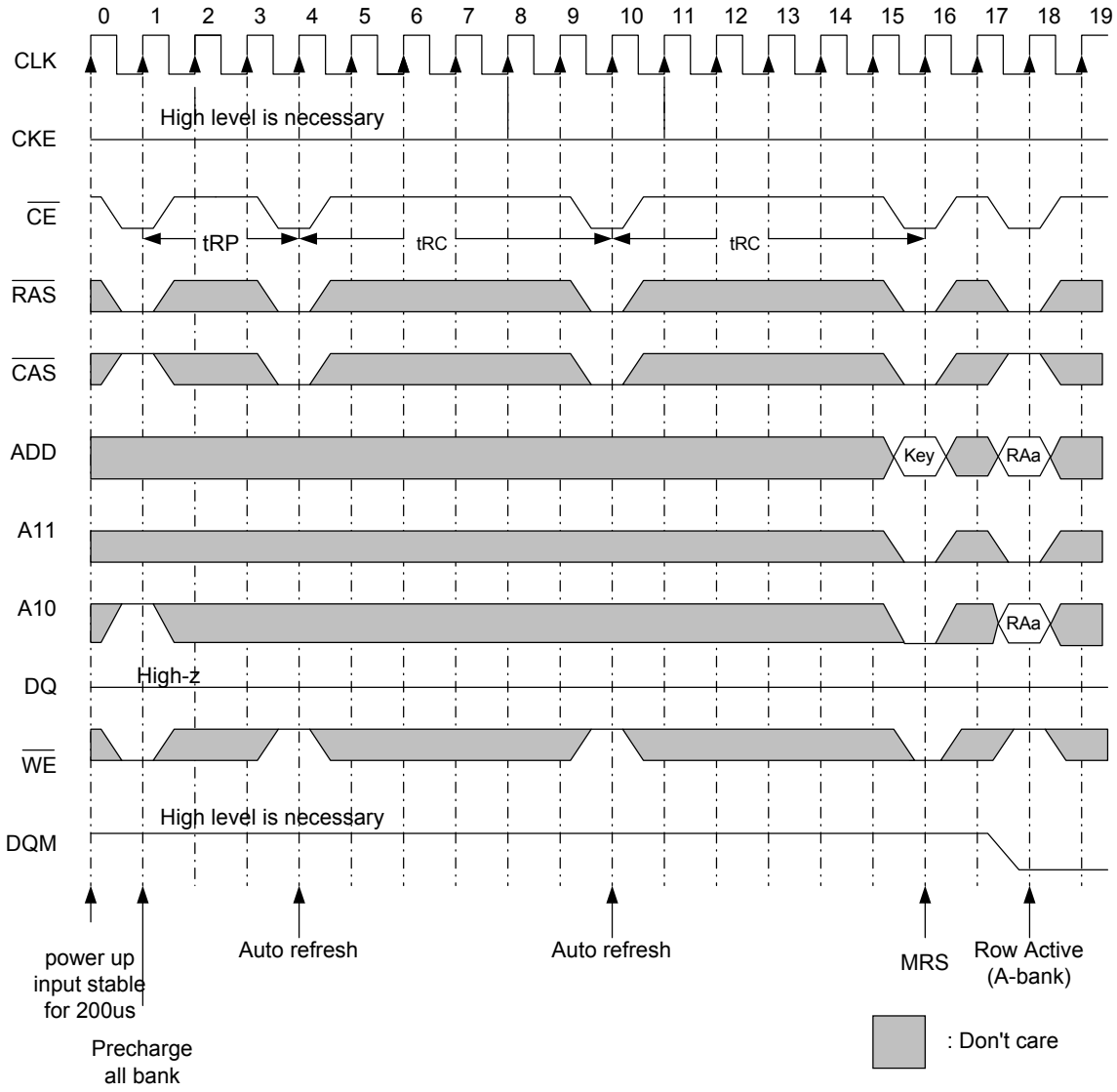
FREQUENCY	CL	t_{RC}	t_{RAS}	t_{RP}	t_{RCD}
125MHZ(8ns)	3	9	6	3	3
100MHZ(10ns)	3	7	5	2	2
83MHZ(12ns)	2	6	4	2	2

UT52L1616-10

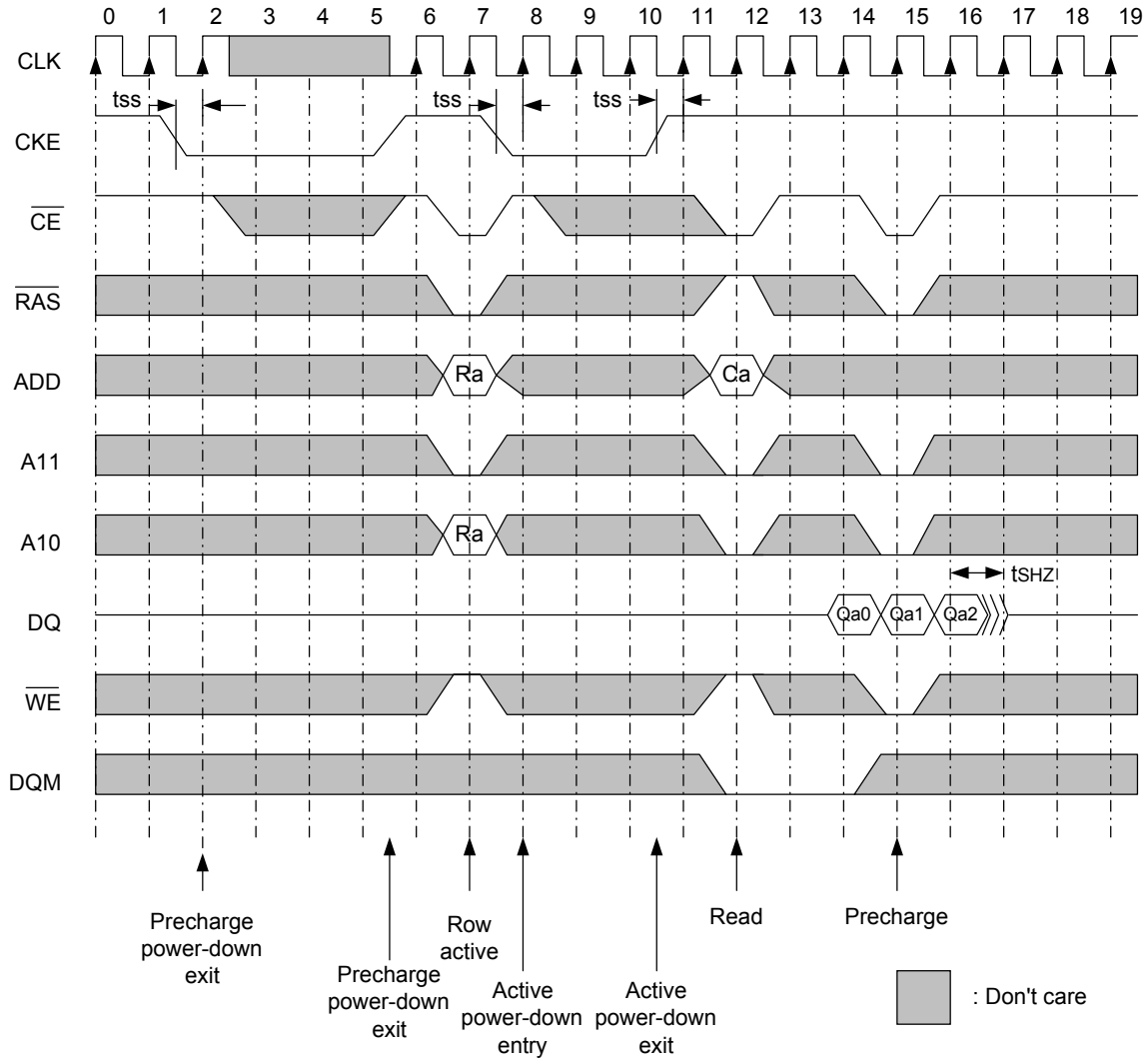
FREQUENCY	CL	t_{RC}	t_{RAS}	t_{RP}	t_{RCD}
125MHZ(8ns)	3	9	6	3	3
100MHZ(10ns)	3	7	5	2	2
83MHZ(12ns)	2	6	4	2	2

TIMEING WAVEFORM

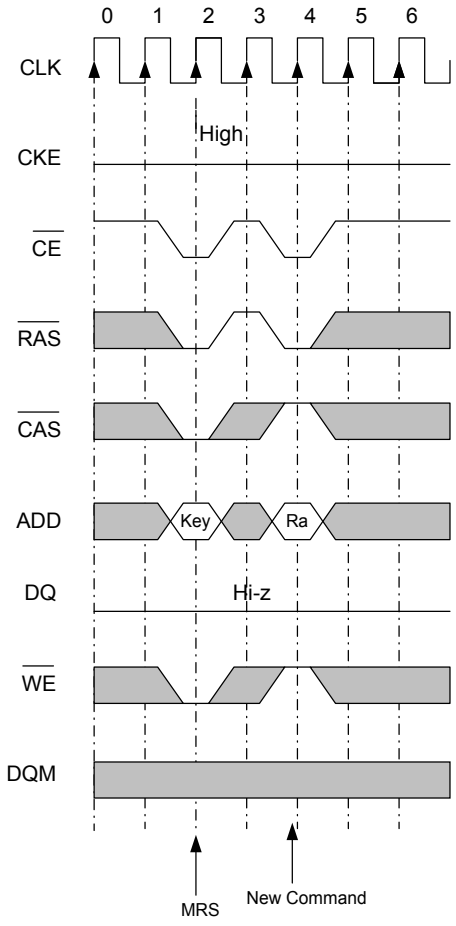
Power Up Initialization Sequence



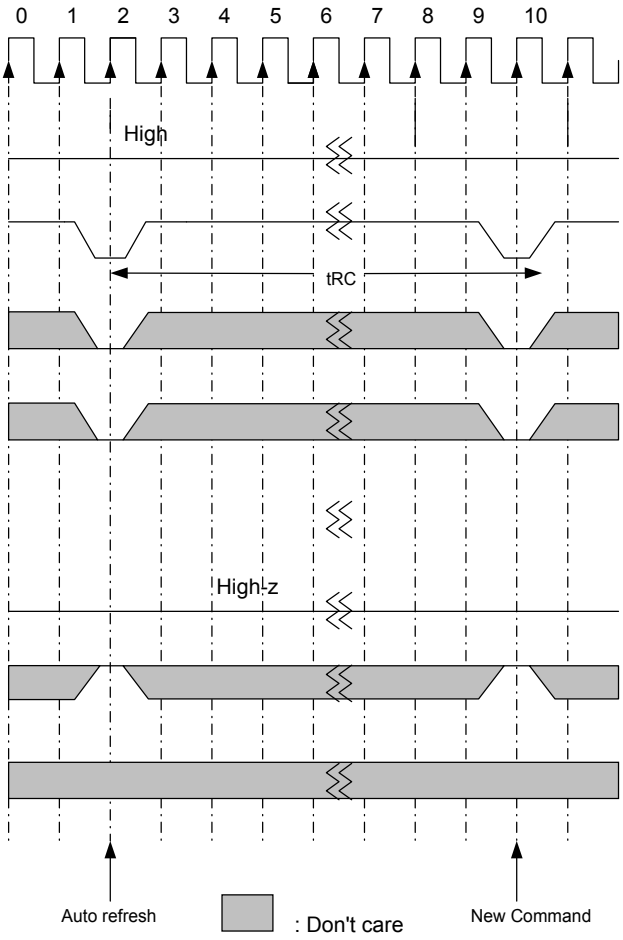
Active / Prechange Power Down Mode (CL=2 , BL=4)



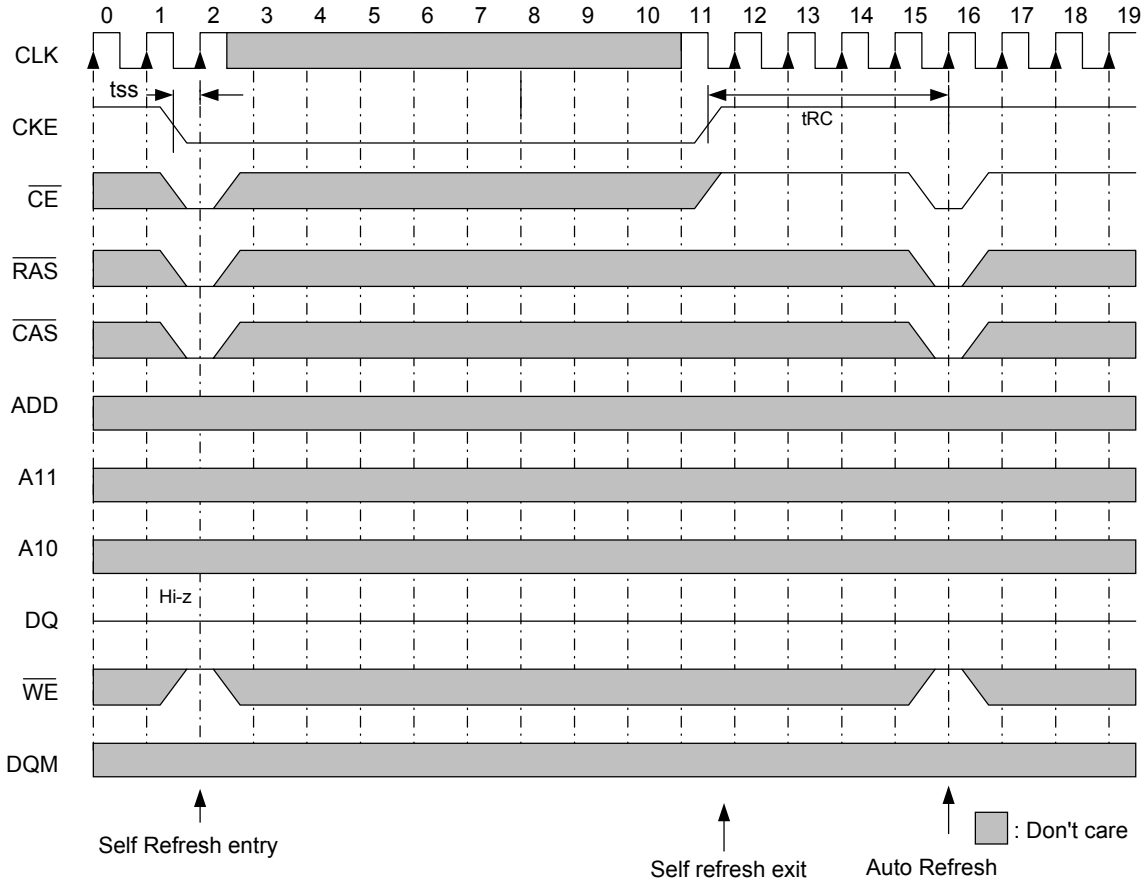
Mode Register Set Cycle



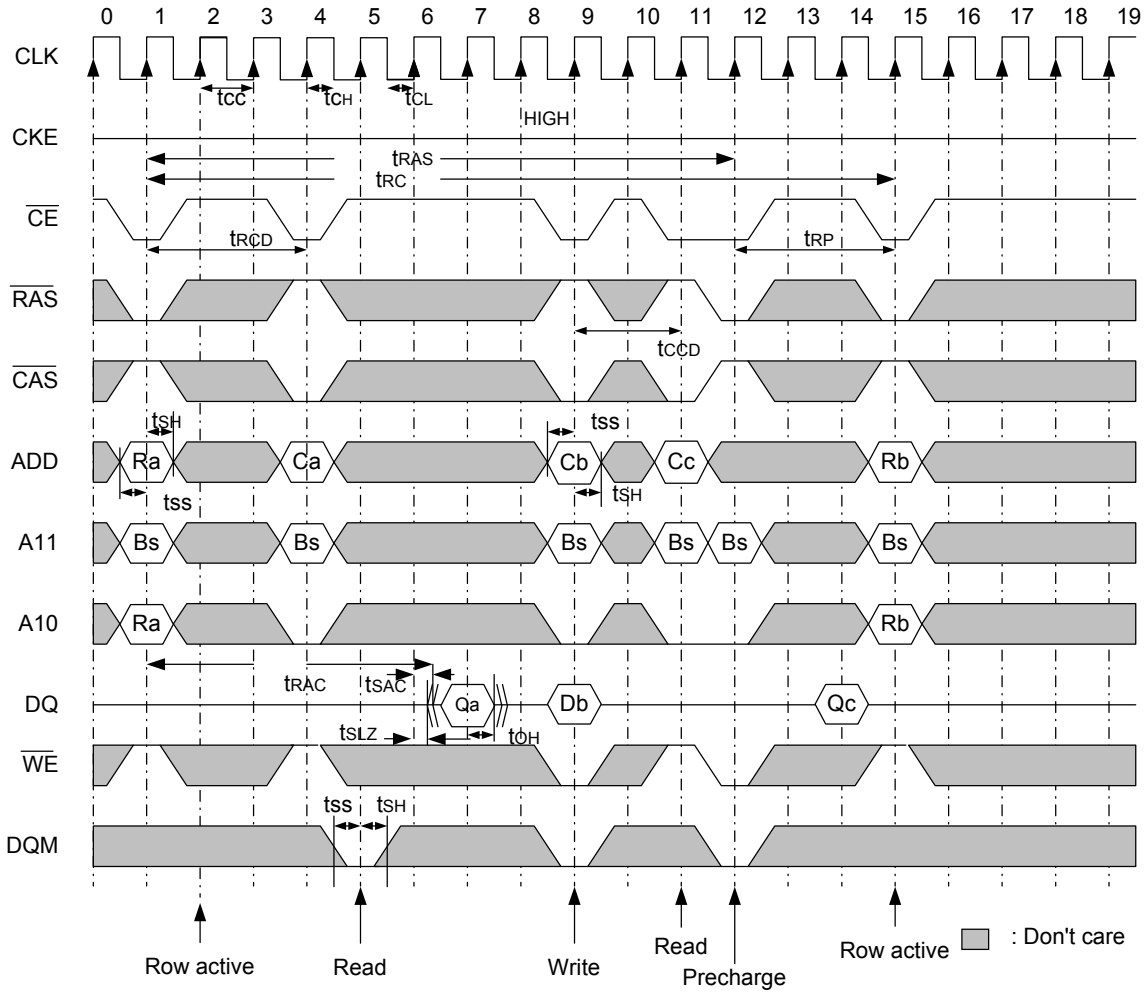
Auto Refresh Cycle



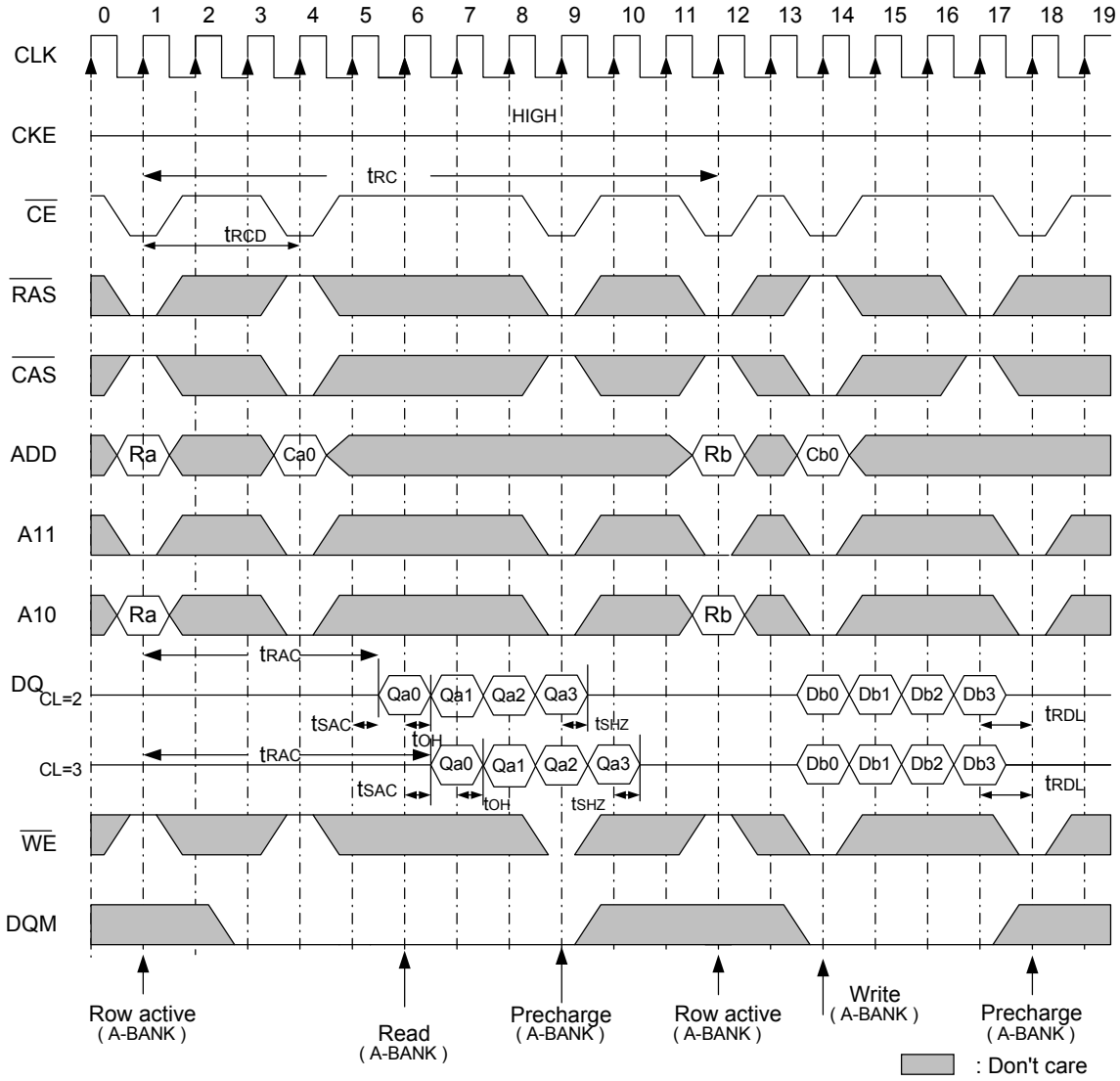
Self Refresh Entry & Exit Cycle



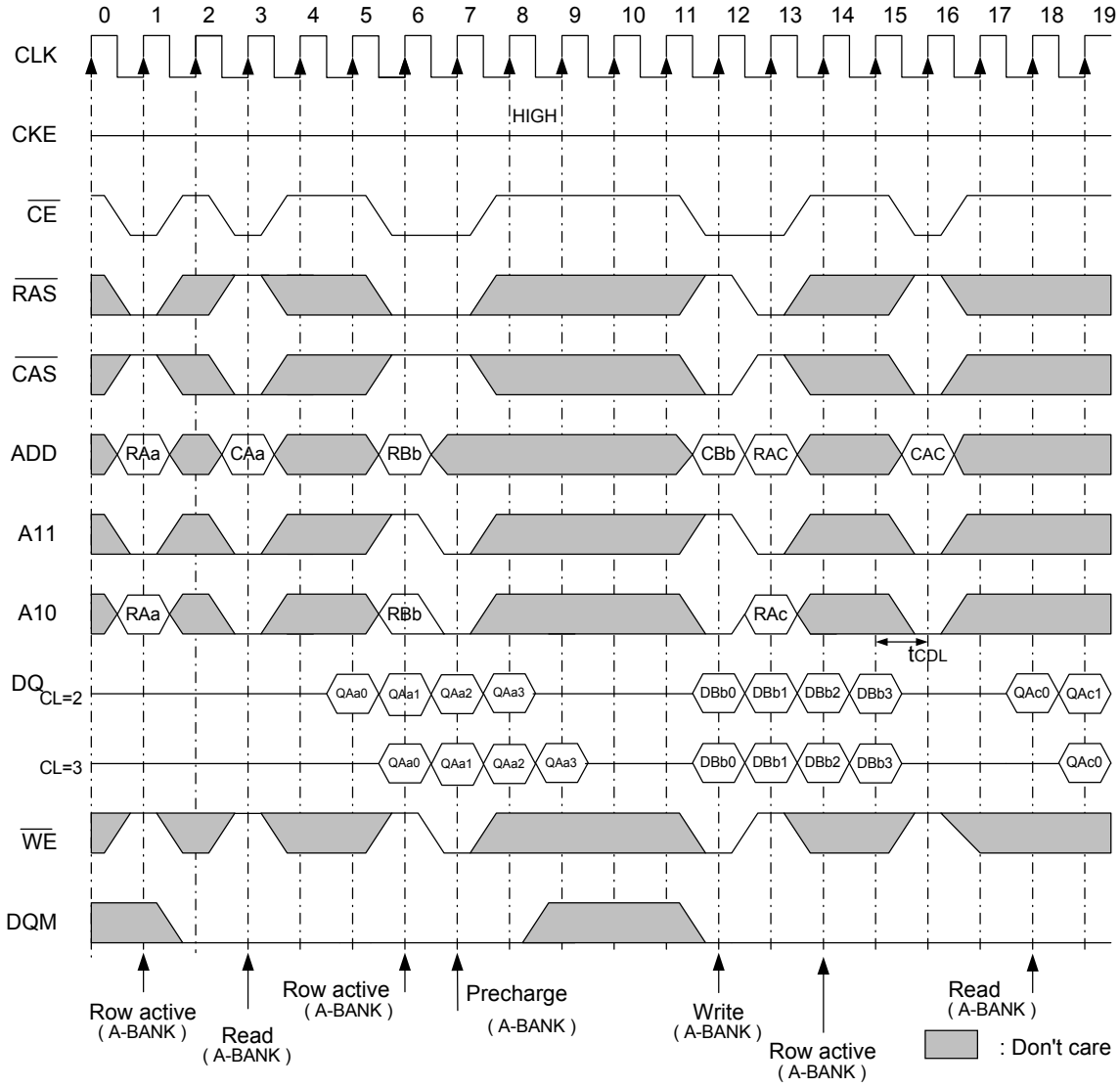
Single Bit Read-Write-Read Cycle At Same Page (CL=3 , BL=1)



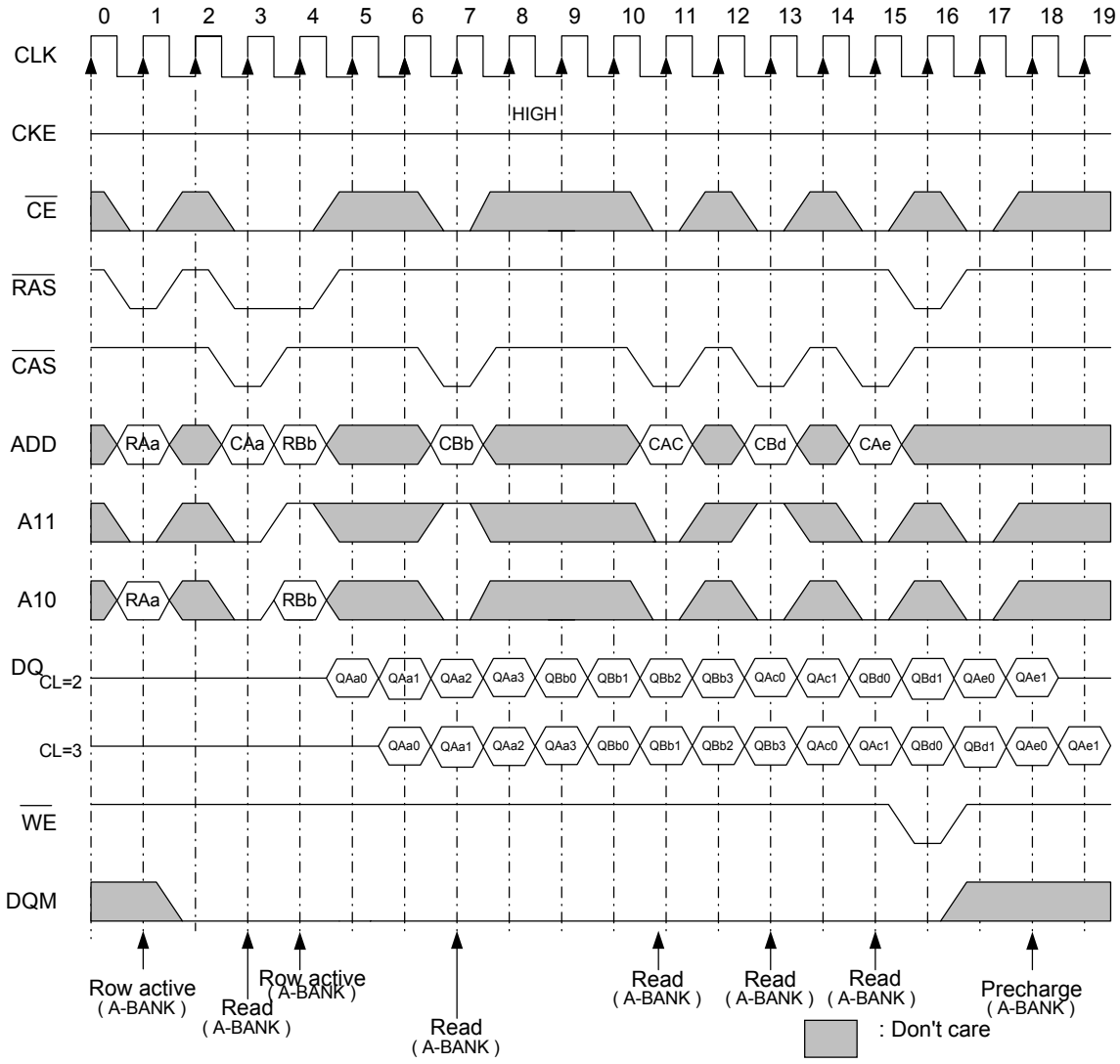
Read & Write Cycle At Same Bank (BL=4)



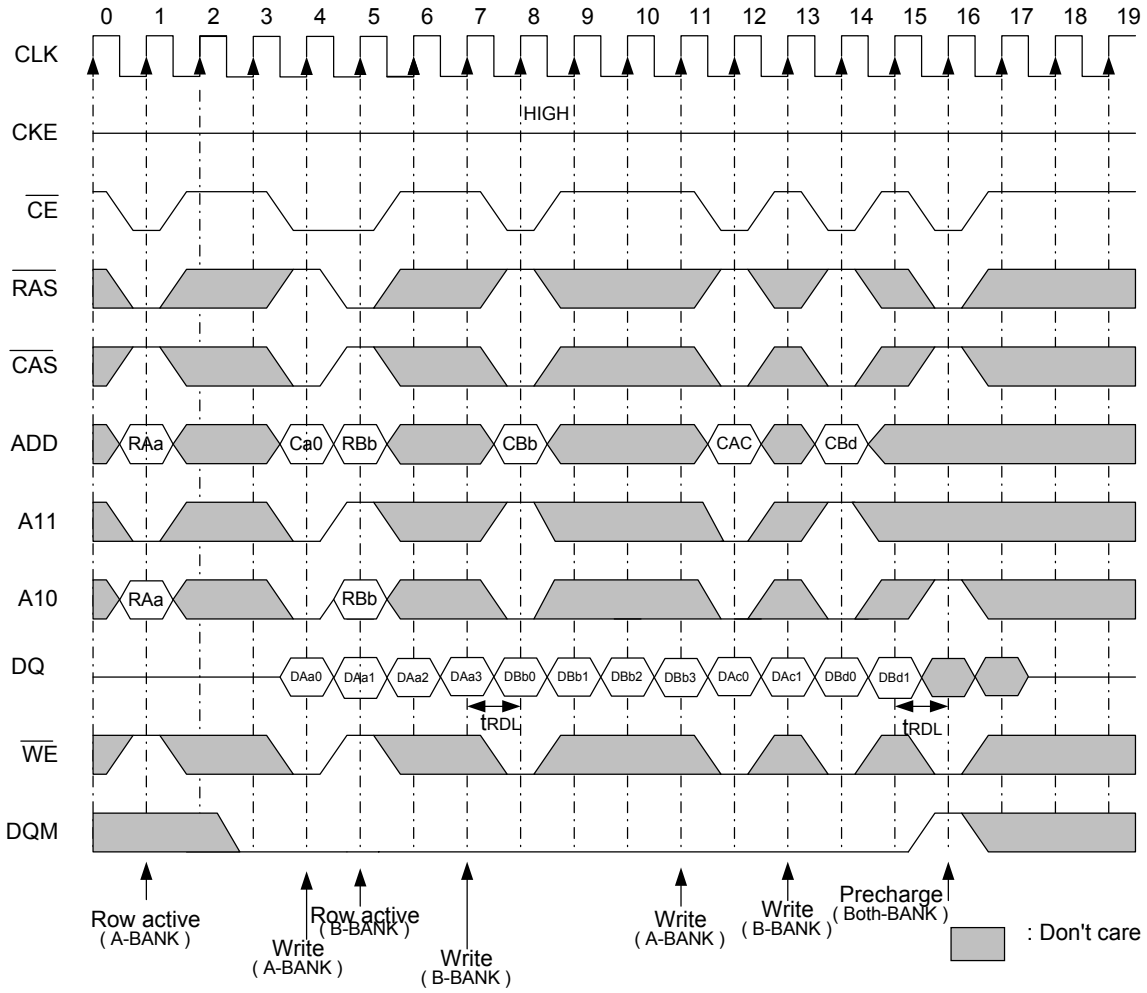
Read & Write Cycle With Random Row At Different Bank (BL=4)



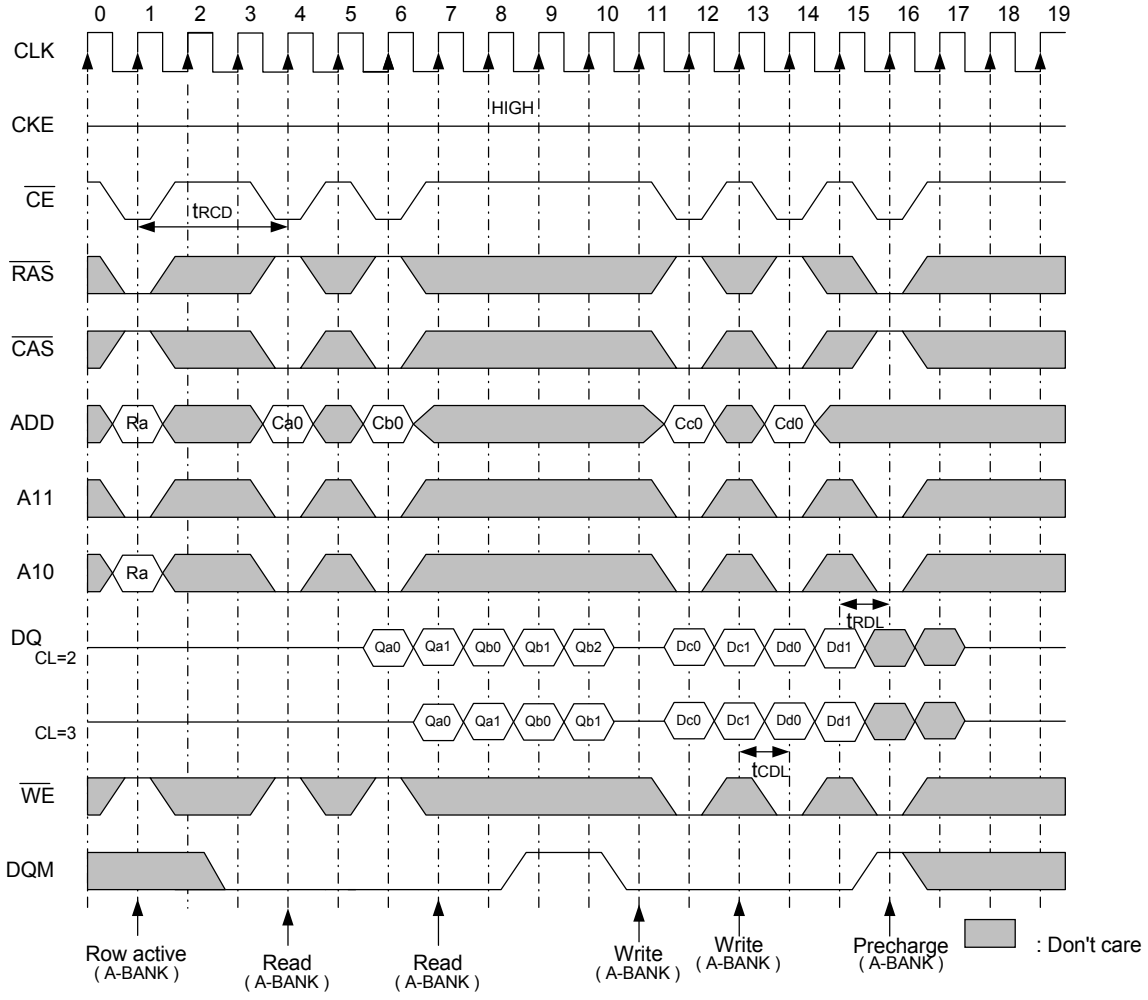
Page Read Cycle At Different Bank (BL=4)



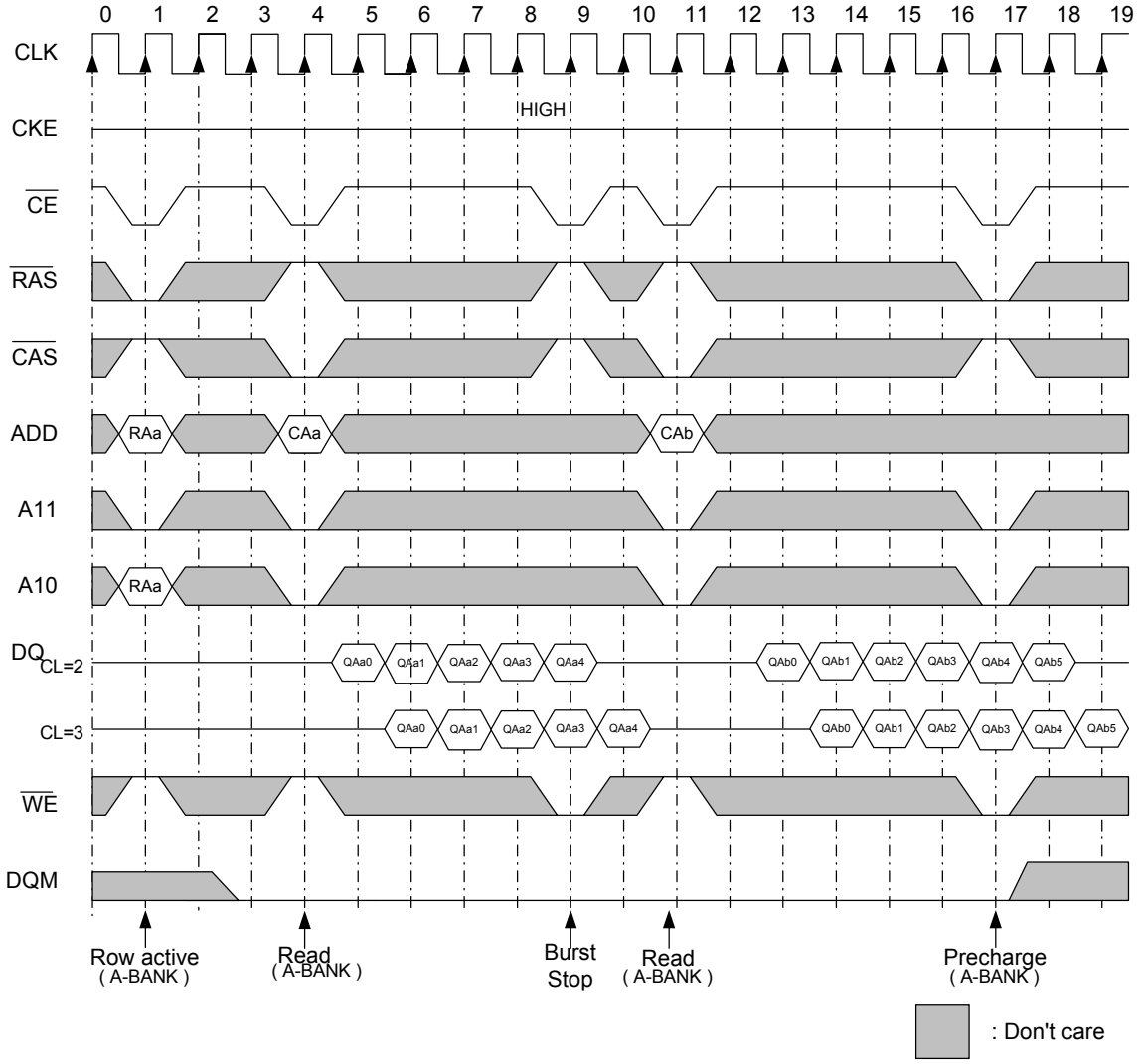
Page Write Cycle At Different Bank (BL=4)



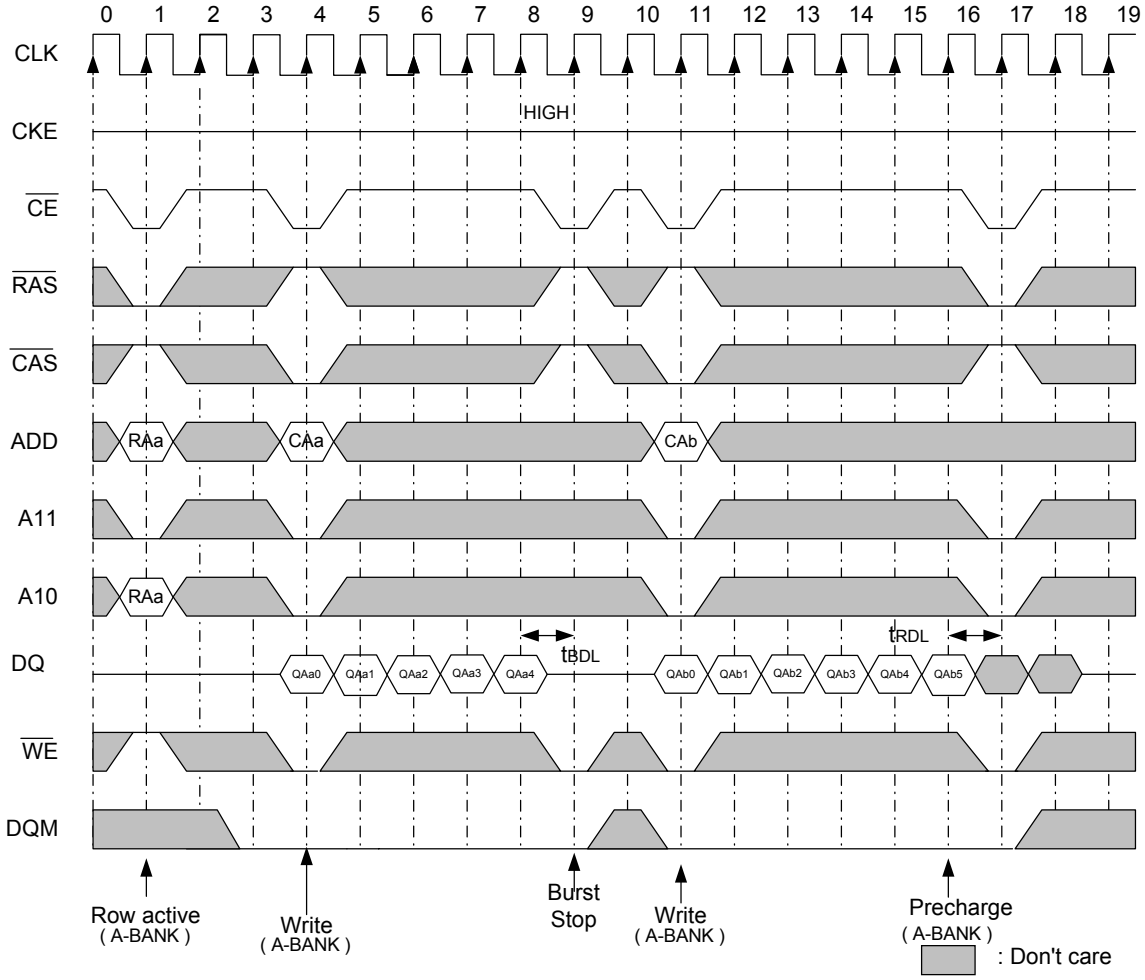
Page Read & Write Cycle At Same Bank (CL=2 , BL=4)



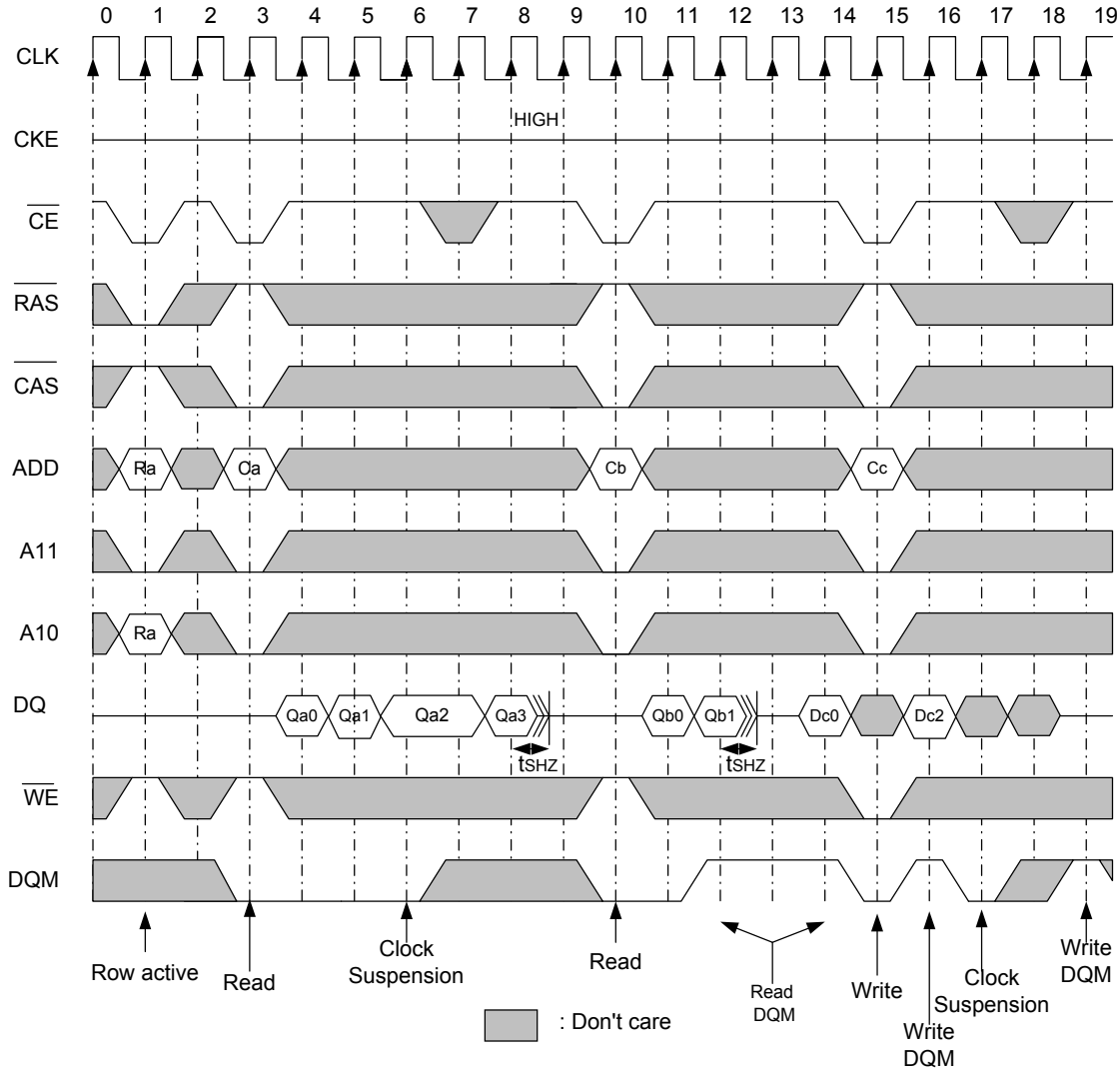
Read Interruption By Precharge Command & Read Burst Stop Cycle (BL= Full Page)



Write Interruption By Precharge Command & Read Burst Stop Cycle (BL= Full Page)

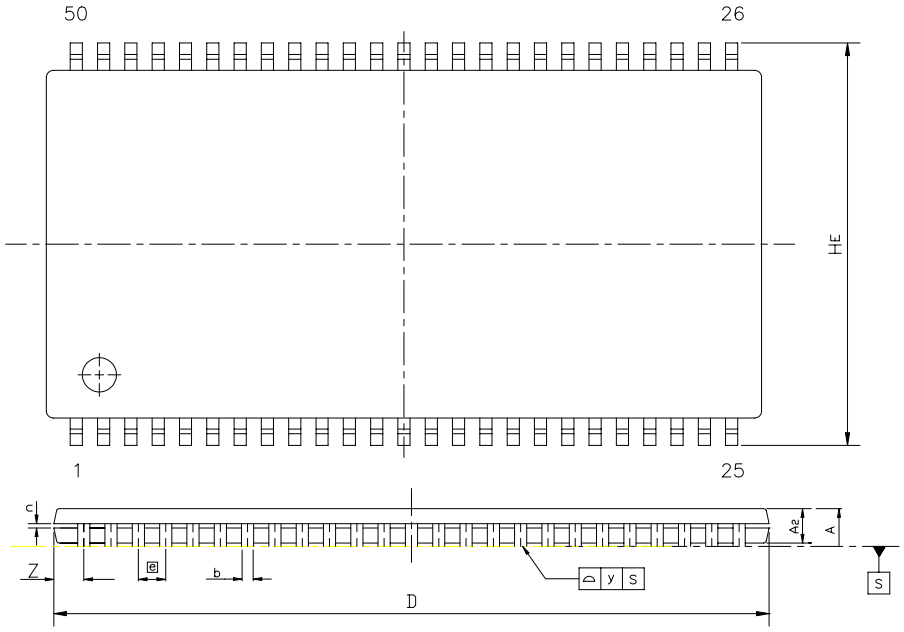


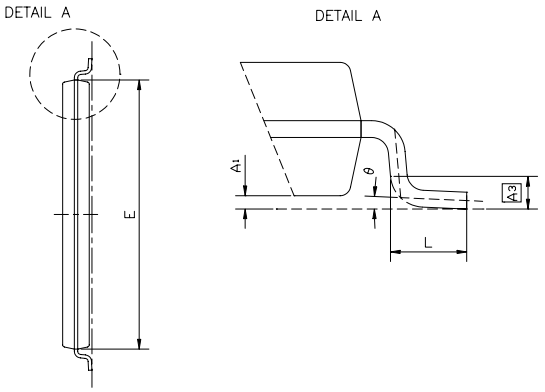
Clock Suspension & DQM Operation Cycle (CL=2 , BL=4)



PACKAGE OUTLINE DIMENTION

50 pin 400mil Package Outline Dimention





SYMBOL	Dimension(inch)			Dimension(mm)		
	Min.	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A1	0.002	0.004	0.006	0.05	0.10	0.15
A2	0.037	0.040	0.042	0.95	1.00	1.05
A3	-	0.010	-	-	0.025	-
b	0.012	0.014	0.017	0.30	0.36	0.42
c	0.004	0.005	0.006	0.11	0.13	0.15
D	0.820	0.825	0.830	20.82	20.95	21.08
E	0.395	0.400	0.405	10.03	10.16	10.29
e	-	0.032	-	-	0.80	-
He	0.455	0.463	0.471	11.56	11.76	11.96
L	0.016	0.020	0.024	0.40	0.50	0.60
y	-	-	0.004	-	-	0.10
Z	-	-	0.040	-	-	1.0
Θ	0°	-	5°	0°	-	5°

NOTE:

1.

DESCRIPTION / DIMENSION	INNERLEAD FLASH	MOLD FLASH	MOLD MISMATCH	MOLD PROTRUSION	TIE BAR BURRS	GATE REMAINDER	DAMBAR PROTRUSION/INTRUSION
D	—	X	O	—	X	X	—
Dmax	—	O	O	—	O	X	—
E	X	X	O	—	—	—	—
Zmax	—	O	O	O	O	O	—
b1	—	—	—	—	—	—	X

O –> INCLUDE X –> EXCLUDE —— –> UNNECESSARY

2. GENERAL APPEARANCE SPEC. SHOULD BE BASED ON FINAL VISUAL INSPECTION SPEC.

ORDERING INFORMATION

PART NO.	ACCESS TIME	PACKAGE
UT52L1616MC-7	5.5 ns	50 PIN TSOP II
UT52L1616MC-8	6 ns	50 PIN TSOP II
UT52L1616MC-10	7 ns	50 PIN TSOP II

REVISION HISTORY

REVISION	DESCRIPTION	DATE
Preliminary Rev.0.9	Original.	Feb 12, 2001
Preliminary Rev.0.91	A new version.	Dec. 13, 2001

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