UTRON

UT61L512

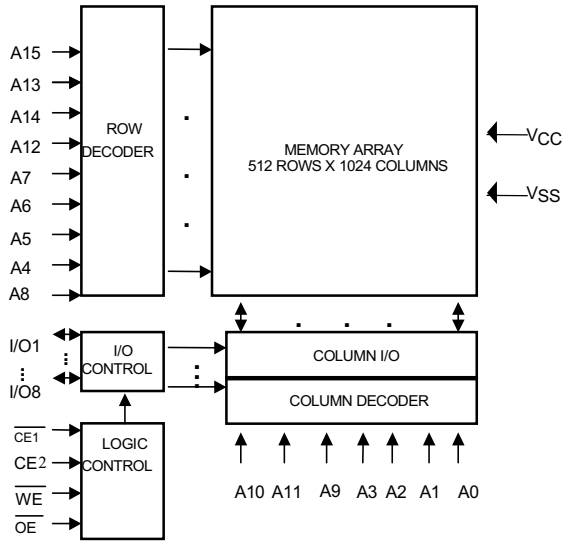
Rev 1.2

64K X 8 BIT HIGH SPEED CMOS SRAM

FEATURES

- Fast access time : 10/12/15 ns (max.)
- Low operating power consumption : 60 mA (typical)
- Single 3.3V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Package : 32-pin 300 mil SOJ
  32-pin 8mmx20mm TSOP-I

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A15	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
$\overline{CE1}$,CE2	Chip Enable 1, 2 Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

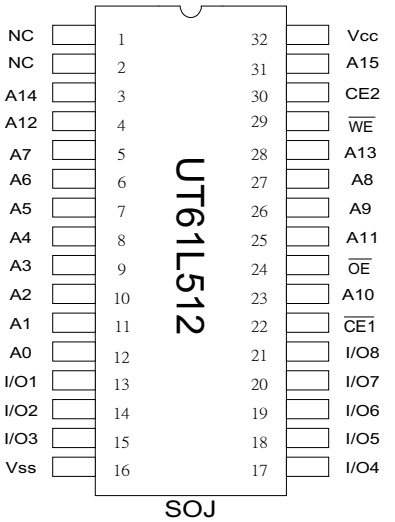
GENERAL DESCRIPTION

The UT61L512 is a 524,288-bit high-speed CMOS static random access memory organized as 524,288 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

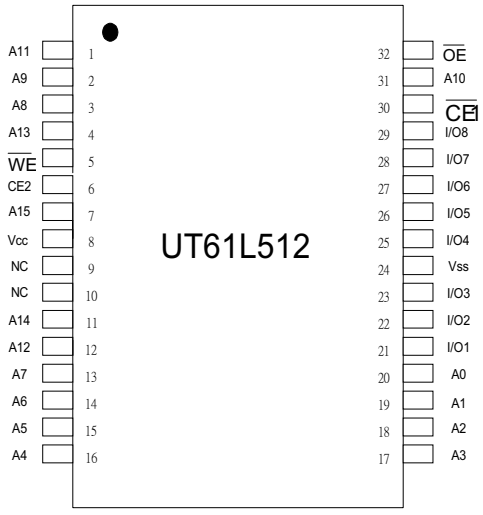
The UT61L512 is designed for high-speed system applications. It is particularly suited for use in high-density high-speed system applications.

The UT61L512 operates from a single 3.3V power supply and all inputs and outputs are fully TTL compatible.

PIN CONFIGURATION



SOJ



TSOP-I

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ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to Vss	V_{TERM}	-0.5 to +7.0	V
Operating Temperature	T_A	0 to +70	℃
Storage Temperature	T_{STG}	-65 to +150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA
Soldering Temperature (under 10 sec)	Tsolder	260	℃

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High - Z	I_{SB},I_{SB1}
Standby	X	L	X	X	High -Z	I_{SB},I_{SB1}
Output Disable	L	H	H	H	High - Z	I_{CC}
Read	L	H	L	H	D_{OUT}	I_{CC}
Write	L	H	X	L	D_{IN}	I_{CC}

Note: H = V_{IH}, L=V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS (V_{CC} =3.1V~3.6V, T_A = 0℃ to 70℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	MAX.	UNIT
Input High Voltage	V_{IH}			2.2	V_{CC}+0.5	V
Input Low Voltage	V_{IL}			- 0.5	0.8	V
Input Leakage Current	I_{LI}	$V_{SS} \leqq V_{IN} \leqq V_{CC}$		- 1	1	μA
Output Leakage Current	I_{LO}	$V_{SS} \leqq V_{I/O} \leqq V_{CC}$ $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}		- 1	1	μA
Output High Voltage	V_{OH}	I_{OH} = - 4mA		2.4	-	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA		-	0.4	V
Operating Power Supply Current	I_{CC}	$\overline{CE1}$ = V_{IL} , CE2 = V_{IH} $I_{I/O}$ = 0mA , Cycle=Min.	- 10	-	180	mA
			- 12	-	160	mA
			- 15	-	140	mA
Standby Power Supply Current	I_{SB}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}		-	30	mA
	I_{SB1}	$\overline{CE1} \geqq V_{CC}$-0.2V or CE2 $\leqq$ 0.2V		-	5	mA

CAPACITANCE (T_A=25℃, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.3.3V
Output Load	C_L=30pF, I_{OH}/I_{OL}=-4mA/8mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.1V~3.6V , T_A = 0℃ to 70℃)

(1) READ CYCLE

PARAMETER	SYMBOL	UT61L512-10		UT61L512-12		UT61L512-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	10	-	12	-	15	-	ns
Address Access Time	t_{AA}	-	10	-	12	-	15	ns
Chip Enable Access Time	t_{ACE1}, t_{ACE1}	-	10	-	12	-	15	ns
Output Enable Access Time	t_{OE}	-	5	-	6	-	7	ns
Chip Enable to Output in Low Z	t_{CLZ1*}, t_{CLZ2*}	2	-	3	-	4	-	ns
Output Enable to Output in Low Z	t_{OLZ*}	0	-	0	-	0	-	ns
Chip Disable to Output in High Z	t_{CHZ1*}, t_{CHZ2*}	-	5	-	6	-	7	ns
Output Disable to Output in High Z	t_{OHZ*}	-	5	-	6	-	7	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns

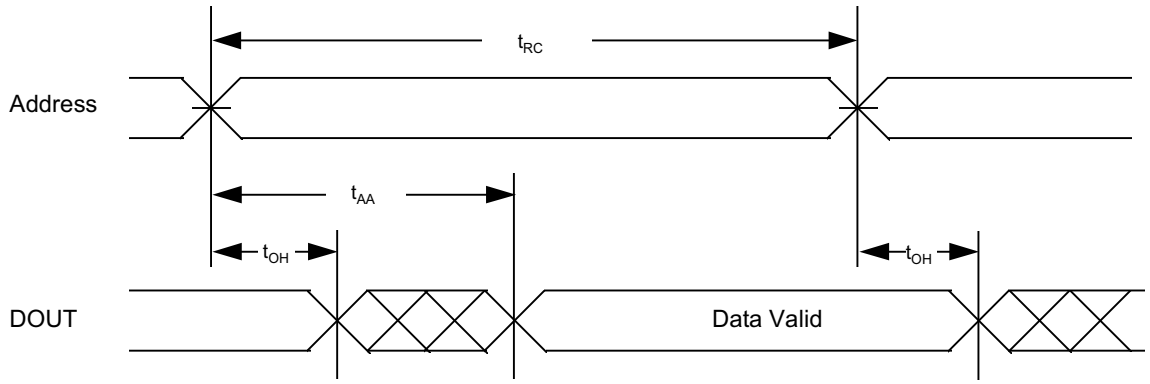
(2) WRITE CYCLE

PARAMETER	SYMBOL	UT61L512-10		UT61L512-12		UT61L512-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	10	-	12	-	15	-	ns
Address Valid to End of Write	t_{AW}	8	-	10	-	12	-	ns
Chip Enable to End of Write	t_{CW1}, t_{CW2}	8	-	10	-	12	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	8	-	9	-	10	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	6	-	7	-	8	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW*}	2	-	3	-	4	-	ns
Write to Output in High Z	t_{WHZ*}	-	6	-	7	-	8	ns

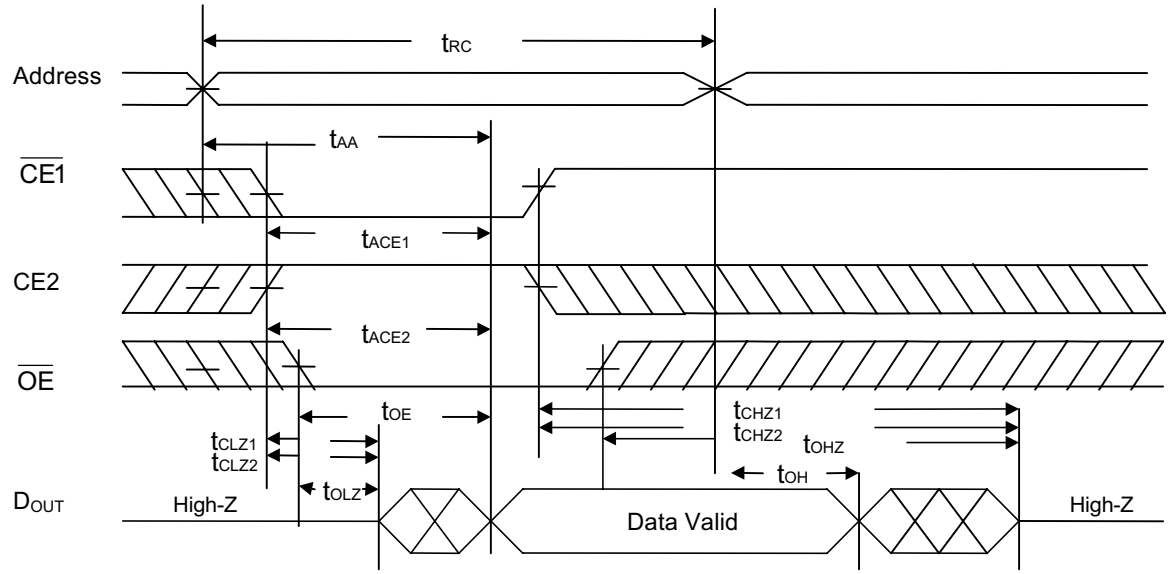
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)



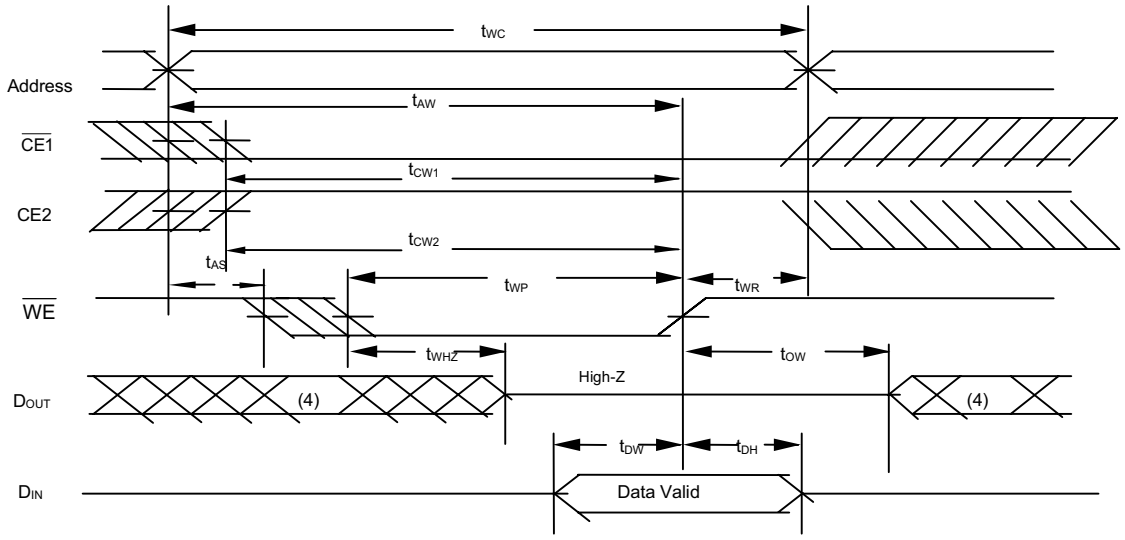
READ CYCLE 2 ($\overline{CE1}$, CE2 and $\overline{OE}$ Controlled) (1,3,5,6)



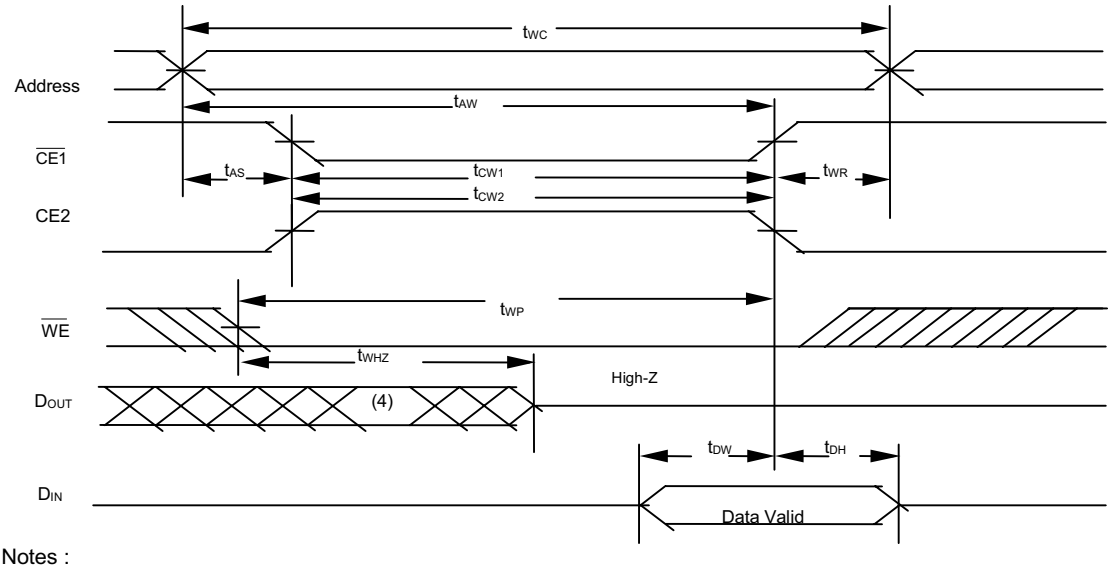
Notes :

1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected $\overline{CE1}$=V_{IL} and CE2=V_{IH}.
3. Address must be valid prior to or coincident with $\overline{CE1}$ and CE2 transition; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is low.
5. t_{CLZ1}, t_{CLZ2}, t_{OLZ}, t_{CHZ1}, t_{CHZ2} and t_{OHZ} are specified with C_L=5pF. Transition is measured ± 500mV from steady state.
6. At any given temperature and voltage condition, t_{CHZ1} is less than t_{CLZ1}, t_{CHZ2} is less than t_{CLZ2}, t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 ($\overline{WE}$ Controlled) (1,2,3,5)



WRITE CYCLE 2 ($\overline{CE1}$ and CE2 Controlled) (1,2,5)

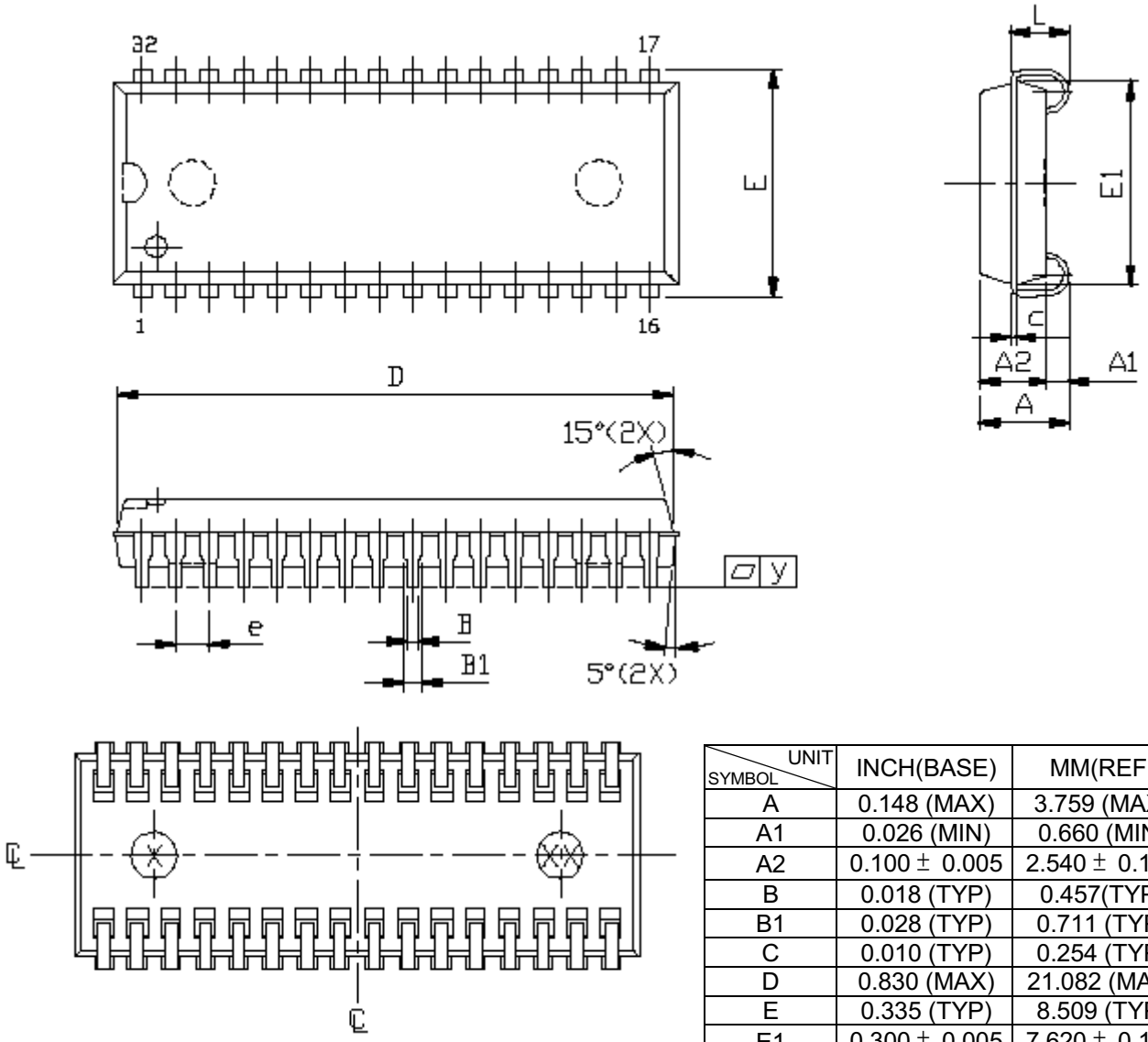


Notes :

1. $\overline{WE}$ or $\overline{CE1}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a low $\overline{CE1}$ and a low $\overline{WE}$.
3. During a $\overline{WE}$ controlled with write cycle with $\overline{OE}$ LOW, t_{WP} must be greater than $t_{WHZ}+t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input singals must not be applied.
5. If the $\overline{CE1}$ LOW transition occurs simultaneously with or after $\overline{WE}$ LOW transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ± 500mV from steady state.

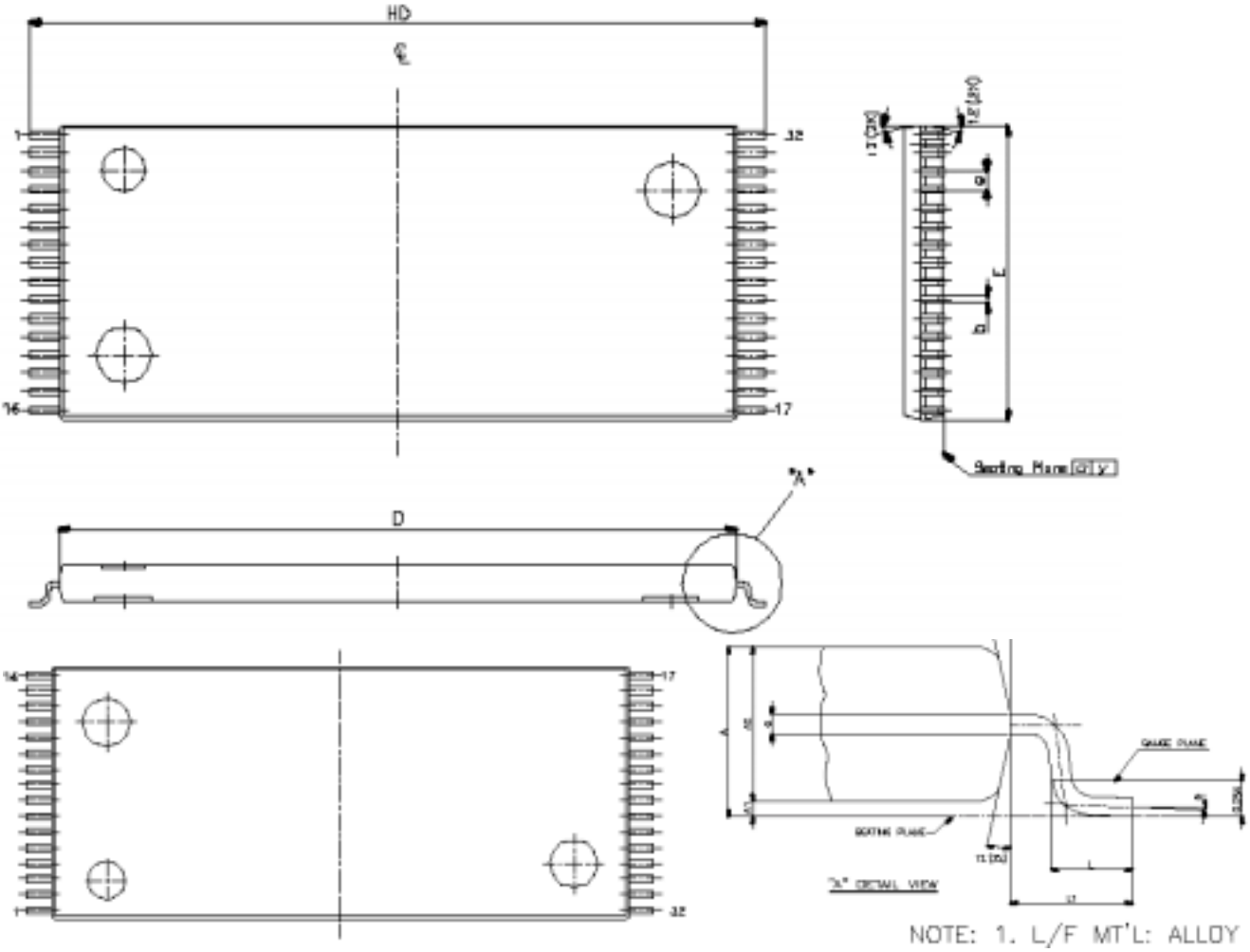
PACKAGE OUTLINE DIMENSION

32PIN SOJ Package Outline Dimension



UNIT / SYMBOL	INCH(BASE)	MM(REF)
A	0.148 (MAX)	3.759 (MAX)
A1	0.026 (MIN)	0.660 (MIN)
A2	0.100 ± 0.005	2.540 ± 0.127
B	0.018 (TYP)	0.457(TYP)
B1	0.028 (TYP)	0.711 (TYP)
C	0.010 (TYP)	0.254 (TYP)
D	0.830 (MAX)	21.082 (MAX)
E	0.335 (TYP)	8.509 (TYP)
E1	0.300 ± 0.005	7.620 ± 0.127
e	0.050 (TYP)	1.270 (TYP)
L	0.086 ± 0.010	2.184 ± 0.254
y	0.003 (MAX)	0.076 (MAX)

32PIN TSOP-I Package Outline Dimension



SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004 ± 0.002	0.10 ± 0.05
A2	0.039 ± 0.002	1.00 ± 0.05
b	0.008 + 0.002 - 0.001	0.20 + 0.05 -0.03
c	0.005 (TYP)	0.127 (TYP)
D	0.724 ± 0.004	18.40 ± 0.10
E	0.315 ± 0.004	8.00 ± 0.10
e	0.020 (TYP)	0.50 (TYP)
HD	0.787 ± 0.008	20.00 ± 0.20
L	0.0197 ± 0.004	0.50 ± 0.10
L1	0.0315 ± 0.004	0.08 ± 0.10
y	0.003 (MAX)	0.076 (MAX)
θ	0°～5°	0°～5°

ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	PACKAGE
UT61L512JC-10	10	32PIN SOJ
UT61L512JC-12	12	32PIN SOJ
UT61L512JC-15	15	32PIN SOJ
UT61L512LC-10	10	32PIN TSOP-I
UT61L512LC-12	12	32PIN TSOP-I
UT61L512LC-15	15	32PIN TSOP-I

REVISION HISTORY

REVISION	DESCRIPTION	DATE
REV. 1.0	Original.	AUG. 24,1999
REV 1.1	Revise “WRITE CYCLE”	OCT. 18,1999
REV. 1.2	The symbols CE1#,OE# and WE# are revised as $\overline{CE1}$, $\overline{OE}$ and $\overline{WE}$.	MAY. 25,2001

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