FEATURES

- Access time : 55/70/100 ns
- CMOS Low operating power
  Operating : 45/35/25mA (max.)
  Standby : 20μA (typ.) L-version
  3μA (typ.) LL-version
- Single 2.7V~3.6V power supply
- Industrial Temperature : -40℃~85℃
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Data retention voltage : 1.5V (min)
- Package : 32-pin 450 mil SOP
  32-pin 8mm×20mm TSOP-I
  32-pin 8mm×13.4mm STSOP
  36-pin 6mm×8mm TFBGA

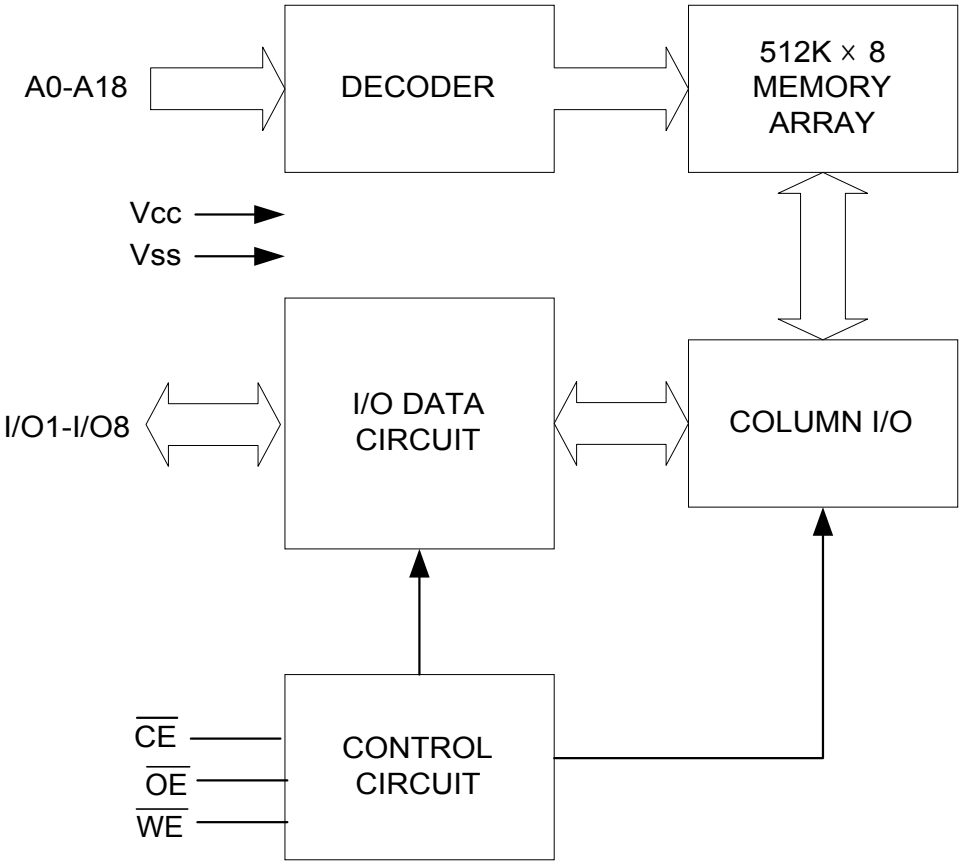
GENERAL DESCRIPTION

The UT62L5128 is a 4,194,304-bit low power CMOS static random access memory organized as 524,288 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

The UT62L5128 operates from a wide range 2.7V~3.6V power supply and all inputs and outputs are fully TTL compatible.

The UT62L5128 supports industrial operating temperature range, and supports low data retention voltage for battery back-up operation with low data retention current.

FUNCTIONAL BLOCK DIAGRAM



UTRON TECHNOLOGY INC.
1F, No. 11, R&D Rd. II, Science-Based Industrial Park, Hsinchu, Taiwan, R. O. C.
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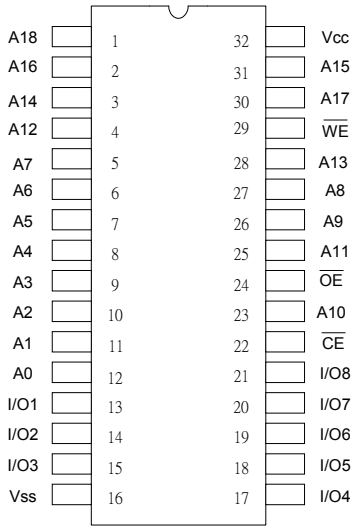
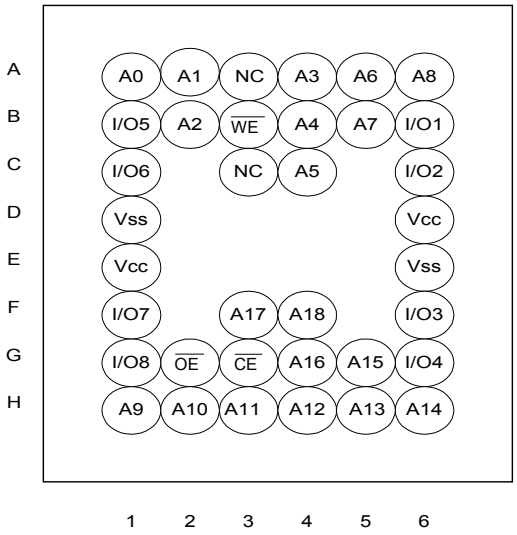
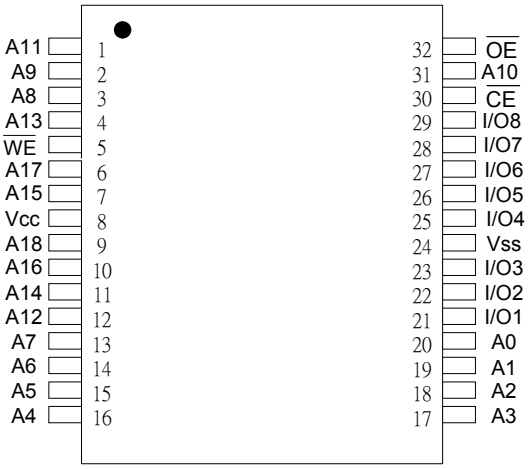
PIN CONFIGURATION



SOP



TFBGA



TSOP-1 / STSOP

PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A18	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS*

PARAMETER		SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V_{SS}		V_{TERM}	-0.5 to 4.6	V
Operating Temperature	Industrial	T_A	-40 to 85	℃
Storage Temperature		T_{STG}	-65 to 150	℃
Power Dissipation		P_D	1	W
DC Output Current		I_{OUT}	50	mA
Soldering Temperature (under 10 secs)		Tsolder	260	℃

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	I/O OPERATION	SUPPLY CURRENT
Standby	X	H	X	High – Z	I_{SB}, I_{SB1}
Output Disable	H	L	H	High – Z	I_{CC} , I_{CC1}, I_{CC2}
Read	H	L	L	D_{OUT}	I_{CC} , I_{CC1}, I_{CC2}
Write	L	L	X	D_{IN}	I_{CC} , I_{CC1}, I_{CC2}

Note: H = V_{IH}, L=V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7V~3.6V, T_A = -40℃ to 85℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Power Voltage	V_{CC}			2.7	3.0	3.6	V
Input High Voltage	V_{IH}			2.0	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}			-0.2	-	0.6	V
Input Leakage Current	I_{LI}	$V_{SS} \leqq V_{IN} \leqq V_{CC}$		- 1	-	1	μA
Output Leakage Current	I_{LO}	$V_{SS} \leqq V_{I/O} \leqq V_{CC;}$ Output Disabled		- 1	-	1	μA
Output High Voltage	V_{OH}	I_{OH}= -1mA		2.2	-	-	V
Output Low Voltage	V_{OL}	I_{OL}= 2.1mA		-	-	0.4	V
Operating Power Supply Current	I_{CC}	Cycle time=min, 100%duty, $I_{I/O}$=0mA, $\overline{CE}$=V_{IL} ;	55	-	30	45	mA
			70	-	25	35	mA
			100	-	20	25	mA
Average Operation Current	I_{CC1}	Cycle time=1μs,100%duty,$I_{I/O}$=0mA, $\overline{CE}$ ≦0.2V,other pins at 0.2V or Vcc-0.2V,		-	4	5	mA
	I_{CC2}	Cycle time=500ns,100%duty,$I_{I/O}$=0mA, $\overline{CE}$ ≦0.2V,other pins at 0.2V or Vcc-0.2V,		-	8	10	mA
Standby Current (TTL)	I_{SB}	$\overline{CE}$=$V_{IH,}$ other pins = V_{IH} or V_{IL} ;		-	0.3	0.5	mA
Standby Current (CMOS)	I_{SB1}	$\overline{CE}$=V_{CC}-0.2V, other pins at 0.2V or Vcc-0.2V,	-L	-	20	80	μA
			-LL	-	3	25	μA

CAPACITANCE (T_A=25℃, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 30pF+1TTL , I_{OH}/I_{OL} = -1mA / 2.1mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7V~3.6V , T_A = -40℃ to 85℃)

(1) READ CYCLE

PARAMETER	SYMBOL	UT62L5128-55		UT62L5128-70		UT62L5128-100		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	55	-	70	-	100	-	ns
Address Access Time	t_{AA}	-	55	-	70	-	100	ns
Chip Enable Access Time	t_{ACE}	-	55	-	70	-	100	ns
Output Enable Access Time	t_{OE}	-	30	-	35	-	50	ns
Chip Enable to Output in Low Z	t_{CLZ*}	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	t_{OLZ*}	5	-	5	-	5	-	ns
Chip Disable to Output in High Z	t_{CHZ*}	-	20	-	25	-	30	ns
Output Disable to Output in High Z	t_{OHZ*}	-	20	-	25	-	30	ns
Output Hold from Address Change	t_{OH}	10	-	10	-	10	-	ns

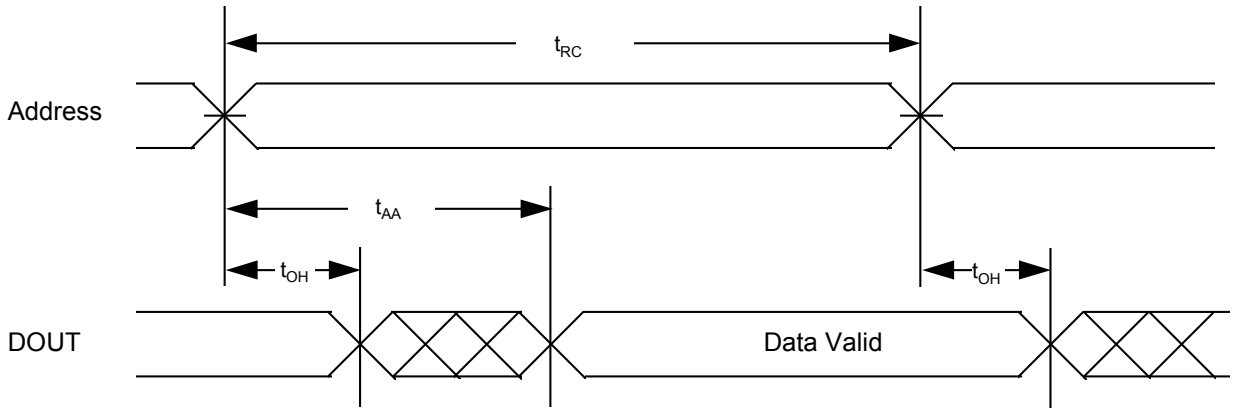
(2) WRITE CYCLE

PARAMETER	SYMBOL	UT62L5128-55		UT62L5128-70		UT62L5128-100		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	55	-	70	-	100	-	ns
Address Valid to End of Write	t_{AW}	50	-	60	-	80	-	ns
Chip Enable to End of Write	t_{CW}	50	-	60	-	80	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	45	-	55	-	70	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	25	-	30	-	40	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW*}	5	-	5	-	5	-	ns
Write to Output in High Z	t_{WHZ*}	-	30	-	30	-	40	ns

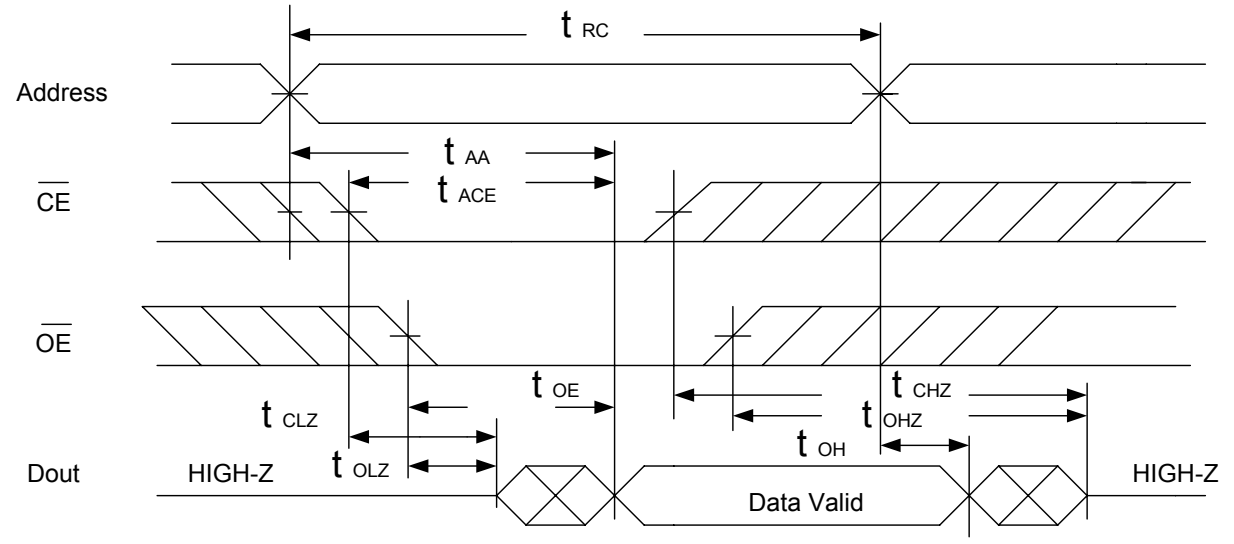
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)



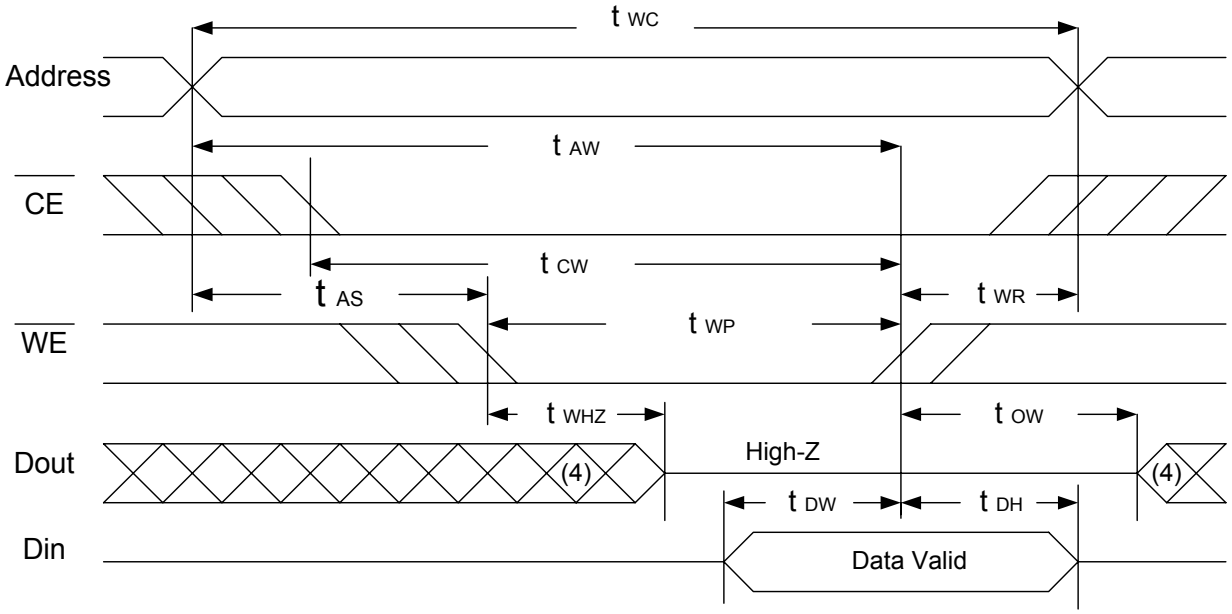
READ CYCLE 2 ($\overline{CE}$ and $\overline{OE}$ Controlled) (1,3,5,6)



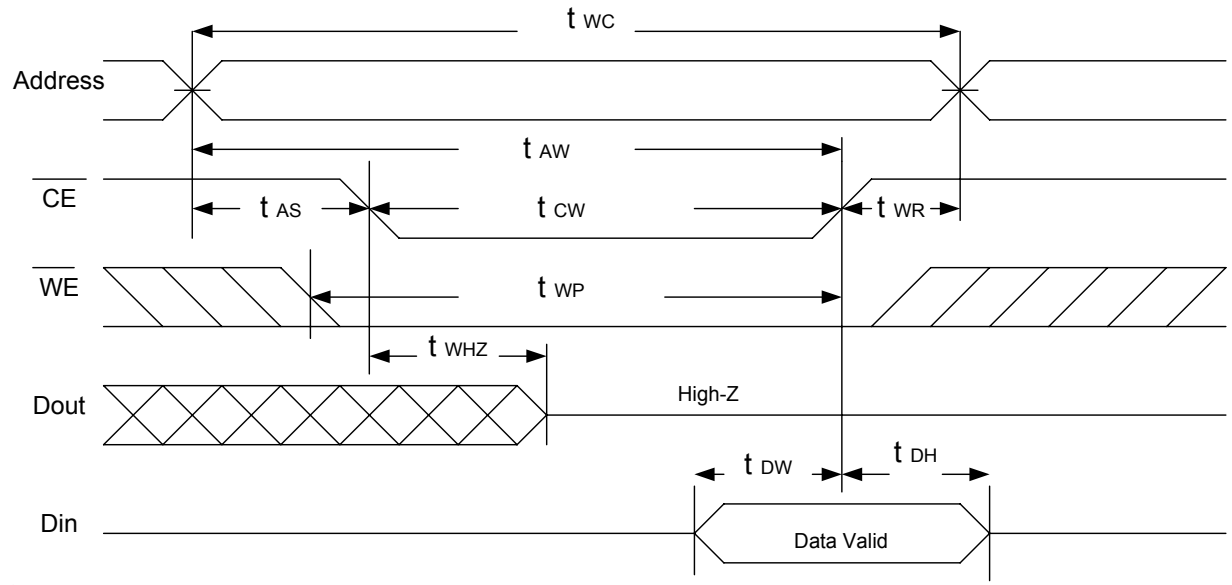
Notes :

1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected $\overline{CE}$ =V_{IL}.
3. Address must be valid prior to or coincident with $\overline{CE}$ transition; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. t_{CLZ}, t_{OLZ}, t_{CHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.
6. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ}, t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 ($\overline{WE}$ Controlled) (1,2,3,5)



WRITE CYCLE 2 ($\overline{CE}$ Controlled) (1,2,5)



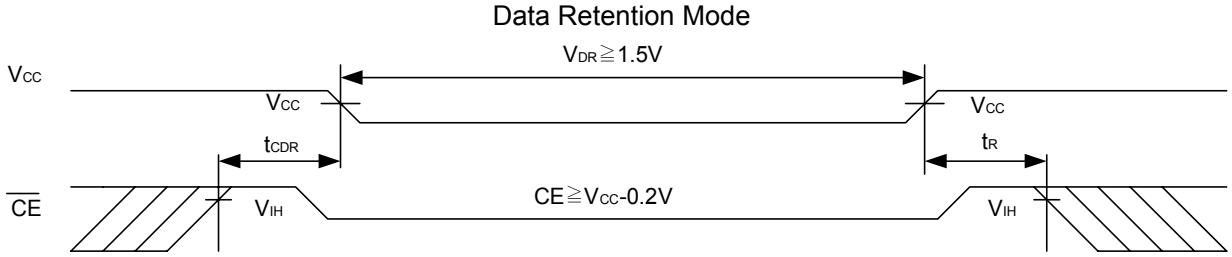
Notes :

1. $\overline{WE}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$.
3. During a $\overline{WE}$ controlled with write cycle with $\overline{OE}$ LOW, t_{WP} must be greater than $t_{WHZ}+t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input singals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

DATA RETENTION CHARACTERISTICS (T_A = -40℃ to 85℃)

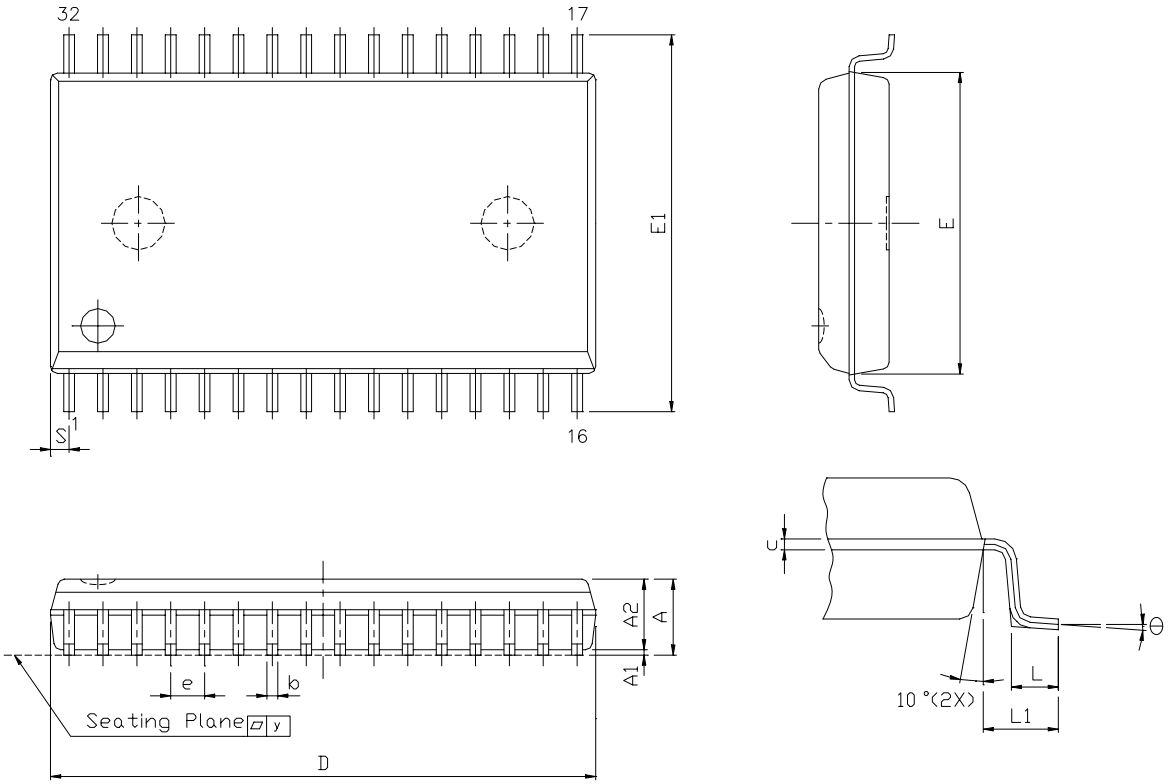
PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V_{DR}	$\overline{CE} \geqq V_{CC}$-0.2V		1.5	-	3.6	V
Data Retention Current	I_{DR}	Vcc=1.5V	- L	-	1	50	µA
		$\overline{CE} \geqq V_{CC}$-0.2V	- LL	-	0.5	20	µA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)		0	-	-	ms
Recovery Time	t_R			5	-	-	ms

DATA RETENTION WAVEFORM ($\overline{CE}$ controlled)



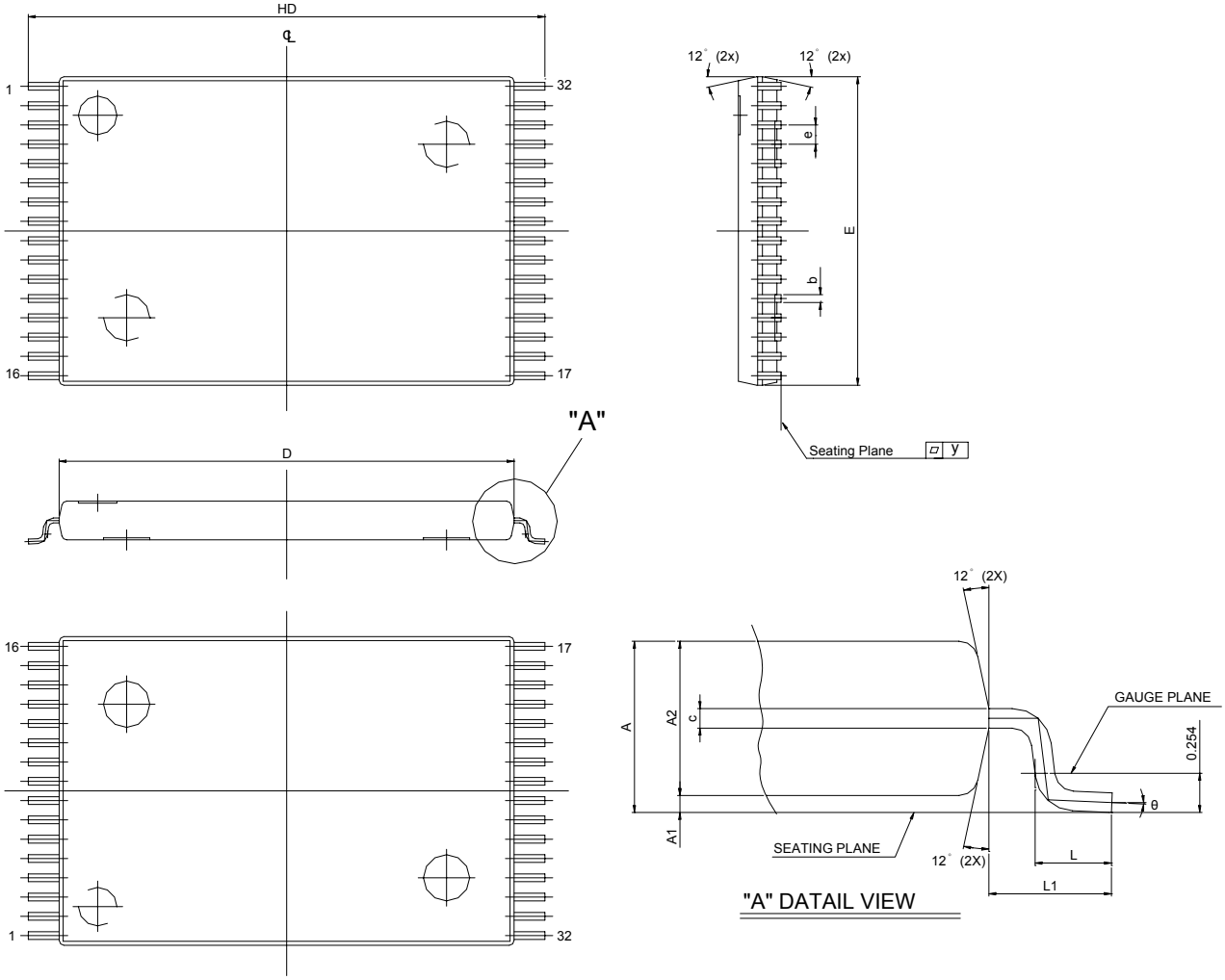
PACKAGE OUTLINE DIMENSION

32 pin 450 mil SOP Package Outline Dimension



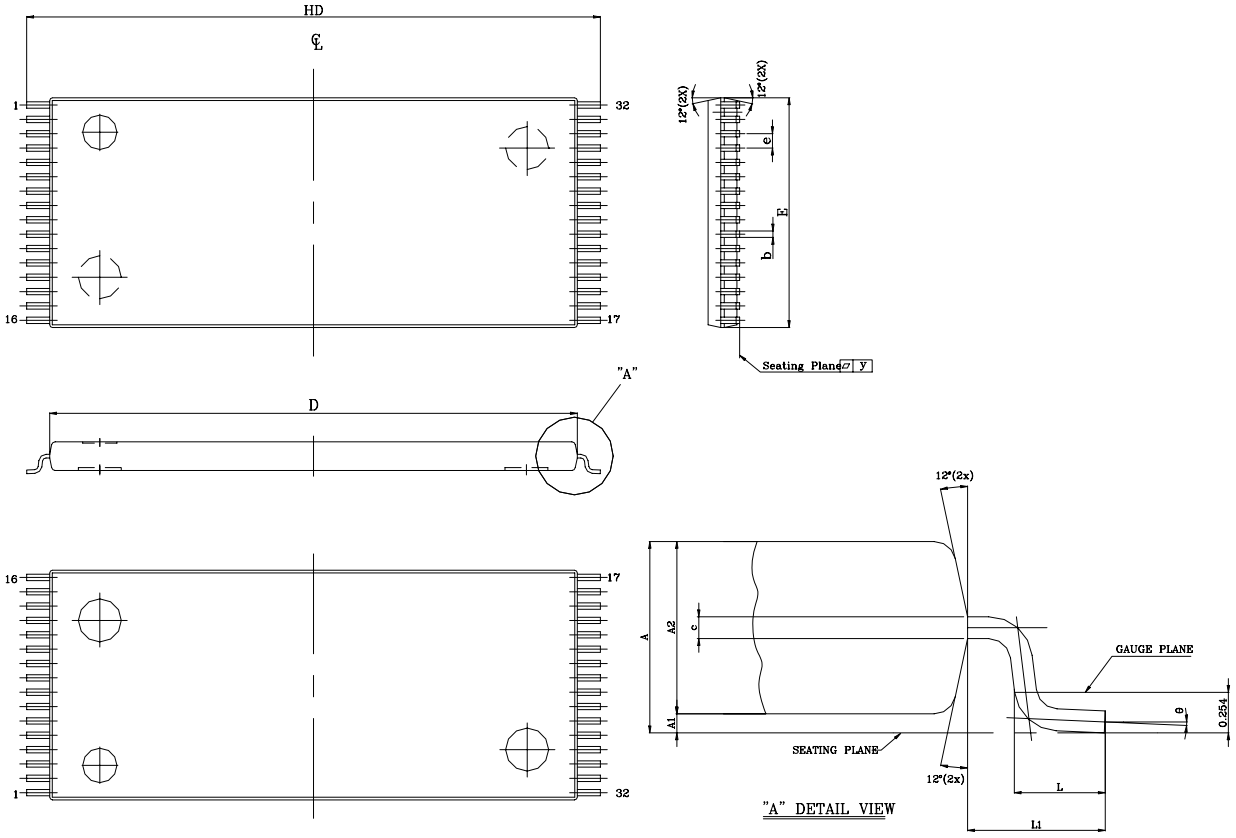
UNIT / SYMBOL	INCH(REF)	MM(BASE)
A	0.118 (MAX)	2.997 (MAX)
A1	0.004(MIN)	0.102(MIN)
A2	0.111(MAX)	2.82(MAX)
b	0.016(TYP)	0.406(TYP)
c	0.008(TYP)	0.203(TYP)
D	0.817(MAX)	20.75(MAX)
E	0.445 ±0.005	11.303 ±0.127
E1	0.555 ±0.012	14.097 ±0.305
e	0.050(TYP)	1.270(TYP)
L	0.0347 ±0.008	0.881 ±0.203
L1	0.055 ±0.008	1.397 ±0.203
S	0.026(MAX)	0.660 (MAX)
y	0.004(MAX)	0.101(MAX)
θ	0^o -10^o	0^o -10^o

32 pin STSOP Package Outline Dimension



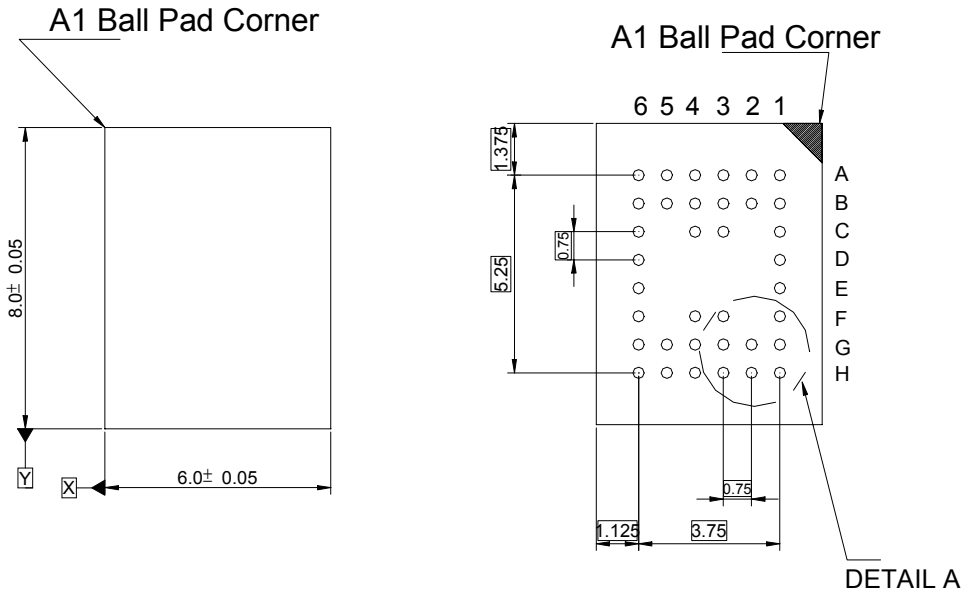
UNIT / SYMBOL	INCH(BASE)	MM(REF)
A	0.049 (MAX)	1.25 (MAX)
A1	0.005 ±0.002	0.130 ±0.05
A2	0.039 ±0.002	1.00 ±0.05
b	0.008 ±0.001	0.200±0.025
c	0.005 (TYP)	0.127 (TYP)
D	0.465 ±0.004	11.800 ±0.100
E	0.315 ±0.004	8.000 ±0.100
e	0.020 (TYP)	0.50 (TYP)
HD	0.528 ±0.008	13.40 ±0.20.
L	0.0197 ±0.004	0.50 ±0.10
L1	0.0315 ±0.004	0.8 ±0.10
y	0.003 (MAX)	0.076 (MAX)
Θ	0°～5°	0°～5°

32 pin TSOP-I Package Outline Dimension



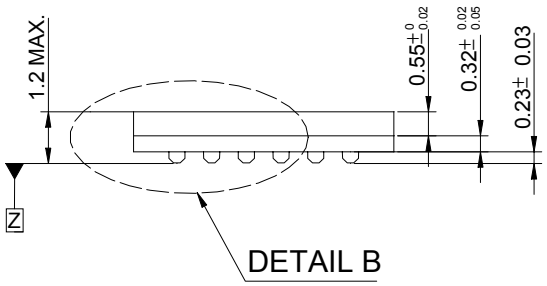
SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004 ±0.002	0.10 ±0.05
A2	0.039 ±0.002	1.00 ±0.05
b	0.008 + 0.002 - 0.001	0.20 + 0.05 -0.03
c	0.005 (TYP)	0.127 (TYP)
D	0.724 ±0.004	18.40 ±0.10
E	0.315 ±0.004	8.00 ±0.10
e	0.020 (TYP)	0.50 (TYP)
HD	0.787 ±0.008	20.00 ±0.20
L	0.0197 ±0.004	0.50 ±0.10
L1	0.0315 ±0.004	0.8 ±0.10
y	0.003 (MAX)	0.076 (MAX)
θ	0°～5°	0°～5°

36 pin TFBGA Package Outline Dimension

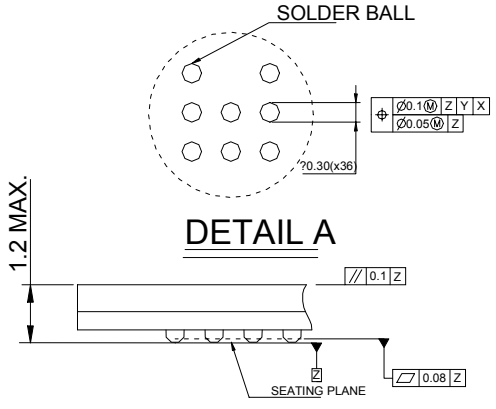


TOP VIEW (DIE VIEW)

BOTTOM VIEW (BALL SIDE)



SIDE VIEW



ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (µA) TYP.	PACKAGE
UT62L5128SC-55LI	55	20	32 PIN SOP
UT62L5128SC-55LLI	55	3	32 PIN SOP
UT62L5128SC-70LI	70	20	32 PIN SOP
UT62L5128SC-70LLI	70	3	32 PIN SOP
UT62L5128SC-100LI	100	20	32 PIN SOP
UT62L5128SC-100LLI	100	3	32 PIN SOP
UT62L5128LS-55LI	55	20	32 PIN STSOP
UT62L5128LS-55LLI	55	3	32 PIN STSOP
UT62L5128LS-70LI	70	20	32 PIN STSOP
UT62L5128LS-70LLI	70	3	32 PIN STSOP
UT62L5128LS-100LI	100	20	32 PIN STSOP
UT62L5128LS-100LLI	100	3	32 PIN STSOP
UT62L5128LC-55LI	55	20	32 PIN TSOP- I
UT62L5128LC-55LLI	55	3	32 PIN TSOP- I
UT62L5128LC-70LI	70	20	32 PIN TSOP- I
UT62L5128LC-70LLI	70	3	32 PIN TSOP- I
UT62L5128LC-100LI	100	20	32 PIN TSOP- I
UT62L5128LC-100LLI	100	3	32 PIN TSOP- I
UT62L5128BS-55LI	55	20	36 PIN TFBGA
UT62L5128BS-55LLI	55	3	36 PIN TFBGA
UT62L5128BS-70LI	70	20	36 PIN TFBGA
UT62L5128BS-70LLI	70	3	36 PIN TFBGA
UT62L5128BS-100LI	100	20	36 PIN TFBGA
UT62L5128BS-100LLI	100	3	36 PIN TFBGA

REVISION HISTORY

REVISION	DESCRIPTION	DATE
Preliminary Rev. 0.5	Original.	Mar, 2001
Preliminary Rev. 0.6	1. The symbols CE# and OE# and WE# are revised as. $\overline{CE}$ and $\overline{OE}$ and $\overline{WE}$. 2. Separate Industrial and Consumer SPEC. 3. Add access time 55ns range.	Jun 21,2001
Preliminary Rev. 0.7	1. Add SOP and STSOP package	Dec 18,2001

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