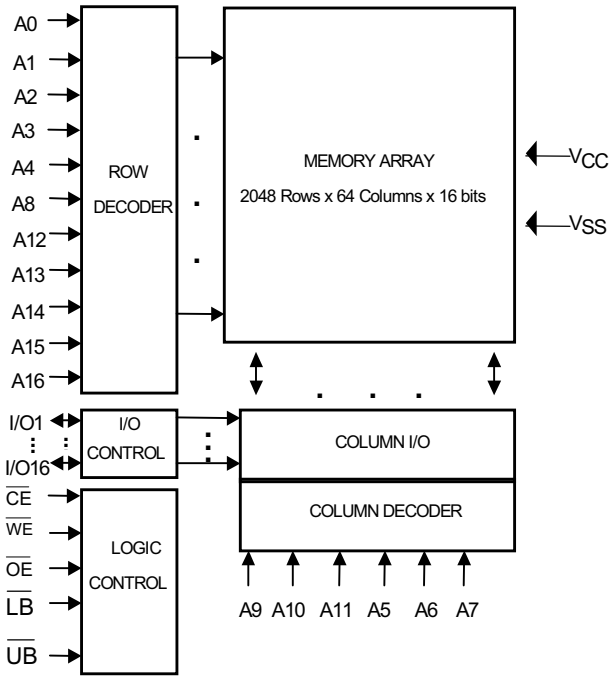
FEATURES

- Fast access time :
  55ns(max) for Vcc=3.0V~3.6V
  70/100 ns(max) for Vcc=2.7V~3.6V
- CMOS Low operating power
  Operating current: 45/35/25mA (Icc max)
  Standby current: 20 uA(TYP.) L-version
  3 uA(TYP.) LL-version
- Single 2.7V~3.6V power supply
- Operating temperature:
  Industrial : -40℃~85℃
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Data retention voltage: 1.5V (min)
- Data byte control : $\overline{LB}$ (I/O1~I/O8)
  $\overline{UB}$ (I/O9~I/O16)
- Package : 44-pin 400mil TSOP Ⅱ
  48-pin 6mm × 8mm TFBGA

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The UT62L12816(I) is a 2,097,152-bit low power CMOS static random access memory organized as 131,072 words by 16 bits.

The UT62L12816(I) operates from a single 2.7V ~ 3.6V power supply and all inputs and outputs are fully TTL compatible.

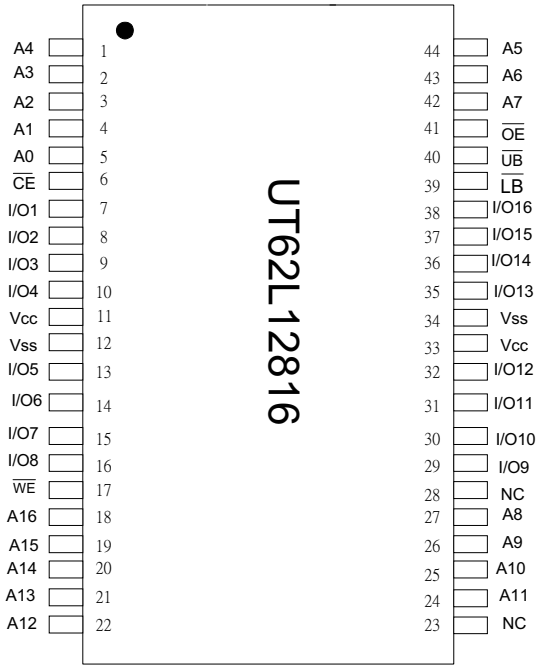
The UT62L12816(I) is designed for low power system applications. It is particularly suited for use in high-density high-speed system applications.

PIN DESCRIPTION

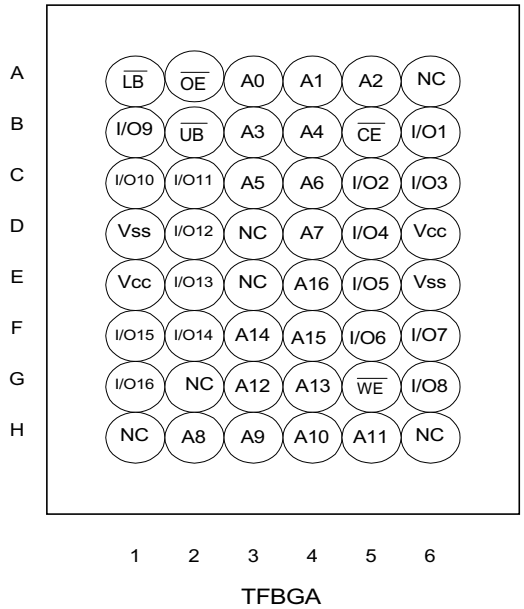
SYMBOL	DESCRIPTION
A0 - A16	Address Inputs
I/O1 - I/O16	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$	Lower-Byte Control
$\overline{UB}$	High-Byte Control
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

UTRON TECHNOLOGY INC.
1F, No. 11, R&D Rd. II, Science-Based Industrial Park, Hsinchu, Taiwan, R. O. C.
TEL: 886-3-5777882 FAX: 886-3-5777919

PIN CONFIGURATION



TSOP II



TFBGA

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O OPERATION		SUPPLY CURRENT
						I/O1-I/O8	I/O9-I/O16	
Standby	H	X	X	X	X	High – Z	High – Z	I_{SB}, I_{SB1}
	X	X	X	H	H	High – Z	High – Z	I_{SB}, I_{SB1}
Output Disable	L	H	H	L	X	High – Z	High – Z	I_{CC},I_{CC1},I_{CC2}
	L	H	H	X	L	High – Z	High – Z	
Read	L	L	H	L	H	D_{OUT}	High – Z	I_{CC},I_{CC1},I_{CC2}
	L	L	H	H	L	High – Z	D_{OUT}	
	L	L	H	L	L	D_{OUT}	D_{OUT}	
Write	L	X	L	L	H	D_{IN}	High – Z	I_{CC},I_{CC1},I_{CC2}
	L	X	L	H	L	High – Z	D_{IN}	
	L	X	L	L	L	D_{IN}	D_{IN}	

Note: H = V_{IH}, L=V_{IL}, X = Don't care.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER		SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V_{SS}		V_{TERM}	-0.5 to 4.6	V
Operating Temperature	Industrial	T_A	-40 to 85	℃
Storage Temperature		T_{STG}	-65 to 150	℃
Power Dissipation		P_D	1	W
DC Output Current		I_{OUT}	50	mA
Soldering Temperature (under 10 secs)		Tsolder	260	℃

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7V~3.6V, TA = -40℃ to 85℃(I))

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Power Voltage	V_{CC}			2.7	3.0	3.6	V
Input High Voltage	V_{IH}			2.0	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}			-0.2	-	0.6	V
Input Leakage Current	I_{LI}	$V_{SS} \leqq V_{IN} \leqq V_{CC}$		- 1	-	1	µA
Output Leakage Current	I_{LO}	$V_{SS} \leqq V_{I/O} \leqq V_{CC;}$ Output Disabled		- 1	-	1	µA
Output High Voltage	V_{OH}	I_{OH}= -1mA		2.2	-	-	V
Output Low Voltage	V_{OL}	I_{OL}= 2.1mA		-	-	0.4	V
Operating Power Supply Current	I_{CC}	Cycle time=min, 100%duty, I/O=0mA, $\overline{CE}$=V_{IL} ;	55	-	30	45	mA
			70	-	25	35	mA
			100	-	20	25	mA
Average Operation Current	Icc1	Cycle time=1µs,100%duty,I/O=0mA, $\overline{CE}$ ≦0.2V,other pins at 0.2V or Vcc-0.2V,		-	4	5	mA
	Icc2	Cycle time=500ns,100%duty,I/O=0mA, $\overline{CE}$ ≦0.2V,other pins at 0.2V or Vcc-0.2V,		-	8	10	mA
Standby Current (TTL)	I_{SB}	$\overline{CE}$=$V_{IH,}$ other pins =V_{IL} or V_{IH},		-	0.3	0.5	mA
Standby Current (CMOS)	I_{SB1}	$\overline{CE}$=V_{CC}-0.2V, other pins at 0.2V or Vcc-0.2V,	-L	-	20	80	µA
			-LL	-	3	25	µA

CAPACITANCE (TA=25℃, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 30pF, I_{OH}/I_{OL} = -1mA / 2mA

AC ELECTRICAL CHARACTERISTICS (VCC =2.7V~3.6V, TA = -40℃ to 85℃(I))

(1) READ CYCLE

PARAMETER	SYMBOL	UT62L12816(I)-55*		UT62L12816(I)-70		UT62L12816(I)-100		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	55	-	70	-	100	-	ns
Address Access Time	t_{AA}	-	55	-	70	-	100	ns
Chip Enable Access Time	t_{ACE}	-	55	-	70	-	100	ns
Output Enable Access Time	t_{OE}	-	30	-	35	-	50	ns
Chip Enable to Output in Low Z	t_{CLZ*}	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	t_{OLZ*}	5	-	5	-	5	-	ns
Chip Disable to Output in High Z	t_{CHZ*}	-	20	-	25	-	30	ns
Output Disable to Output in High Z	t_{OHZ*}	-	20	-	25	-	30	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	5	-	ns
$\overline{LB}$, $\overline{UB}$ Access Time	t_{BA}	-	55	-	70	-	100	ns
$\overline{LB}$, $\overline{UB}$ to High-Z Output	t_{HZB}	-	25	-	30	-	40	ns
$\overline{LB}$, $\overline{UB}$ to Low-Z Output	t_{LZB}	0	-	0	-	0	-	ns

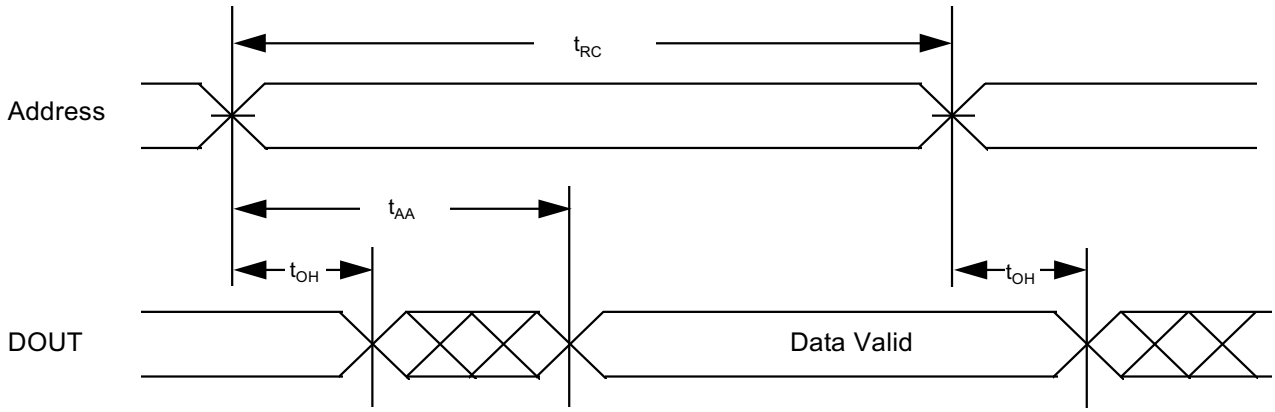
(2) WRITE CYCLE

PARAMETER	SYMBOL	UT62L12816(I)-55*		UT62L12816(I)-70		UT62L12816(I)-100		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	55	-	70	-	100	-	ns
Address Valid to End of Write	t_{AW}	50	-	60	-	80	-	ns
Chip Enable to End of Write	t_{CW}	50	-	60	-	80	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	45	-	55	-	70	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	25	-	30	-	40	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW*}	5	-	5	-	5	-	ns
Write to Output in High Z	t_{WHZ*}	-	30	-	30	-	40	ns
$\overline{LB}$, $\overline{UB}$ Valid to End of Write	t_{PWB}	45	-	60	-	80	-	ns

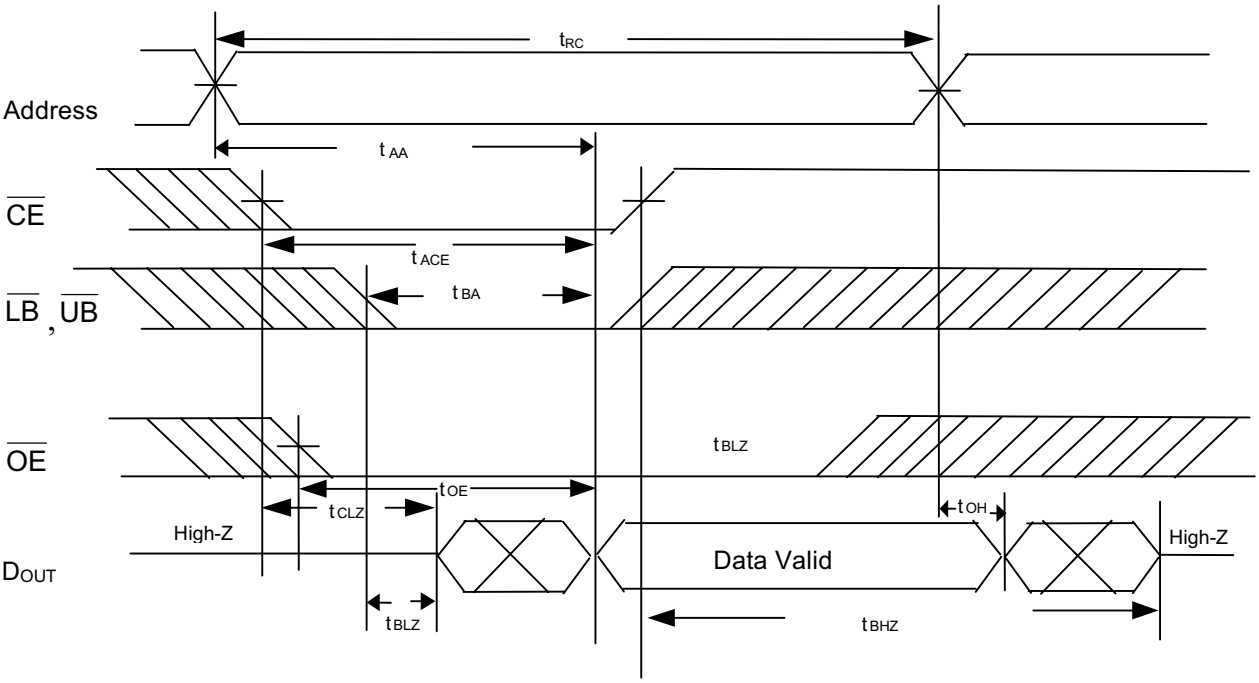
* These parameters are guaranteed by device characterization, but not production tested.
* 55ns for Vcc=3.0V~3.6V

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)



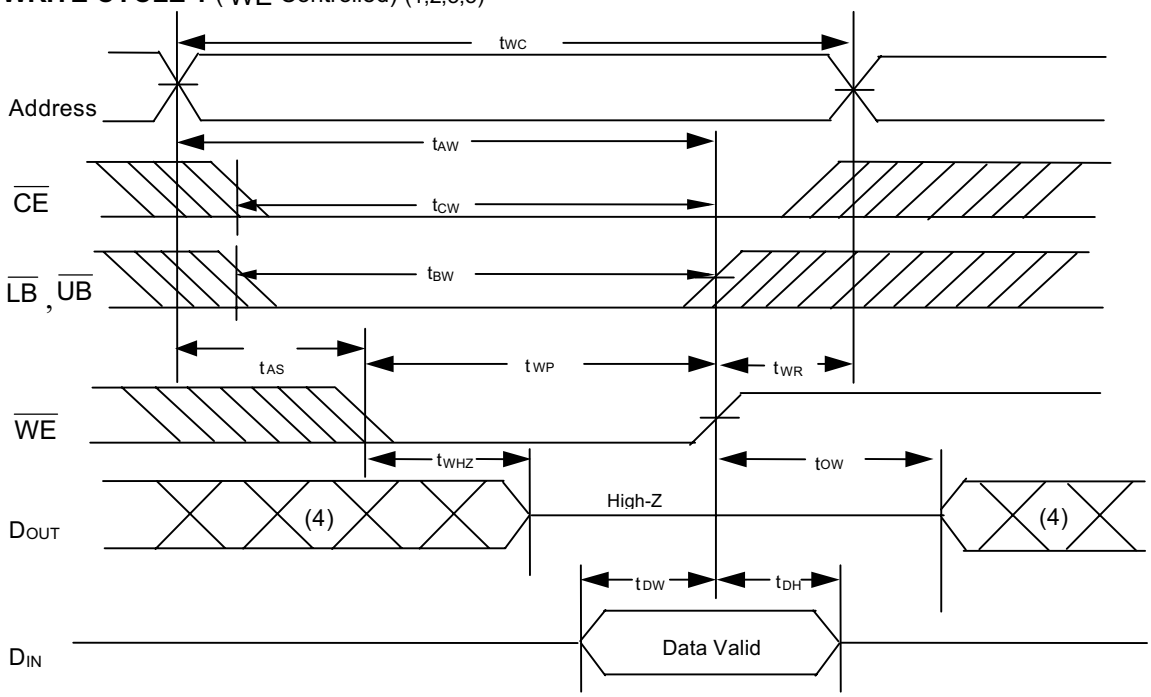
READ CYCLE 2 ($\overline{CE}$ and $\overline{OE}$ Controlled) (1,3,5,6)



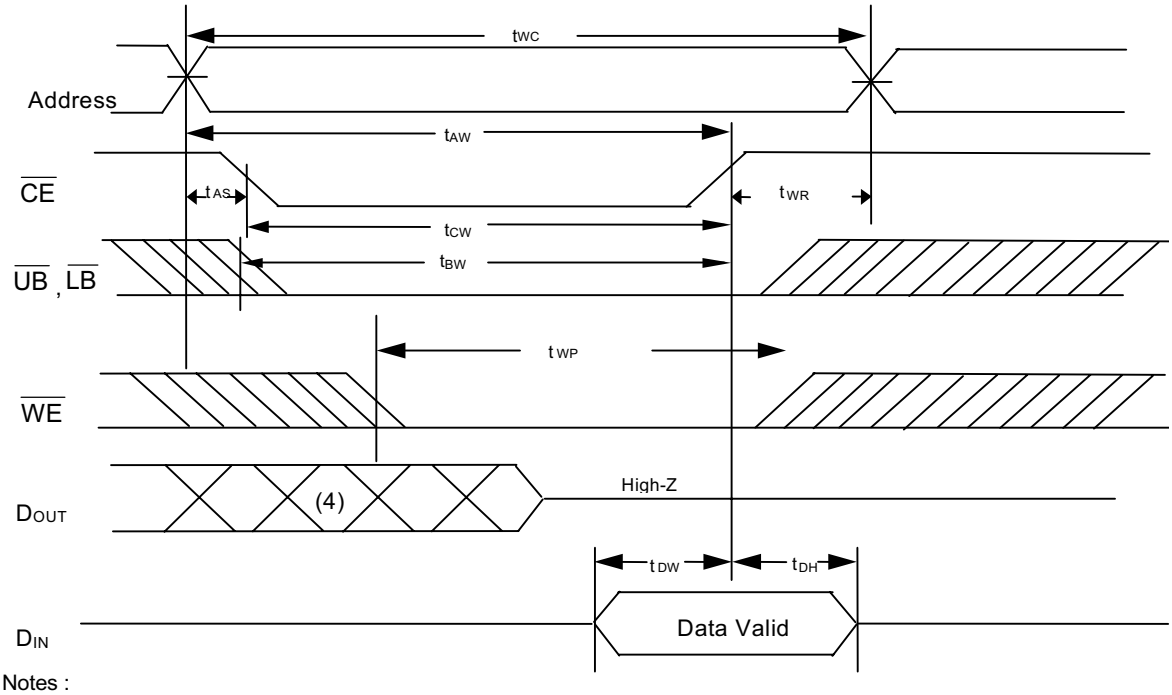
Notes :

1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected $\overline{CE}$ =V_{IL}.
3. Address must be valid prior to or coincident with $\overline{CE}$ transition; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. t_{CLZ}, t_{OLZ}, t_{CHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ± 500mV from steady state.
6. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ}, t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 ($\overline{WE}$ Controlled) (1,2,3,5)



WRITE CYCLE 2 ($\overline{CE}$ Controlled) (1,2,5)



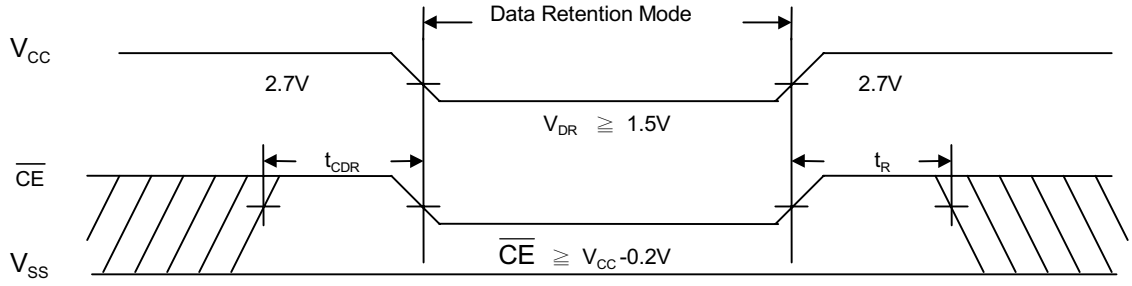
Notes :

1. $\overline{WE}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$.
3. During a $\overline{WE}$ controlled with write cycle with $\overline{OE}$ LOW, t_{WP} must be greater than $t_{WHZ}+t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ LOW transition occurs simultaneously with or after $\overline{WE}$ LOW transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ± 500mV from steady state.

DATA RETENTION CHARACTERISTICS (TA = -40℃ to 85℃(I))

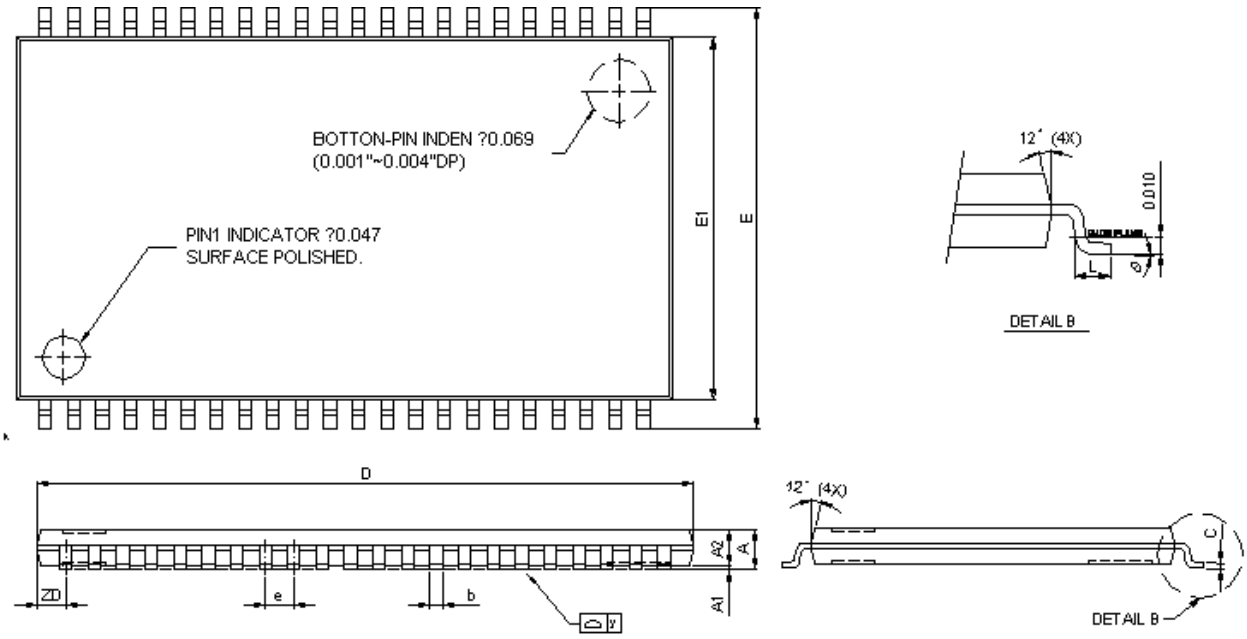
PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V_{DR}	$\overline{CE} \geqq V_{CC}$-0.2V		1.5	-	3.6	V
Data Retention Current	I_{DR}	Vcc=1.5V	- L	-	1	50	µA
		$\overline{CE} \geqq V_{CC}$-0.2V	- LL	-	0.5	20	µA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)		0	-	-	ms
Recovery Time	t_R			5	-	-	ms

DATA RETENTION WAVEFORM



PACKAGE OUTLINE DIMENSION

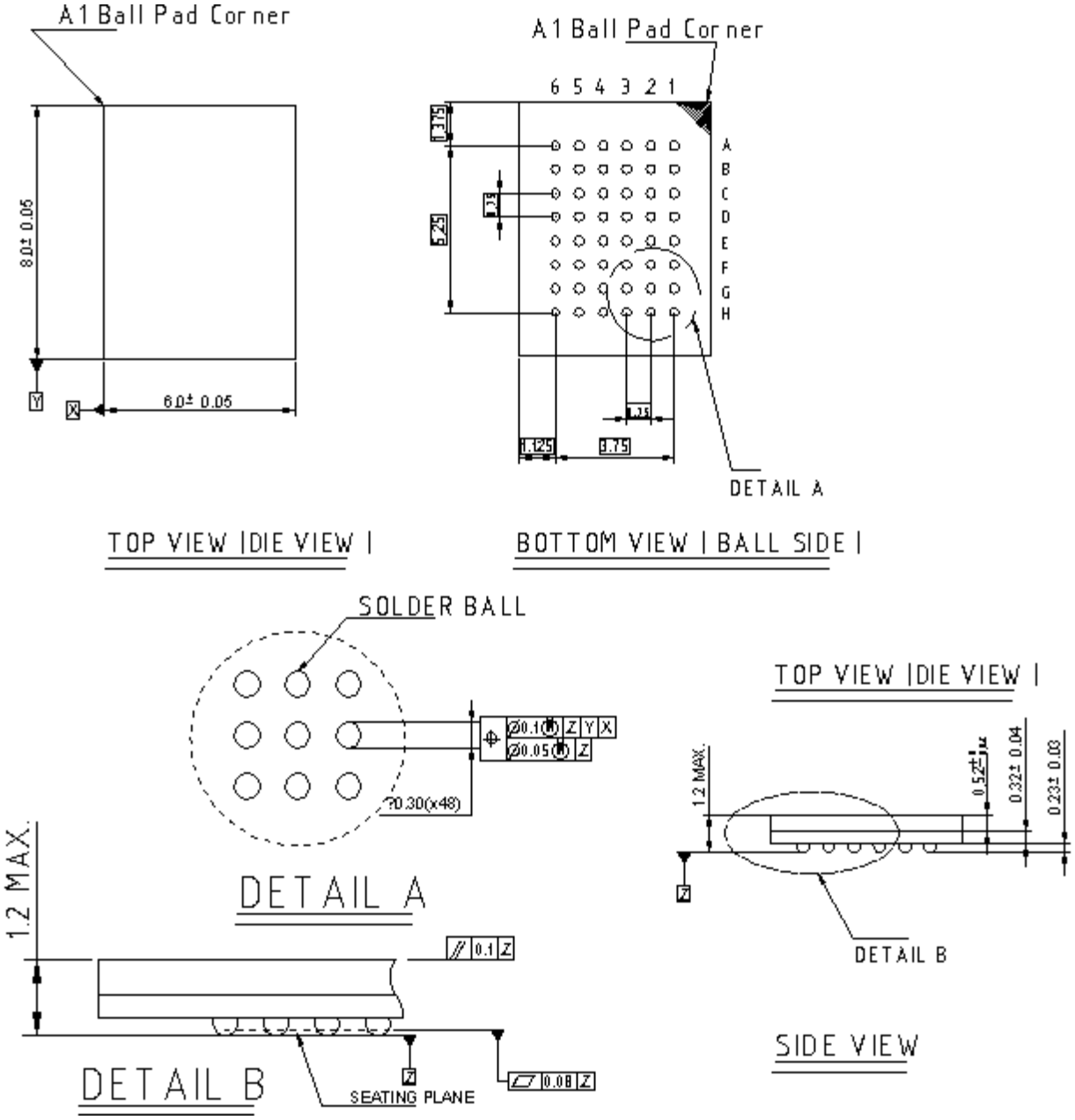
44 pin 400mil TSOP-Ⅱ Package Outline Dimension



1.CONTROLLING DIMENSION: INCH
2.LEAD FRAME MATERIAL: ALLOY 42
3.DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, THE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006"[0.15mm] PER END DIMENSION "E1" DOES NOT INCLUDE INTERLEAD FLASH, INTERLEAD FLASH SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4.DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003"[0.008mm] TOTAL IN EXCEED OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.0028"[0.07mm]
5.TOLERANCE: 60.010"[0.25mm] UNLESS OTHERWISE SPECIFIED.
6.OTHERWISE DIMENSION FOLLOW ACCEPTABLE SPEC.
7.REFERENCE DOCUMENT: JEDEC SPEC. MS-024

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	——	1.20	0.039	——	0.047
A1	0.05	——	0.15	0.002	——	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	0.35	0.45	0.012	0.014	0.018
C	0.12	——	0.21	0.0047	——	0.0083
D	18.313	18.415	18.517	0.721	0.725	0.729
E	11.684	11.836	11.938	0.460	0.466	0.470
E1	10.058	10.160	10.262	0.396	0.400	0.404
e	——	0.800	——	——	0.0315	——
L	0.40	0.50	0.60	0.0157	0.020	0.0236
ZD	——	0.805	——	——	0.0317	——
θ	0°	——	8°	0°	——	8°
y	0.00	——	0.076	0.000	——	0.003

48 pin 6mm×8mm TFBGA Package Outline Dimension



ORDERING INFORMATION

INDUSTRIAL TEMPERATURE

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA) TYP.	PACKAGE
UT62L12816MC-55LI	55	20	44 PIN TSOP-Ⅱ
UT62L12816MC-55LLI	55	3	44 PIN TSOP-Ⅱ
UT62L12816MC-70LI	70	20	44 PIN TSOP-Ⅱ
UT62L12816MC-70LLI	70	3	44 PIN TSOP-Ⅱ
UT62L12816BS-55LI	55	20	48 PIN TFBGA
UT62L12816BS-55LLI	55	3	48 PIN TFBGA
UT62L12816BS-70LI	70	20	48 PIN TFBGA
UT62L12816BS-70LLI	70	3	48 PIN TFBGA

REVISION HISTORY

REVISION	DESCRIPTION	DATE
Preliminary Rev. 0.5	Original.	Mar, 2001
Preliminary Rev. 0.6	1. The symbols CE# and OE# and WE# are revised as. $\overline{CE}$ and $\overline{OE}$ and $\overline{WE}$. 2. Separate Industrial and Consumer SPEC. 3. Add access time 55ns range.	Jun 21,2001

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