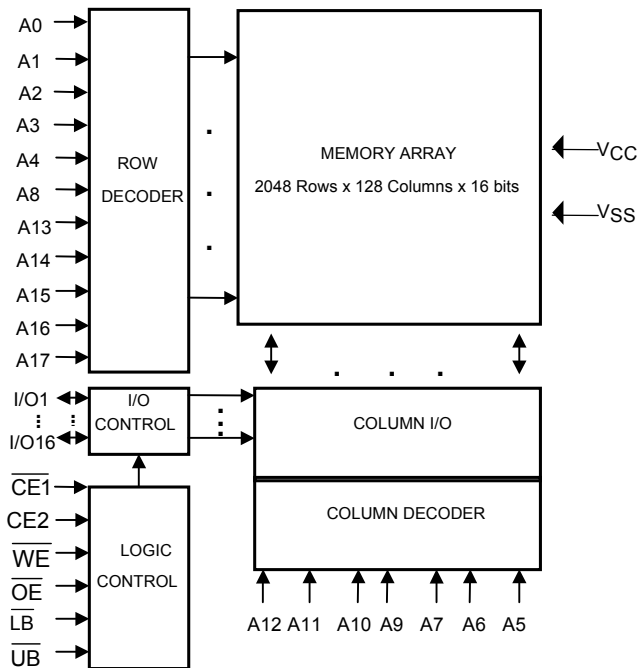




FEATURES

- High speed access time :
55ns(max) for Vcc=3.0V~3.6V
70/100 ns(max) for Vcc=2.7V~3.6V
- CMOS Low power consumption
- Operation current : 45/35/25 (Icc,max.)
- Standby: 20uA (TYP.) L-version
3uA (TYP.) LL-version
- Single 2.7V~3.6V power supply
- Operation temperature:
Industrial : -40°C~85°C
- All inputs and outputs are TTL compatible
- Fully static operation
- Three state outputs
- Data retention voltage:1.5V (min.)
- Data byte control : \overline{LB} (I/O1~I/O8)
 \overline{UB} (I/O9~I/O16)
- Package : 48-pin 6mm x 8mm TFBGA

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The UT62L25716(I) is a 4,194,304-bit low power CMOS static random access memory organized as 262,144 words by 16 bits.

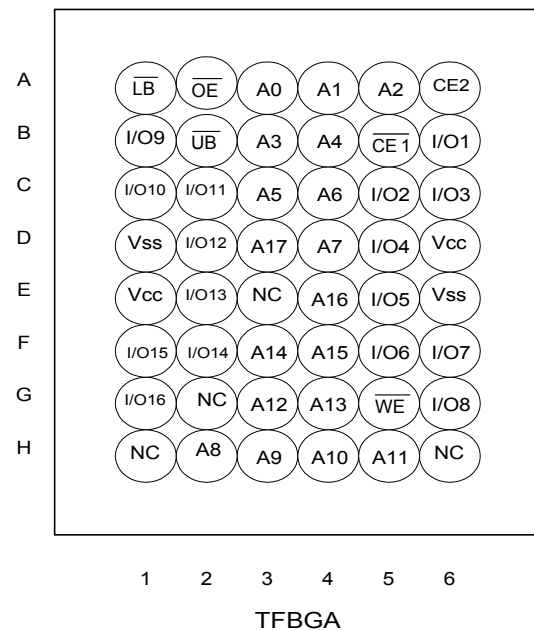
The UT62L25716(I) operates from a single 2.7V ~ 3.6V power supply and all inputs and outputs are fully TTL compatible.

The UT62L25716(I) is designed for low power system applications. It is particularly well suited for use in high-density low power system applications.

PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A17	Address Inputs
I/O1 - I/O16	Data Inputs/Outputs
$\overline{CE1}$, CE2	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
\overline{LB}	Lower-Byte Control
\overline{UB}	High-Byte Control
Vcc	Power Supply
Vss	Ground
NC	No Connection

PIN CONFIGURATION





ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V _{SS}	V _{TERM}	-0.3 to 4.6	V
Operating Temperature	T _A	-40 to 85	°C
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1.0~1.5	W
DC Output Current	I _{OUT}	20	mA
Soldering Temperature (under 10 secs)	T _{solder}	260.10	°C.sec

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE1	CE2	OE	WE	LB	UB	I/O1-I/O8	I/O9-I/O16	SUPPLY CURRENT
Standby	H	X	X	X	X	X	High - Z	High - Z	I _{SB} , I _{SB1}
	X	L	X	X	X	X	High - Z	High - Z	I _{SB} , I _{SB1}
	X	X	X	X	H	H	High - Z	High - Z	I _{SB} , I _{SB1}
Output Disable	L	H	H	H	L	X	High - Z	High - Z	I _{CC1} , I _{CC2}
	L	H	H	H	X	L	High - Z	High - Z	I _{CC1} , I _{CC2}
Read	L	H	L	H	L	H	D _{OUT}	High - Z	I _{CC1} , I _{CC2}
	L	H	L	H	H	L	High - Z	D _{OUT}	I _{CC1} , I _{CC2}
	L	H	L	H	L	L	D _{OUT}	D _{OUT}	I _{CC1} , I _{CC2}
Write	L	H	X	L	L	H	D _{IN}	High - Z	I _{CC1} , I _{CC2}
	L	H	X	L	H	L	High - Z	D _{IN}	I _{CC1} , I _{CC2}
	L	H	X	L	L	L	D _{IN}	D _{IN}	I _{CC1} , I _{CC2}

Note: H = V_{IH}, L = V_{IL}, X = Don't care. (Must be low or high state)

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7V~3.6V, T_A = -40°C to 85°C (I))

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Power Voltage	V _{CC}		2.7	3.0	3.6	V	
Input High Voltage	V _{IH}		2.0	-	V _{CC} +0.3	V	
Input Low Voltage	V _{IL}		-0.2	-	0.6	V	
Input Leakage Current	I _{LI}	V _{SS} ≤ V _{IN} ≤ V _{CC}	-1	-	1	μA	
Output Leakage Current	I _{LO}	V _{SS} ≤ V _{I/O} ≤ V _{CC} , Output Disabled	-1	-	1	μA	
Output High Voltage	V _{OH}	I _{OH} = -1.0mA	2.2	-	-	V	
Output Low Voltage	V _{OL}	I _{OL} = 2.1mA	-	-	0.4	V	
Operating Power Supply Current	I _{CC}	Cycle time = min, 100% duty, I _{I/O} = 0mA, CE2 = V _{IH} , CE1 = V _{IL} , V _{IN} = V _{IH} or V _{IL} ,	55	-	30	45	mA
			70	-	25	35	mA
			100	-	20	25	mA
	I _{CC1}	Cycle time = 1us, 100% duty, I _{I/O} = 0mA, CE1 ≤ 0.2V, CE2 ≥ V _{CC} -0.2V, other pins at 0.2V or V _{CC} -0.2V,	-	4	5	mA	
	I _{CC2}	Cycle time = 500ns, 100% duty, I _{I/O} = 0mA, CE1 ≤ 0.2V, CE2 ≥ V _{CC} -0.2V, other pins at 0.2V or V _{CC} -0.2V,	-	8	10	mA	
Standby Current	I _{SB}	CE1 = V _{IH} , or CE2 = V _{IH} , other pins = V _{IH} or V _{IL} ,	-	0.3	0.5	mA	
Standby Current	I _{SB1}	CE1 ≥ V _{CC} -0.2V, or CE2 ≤ 0.2V, other pins at 0.2V or V _{CC} -0.2V,	-L	-	20	80	μA
			-LL	-	3	25	μA

**CAPACITANCE** (TA=25°C, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 30pF, I _{OH} /I _{OL} = -1mA/2mA

AC ELECTRICAL CHARACTERISTICS (VCC = 2.7V~3.6V, TA = -40°C to 85°C(I))**(1) READ CYCLE**

PARAMETER	SYMBOL	UT62L25716(I)-55*		UT62L25716(I)-70		UT62L25716(I)-100		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	55	-	70	-	100	-	ns
Address Access Time	t _{AA}	-	55	-	70	-	100	ns
Chip Enable Access Time	t _{ACE}	-	55	-	70	-	100	ns
Output Enable Access Time	t _{OE}	-	30	-	35	-	50	ns
Chip Enable to Output in Low Z	t _{CLZ*}	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	t _{OLZ*}	5	-	5	-	5	-	ns
Chip Disable to Output in High Z	t _{CHZ*}	-	20	-	25	-	30	ns
Output Disable to Output in High Z	t _{OHZ*}	-	20	-	25	-	30	ns
Output Hold from Address Change	t _{OH}	5	-	5	-	5	-	ns
\overline{LB} , \overline{UB} Access Time	t _{BA}	-	55	-	70	-	100	ns
\overline{LB} , \overline{UB} to High-Z Output	t _{HZB}	-	25	-	30	0	40	ns
\overline{LB} , \overline{UB} to Low-Z Output	t _{LZB}	0	-	0	-	0	-	ns

(2) WRITE CYCLE

PARAMETER	SYMBOL	UT62L25716(I)-55*		UT62L25716(I)-70		UT62L25716(I)-100		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	55	-	70	-	100	-	ns
Address Valid to End of Write	t _{AW}	50	-	60	-	80	-	ns
Chip Enable to End of Write	t _{CW}	50	-	60	-	80	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t _{WP}	45	-	55	-	70	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	25	-	30	-	40	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t _{OW*}	5	-	5	-	5	-	ns
Write to Output in High Z	t _{WHZ*}	-	30	-	30	-	40	ns
\overline{LB} , \overline{UB} Valid to End of Write	t _{PWB}	45	-	60	-	80	-	ns

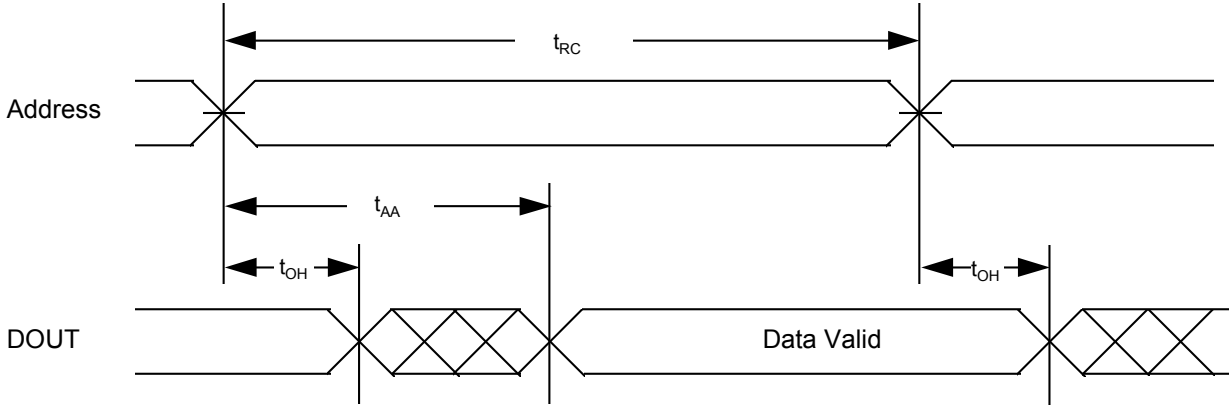
* These parameters are guaranteed by device characterization, but not production tested.

* 55ns for 3.0V~3.6V.

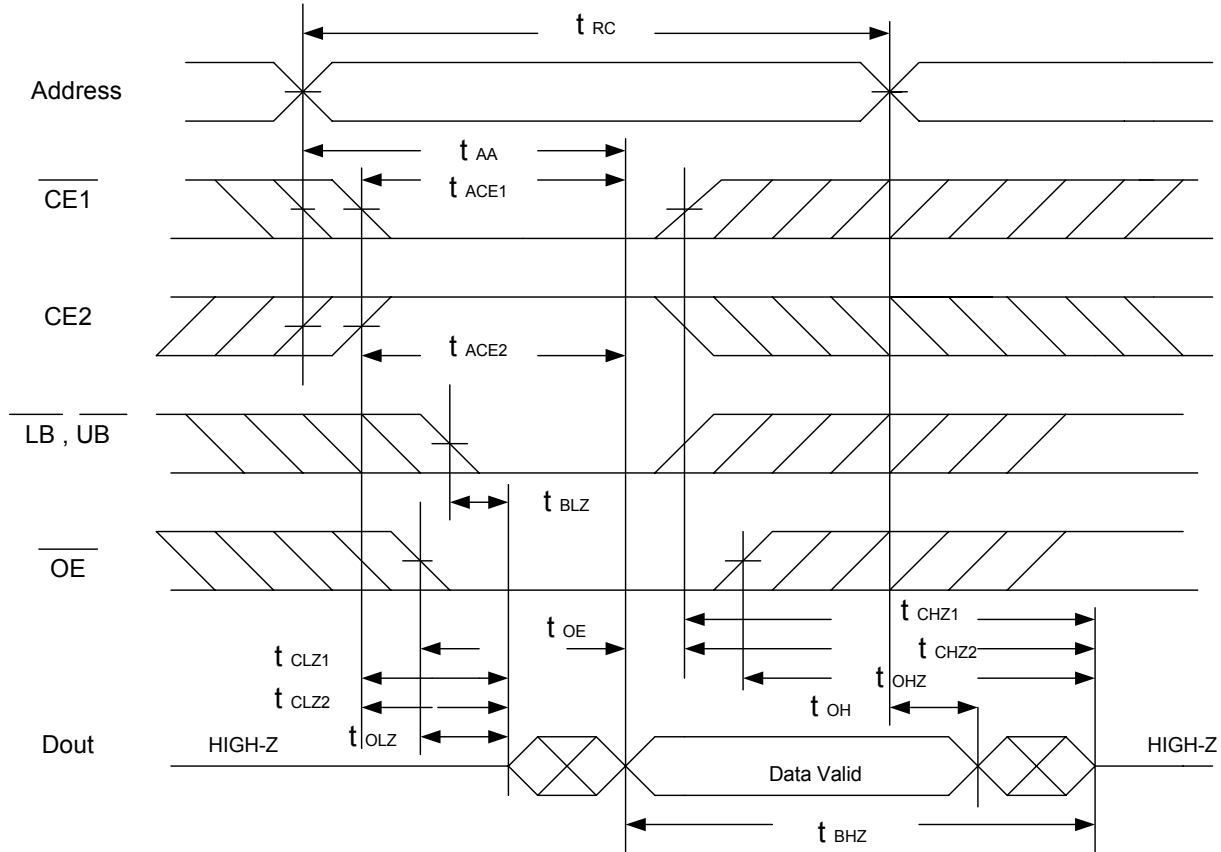


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)



READ CYCLE 2 ($\overline{CE1}$ and $\overline{CE2}$ and \overline{OE} Controlled) (1,3,5,6)

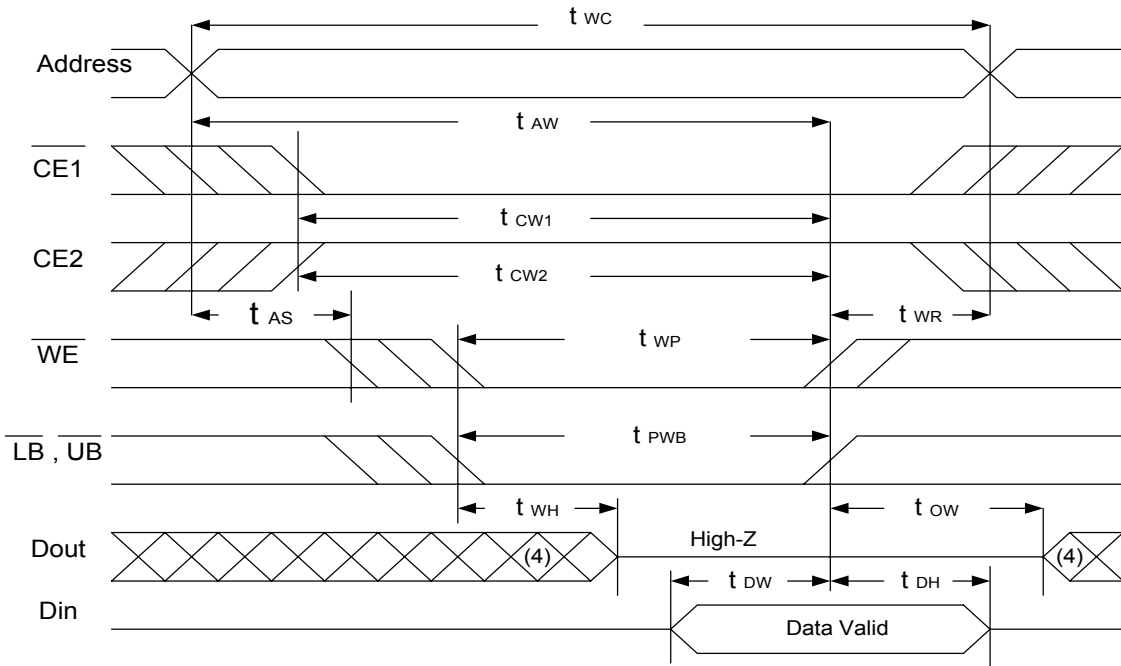


Notes :

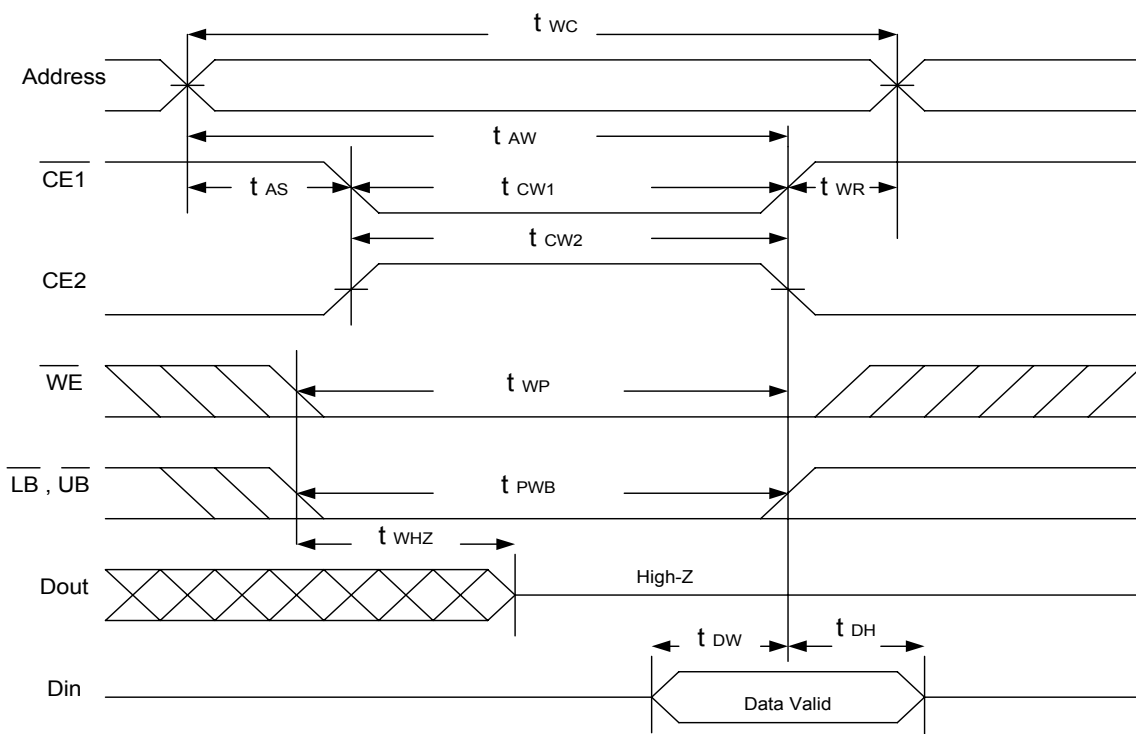
- \overline{WE} is HIGH for read cycle.
- Device is continuously selected $\overline{CE1}=V_{IL}$ and $\overline{CE2}=V_{IH}$. and $\overline{LB}=V_{IL}$ and $\overline{UB}=V_{IH}$.
- Address must be valid prior to or coincident with $\overline{CE1}$ and $\overline{CE2}$ and \overline{LB} and \overline{UB} transition; otherwise t_{AA} is the limiting parameter.
- \overline{OE} is low.
- t_{CLZ1} , t_{CLZ2} , t_{OLZ} , t_{CHZ1} , t_{CHZ2} and t_{OH} are specified with $C_L=5pF$. Transition is measured $\pm 500mV$ from steady state.
- At any given temperature and voltage condition, t_{CHZ1} is less than t_{CLZ1} , t_{CHZ2} is less than t_{CLZ2} , t_{OH} is less than t_{OLZ} .



WRITE CYCLE 1 (\overline{WE} Controlled) (1,2,3,5)



WRITE CYCLE 2 ($\overline{CE1}$ and CE2 Controlled) (1,2,5)



Notes :

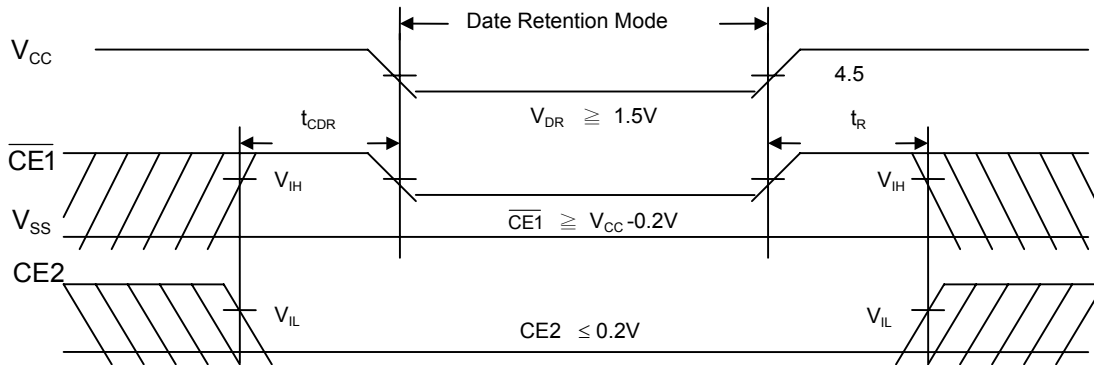
1. \overline{WE} or $\overline{CE1}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a low $\overline{CE1}$ and a low \overline{WE} .
3. During a \overline{WE} controlled with write cycle with \overline{OE} LOW, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE1}$ LOW transition occurs simultaneously with or after \overline{WE} LOW transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.



DATA RETENTION CHARACTERISTICS (TA = -40°C to 85°C(I))

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Vcc for Data Retention	V _{DR}	$\overline{CE1} \geq V_{CC}-0.2V$ or $CE2 \leq 0.2V$	1.5	-	3.6	V	
Data Retention Current	I _{DR}	V _{CC} =1.5V $\overline{CE1} \geq V_{CC}-0.2V$ or $CE2 \leq 0.2V$	- L	-	1	50	μA
			- LL	-	0.5	20	μA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ms	
Recovery Time	t _R		5	-	-	ms	

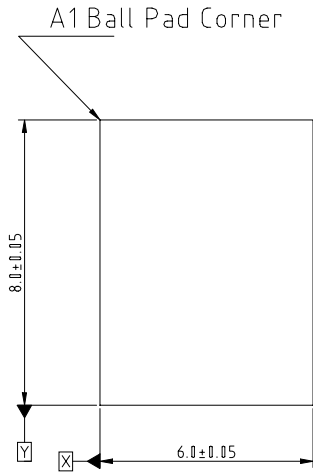
DATA RETENTION WAVEFORM



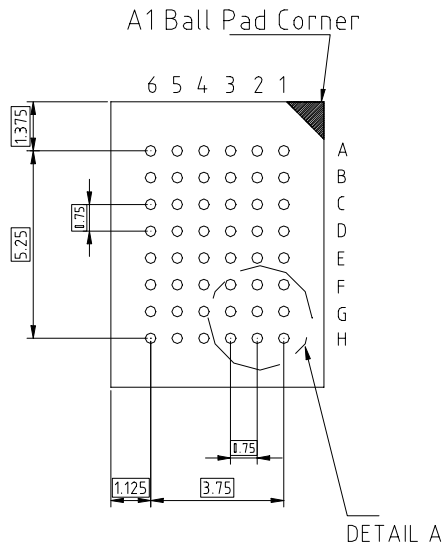


PACKAGE OUTLINE DIMENSION

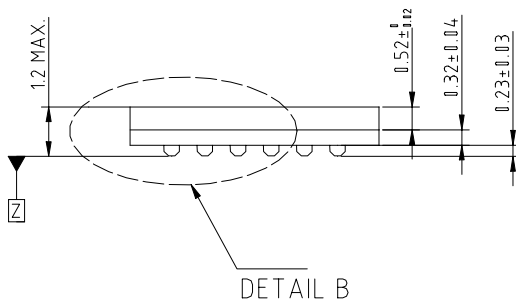
48 pin 6.0mmX8.0mm TFBGA Package Outline Dimension



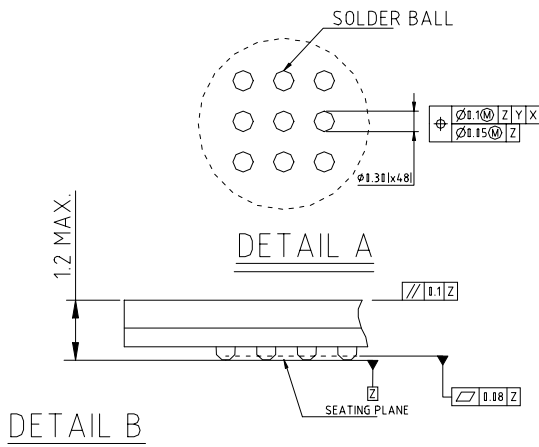
TOP VIEW | DIE VIEW |



BOTTOM VIEW | BALL SIDE |



SIDE VIEW





UTRON

UT62L25716(I)

Rev. 1.0

256K X 16 BIT LOW POWER CMOS SRAM

ORDERING INFORMATION

INDUSTRIAL TEMPERATURE

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA max)	PACKAGE
UT62L25716BS-55LI	55	20	48 PIN BGA
UT62L25716BS-55LLI	55	3	48 PIN BGA
UT62L25716BS-70LI	70	20	48 PIN BGA
UT62L25716BS-70LLI	70	3	48 PIN BGA



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UT62L25716(I)

Rev. 1.0

256K X 16 BIT LOW POWER CMOS SRAM

REVISION HISTORY

REVISION	DESCRIPTION	DATE
Preliminary Rev. 0.5	Original.	Mar, 2001
Rev.1.0	1. Separate Industrial and Commercial SPEC. 2. New waveforms. 3. Add access time 55ns range. 4. The symbols CE1# and OE# and WE# are revised as $\overline{CE1}$ and \overline{OE} and \overline{WE} .	Aug 7,2001



Rev. 1.0

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UT62L25716(I)

256K X 16 BIT LOW POWER CMOS SRAM

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