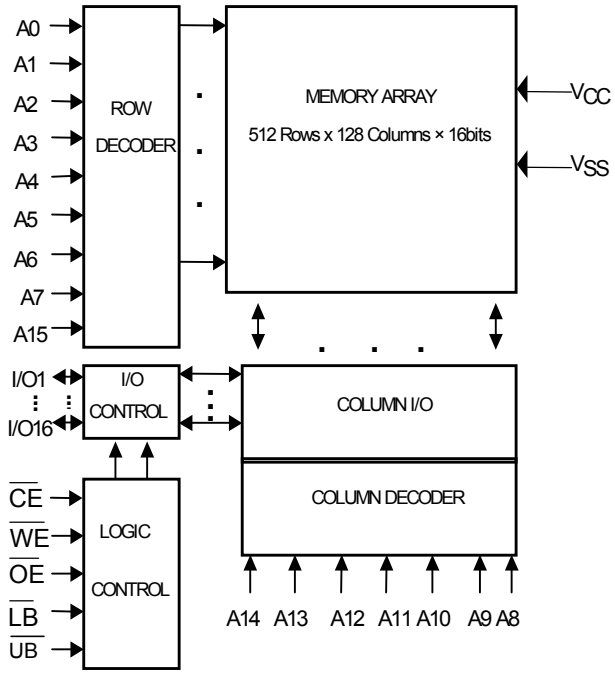
FEATURES

- Fast access time :
  8ns(max) for Vcc=3.15V~3.6V
  10/12/15ns(max) for Vcc=3.0V~3.6V
- Low power consumption
  Operating : 195mA (MAX.)
  Standby : 30 mA(MAX.)
- Single 3.0V~3.6V power supply
- Operating temperature:
  Commercial : 0℃~70℃
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Data byte control : $\overline{LB}$ (I/O1~I/O8)
  $\overline{UB}$ (I/O9~I/O16)
- Package : 44-pin 400mil TSOP Ⅱ

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The UT61L6416 is a 1,048,576-bit high speed CMOS static random access memory organized as 65,536 words by 16 bits.

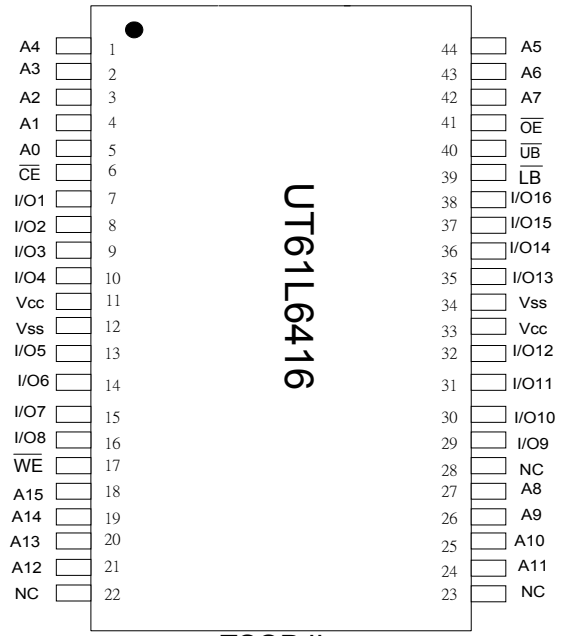
The UT61L6416 operates from a single 3.0V ~ 3.6V power supply and all inputs and outputs are fully TTL compatible.

The UT61L6416 is designed for lower and upper byte access by data byte control.($\overline{LB}$ $\overline{UB}$)

PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A15	Address Inputs
I/O1 - I/O16	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$	Lower-Byte Control
$\overline{UB}$	High-Byte Control
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

PIN CONFIGURATION



TSOP II

UTRON TECHNOLOGY INC.
1F, No. 11, R&D Rd. II, Science-Based Industrial Park, Hsinchu, Taiwan, R. O. C.
TEL: 886-3-5777882 FAX: 886-3-5777919

ABSOLUTE MAXIMUM RATINGS*

PARAMETER		SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V_{SS}		V_{TERM}	-0.5 to 4.6	V
Operating Temperature	Commercial	T_A	0 to 70	℃
Storage Temperature		T_{STG}	-65 to +150	℃
Power Dissipation		P_D	1	W
DC Output Current		I_{OUT}	50	mA
Soldering Temperature (under 10 secs)		Tsolder	260	℃

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O OPERATION		SUPPLY CURRENT
						I/O1-I/O8	I/O9-I/O16	
Standby	H	X	X	X	X	High – Z	High – Z	I_{SB}, I_{SB1}
Output Disable	L	H	H	L	X	High – Z	High – Z	I_{CC}
	L	H	H	X	L	High – Z	High – Z	
Read	L	L	H	L	H	D_{OUT}	High – Z	I_{CC}
	L	L	H	H	L	High – Z	D_{OUT}	
	L	L	H	L	L	D_{OUT}	D_{OUT}	
Write	L	X	L	L	H	D_{IN}	High – Z	I_{CC}
	L	X	L	H	L	High – Z	D_{IN}	
	L	X	L	L	L	D_{IN}	D_{IN}	

Note: H = V_{IH}, L=V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.0V~3.6V, TA = 0℃ to 70℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Power Voltage	V_{CC}			3.0	3.3	3.6	V
Input High Voltage	V_{IH}			2.0	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}			-0.3	-	0.8	V
Input Leakage Current	I_{LI}	$V_{SS} \leqq V_{IN} \leqq V_{CC}$		- 2	-	2	μA
Output Leakage Current	I_{LO}	$V_{SS} \leqq V_{I/O} \leqq V_{CC;}$ Output Disabled		- 2	-	2	μA
Output High Voltage	V_{OH}	I_{OH}= -4mA		2.4	-	-	V
Output Low Voltage	V_{OL}	I_{OL}= 8 mA		-	-	0.4	V
Operating Power Supply Current	I_{CC}	Cycle time=min, 100%duty, I/O=0mA, $\overline{CE}$ =V_{IL} ;	8	-	-	200	mA
			10	-	-	195	mA
			12	-	-	190	mA
			15	-	-	150	mA
Standby Current (TTL)	I_{SB}	$\overline{CE}$ =$V_{IH,}$ other pins =V_{IL} or V_{IH},		-	-	30	mA
Standby Current (CMOS)	I_{SB1}	$\overline{CE}$ =V_{CC}-0.2V, other pins at 0.2V or Vcc-0.2V,		-	-	10	mA

CAPACITANCE (TA=25℃, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	6	pF
Input/Output Capacitance	$C_{I/O}$	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 30pF, I_{OH}/I_{OL} = -4mA / 8mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} =3.0V~3.6V, TA =0℃ to 70℃)

(1) READ CYCLE

PARAMETER	SYMBOL	UT61L6416 -8		UT61L6416 -10		UT61L6416 -12		UT61L6416 -15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	8	-	10	-	12	-	15	-	ns
Address Access Time	t_{AA}	-	8	-	10	-	12	-	15	ns
Chip Enable Access Time	t_{ACE}	-	8	-	10	-	12	-	15	ns
Output Enable Access Time	t_{OE}	-	4	-	5	-	6	-	7	ns
Chip Enable to Output in Low Z	t_{CLZ*}	3	-	3	-	3	-	3	-	ns
Output Enable to Output in Low Z	t_{OLZ*}	0	-	0	-	0	-	0	-	ns
Chip Disable to Output in High Z	t_{CHZ*}	-	4	-	5	-	6	-	7	ns
Output Disable to Output in High Z	t_{OHZ*}	-	4	-	5	-	6	-	7	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	3	-	ns
$\overline{LB}$, $\overline{UB}$ Access Time	t_{BA}	-	4	-	5	-	6	-	7	ns
$\overline{LB}$, $\overline{UB}$ to High-Z Output	t_{BHZ}	-	4	-	5	-	6	-	7	ns
$\overline{LB}$, $\overline{UB}$ to Low-Z Output	t_{BLZ}	0	-	0	-	0	-	0	-	ns

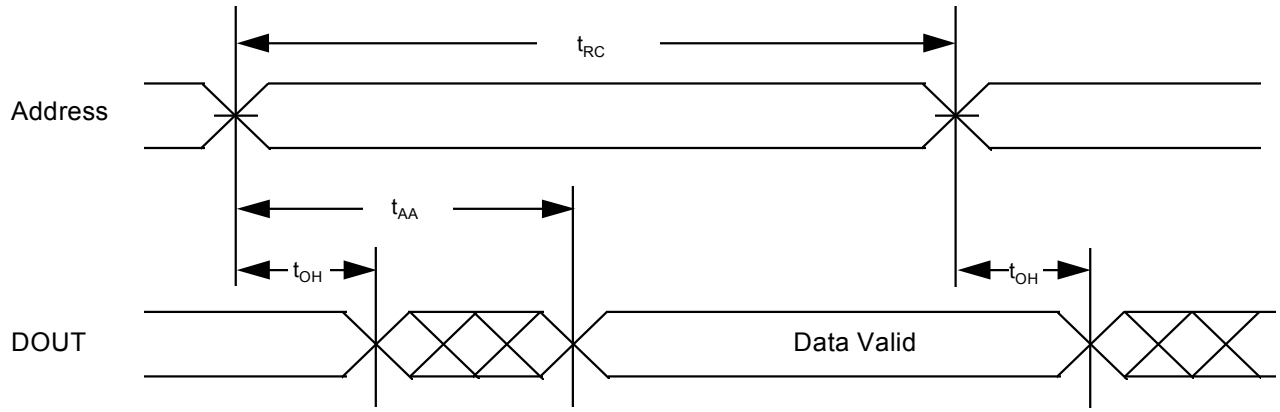
(2) WRITE CYCLE

PARAMETER	SYMBOL	UT61L6416 -8		UT61L6416 -10		UT61L6416 -12		UT61L6416 -15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	8	-	10	-	12	-	15	-	ns
Address Valid to End of Write	t_{AW}	7	-	8	-	9	-	10	-	ns
Chip Enable to End of Write	t_{CW}	7	-	8	-	9	-	10	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	7	-	8	-	9	-	10	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	5.5	-	6	-	7	-	8	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW*}	3	-	3	-	3	-	3	-	ns
Write to Output in High Z	t_{WHZ*}	-	4	-	5	-	6	-	7	ns
$\overline{LB}$, $\overline{UB}$ Valid to End of Write	t_{BW}	7	-	8	-	9	-	10	-	ns

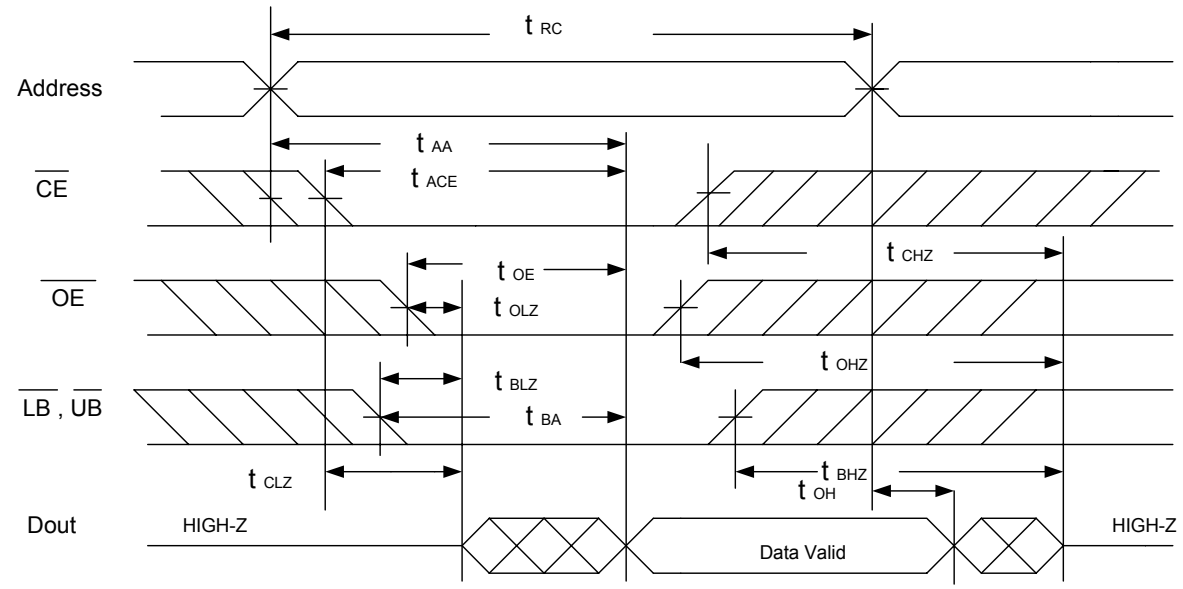
*These parameters are guaranteed by device characterization, but not production tested.
*8ns for Vcc=3.15V~3.6V

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)



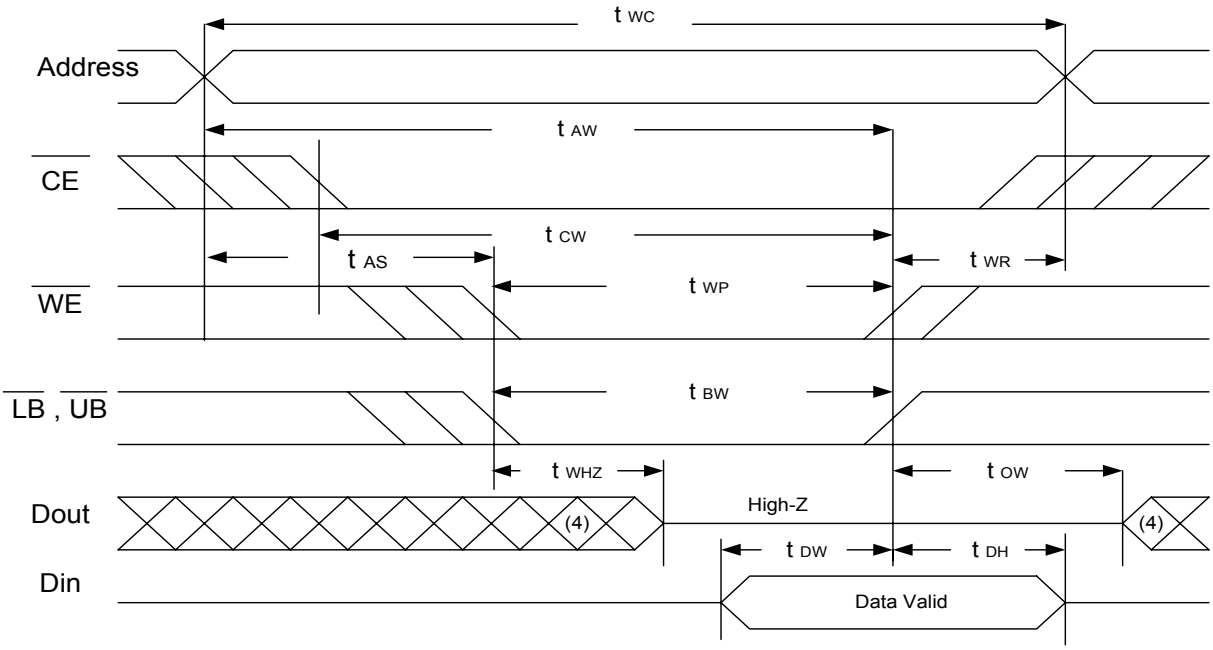
READ CYCLE 2 ($\overline{CE}$ and $\overline{OE}$ Controlled) (1,3,5,6)



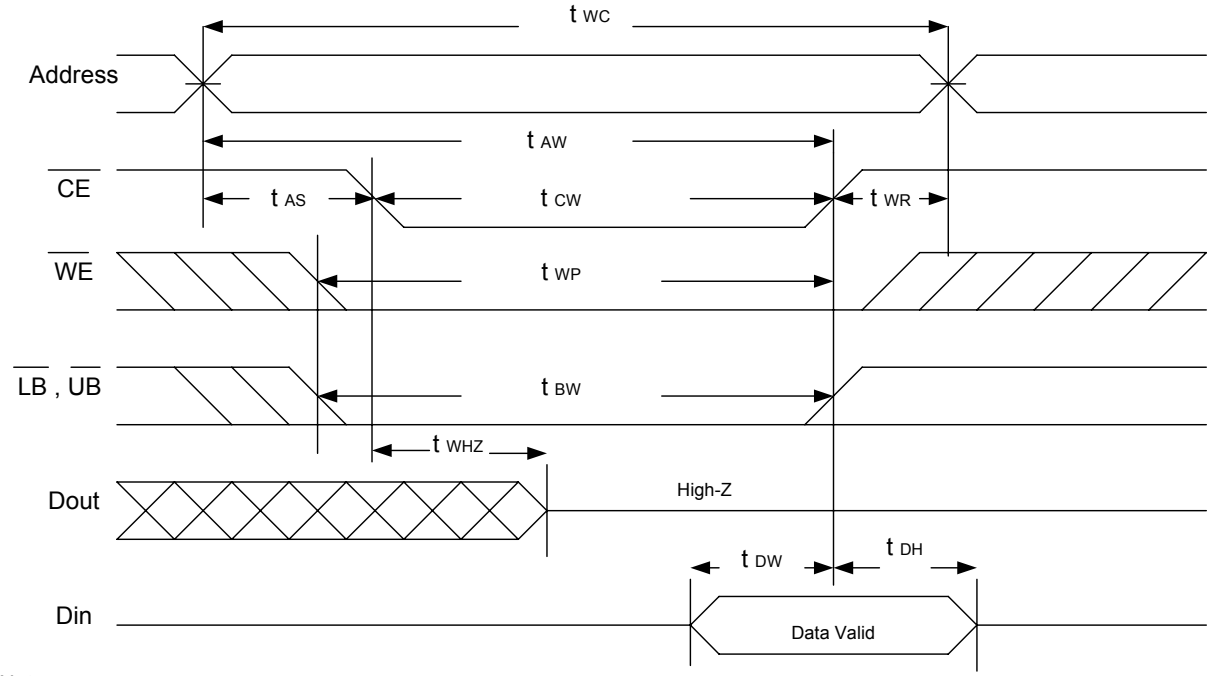
Notes :

1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected $\overline{CE}$ =$V_{IL.}$
3. Address must be valid prior to or coincident with $\overline{CE}$ transition; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. t_{CLZ}, t_{OLZ}, t_{CHZ} , t_{OHZ}, t_{BHZ} and t_{BLZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.
6. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ}, t_{OHZ} is less than $t_{OLZ.}$, t_{BHZ} is less than t_{BLZ}

WRITE CYCLE 1 ($\overline{WE}$ Controlled) (1,2,3,5)



WRITE CYCLE 2 ($\overline{CE}$ Controlled) (1,2,5)

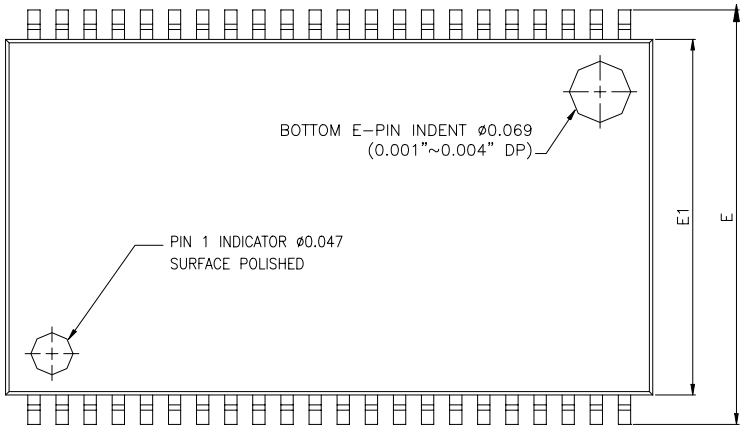


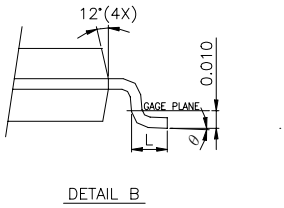
Notes :

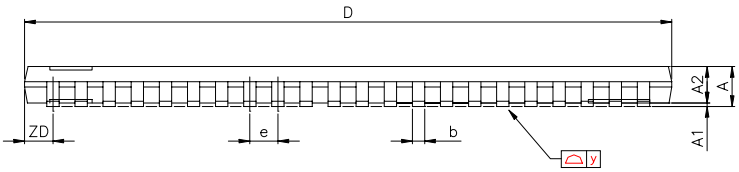
1. $\overline{WE}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of $\overline{CE}$ = low , $\overline{WE}$ =low , $\overline{LB}$ and/or $\overline{UB}$ =low.
3. During a $\overline{WE}$ controlled with write cycle with $\overline{OE}$ LOW, tWP must be greater than tWHZ+tDW to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with CL = 5pF. Transition is measured ±500mV from steady state.

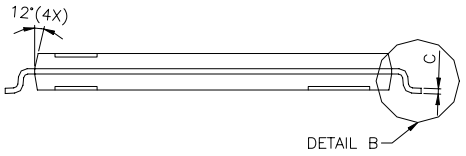
PACKAGE OUTLINE DIMENSION

44 pin 400mil TSOP-Ⅱ PACKAGE OUTLINE DIMENSION









SYMBOLS	DIMENSIONS IN MILLMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX.	MIN.	NOM.	MAX.
A	1.00	-	1.20	0.039	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	0.35	0.45	0.012	0.014	0.018
c	0.12	-	0.21	0.0047	-	0.083
D	18.313	18.415	18.517	0.721	0.725	0.728
E	11.854	11.836	11.838	0.460	0.466	0.470
E1	10.058	10.180	10.282	0.398	0.400	0.404
e	-	0.800	-	-	0.0315	-
L	0.40	0.50	0.60	0.0157	0.020	0.0236
2D	-	0.805	-	-	0.0317	-
y	0.00	-	0.076	0.000	-	0.003
Θ	0°	-	5°	0°	-	5°

ORDERING INFORMATION

COMMERCIAL TEMPERATURE

PART NO.	ACCESS TIME (ns)	PACKAGE
UT61L6416MC-8	8	44 PIN TSOP-Ⅱ
UT61L6416MC-10	10	44 PIN TSOP-Ⅱ
UT61L6416MC-12	12	44 PIN TSOP-Ⅱ
UT61L6416MC-15	15	44 PIN TSOP-Ⅱ

REVISION HISTORY

REVISION	DESCRIPTION	DATE
Preliminary Rev. 0.4	Original.	Mar, 2001
Preliminary Rev. 0.5	1. The symbols CE# and OE# and WE# are revised as. $\overline{CE}$ and $\overline{OE}$ and $\overline{WE}$. 2. Separate Industrial and Commercial SPEC. 3. Add access time 15ns range. 4. Delete SOJ package.	Aug 31,2001