UTRON UT6164C64A

64K X 64 SYNCHRONOUS PIPELINED BURST CMOS SRAM

FEATURES

- Single 3.3V -5% and +10% power supply
- Support 2.5V I/O
- Fast clock access time:
  5ns /100MHz, 6ns /75MHz, 7ns /66Mhz
- 2 clocks chip enable/1 clock chip disable operation
- 5V-tolerant inputs, TTL/LVTTL compatible outputs

- Synchronous pipeline operation
- Internally self-timed WRITE cycle
- BYTE WRITE and GLOBAL WRITE control
- WRITE pass-through capability
- Burst control pin (interleaved or linear burst)
- ZZ snooze mode control
- 128-pin PQFP and TQFP package

GENERAL DESCRIPTION

The UT6164C64A is a 4,194,304-bit synchronous pipelined burst CMOS SRAM organized as 65,536 words by 64 bits. It is fabricated with high performance and high reliability CMOS technology.

The UT6164C64A integrates 65,536 x 64 SRAM cells with advanced synchronous peripheral circuitry and a 2-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include addresses, data inputs, address-pipelining chip enable (CE#), burst control inputs (ADSC#, ADSP#, and ADV#), write enables (BW1#, BW2#, BW3#, BW4#, BW5#, BW6#, BW7#, BW8# and BWE#), and global write (GW#). Asynchronous inputs include the output enable (OE#). The data outputs (I/O), enabled by OE#, are also asynchronous. Addresses and chip enables are registered with either address status processor (ADSP#) or address status controller (ADSC#) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV#). Address, data inputs, and wire controls are registered on-chip to initiate self-timed WRITE cycle. WRITE cycles can be one to four bytes wide as controlled by the write control inputs. Individual byte write allows individual byte to be written. BW1# controls I/O1-I/O8. BW2# controls I/O9-I/O16. BW3# controls I/O17-I/O24. BW4# controls I/O25-I/O32. BW5# controls I/O33-I/O40. BW6# controls I/O41-I/O48. BW7# controls I/O49-I/O56. BW8# controls I/O57-I/O64. BW1#, BW2#, BW3#, BW4#, BW5#, BW6#, BW7# and BW8# can be active only with BWE# being LOW. GW# being LOW causes all bytes to be written. WRITE pass-through capability allows written data available at the output for the immediately next READ cycle. This device also incorporates pipelined enable circuit for easy depth expansion without penalizing system performance.

The UT6164C64A operates from a +3.3V power supply. All inputs and outputs are TTL-compatible. The devise is ideally suited for 486, Pentium^{TM}, 680X0, and PowerPC systems and for systems that are benefited from a wide synchronous data bus.

FUNCTIONAL BLOCK DIAGRAM

REV. 1.1
March 1998

UTRON   UT6164C64A
64K X 64 SYNCHRONOUS PIPELINED BURST CMOS SRAM

PIN CONFIGURATION

UT6164C64A

Top side pins (left to right, 128–103):
VCCQ(128), NC(127), CE2(126), NC(125), CE3#(124), VSS(123), VCC(122), CE1#(121), BW8#(120), BW7#(119), BW6#(118), BW5#(117), OE#(116), CLK(115), BWE#(114), GW#(113), BW4#(112), BW3#(111), VSS(110), VCC(109), BW2#(108), BW1#(107), ADSC#(106), ADSP#(105), ADV/#(104), VSSQ(103)

Left side pins (top to bottom):
VSSQ(1), I/O33(2), I/O34(3), I/O35(4), I/O36(5), I/O37(6), I/O38(7), I/O39(8), I/O40(9), I/O41(10), I/O42(11), I/O43(12), VCCQ(13), VSSQ(14), I/O44(15), I/O45(16), I/O46(17), I/O47(18), I/O48(19), I/O49(20), I/O50(21), I/O51(22), I/O52(23), I/O53(24), VCCQ(25), VSSQ(26), I/O54(27), I/O55(28), I/O56(29), I/O57(30), I/O58(31), I/O59(32), I/O60(33), I/O61(34), I/O62(35), I/O63(36), I/O64(37), VCCQ(38)

Bottom side pins (left to right, 39–64):
VSSQ(39), NC(40), MODE(41), A15(42), A14(43), A13(44), VCC(45), VSS(46), A12(47), A11(48), A10(49), A9(50), A8(51), NC(52), A7(53), A6(54), A5(55), A4(56), A3(57), VCC(58), VSS(59), A2(60), A1(61), A0(62), ZZ(63), VCCQ(64)

Right side pins (top to bottom):
VCCQ(102), I/O32(101), I/O31(100), I/O30(99), I/O29(98), I/O28(97), I/O27(96), I/O26(95), I/O25(94), I/O24(93), I/O23(92), I/O22(91), VSSQ(90), VCCQ(89), I/O21(88), I/O20(87), I/O19(86), I/O18(85), I/O17(84), I/O16(83), I/O15(82), I/O14(81), I/O13(80), I/O12(79), VSSQ(78), VCCQ(77), I/O11(76), I/O10(75), I/O9(74), I/O8(73), I/O7(72), I/O6(71), I/O5(70), I/O4(69), I/O3(68), I/O2(67), I/O1(66), VSSQ(65)

3

REV. 1.1
March 1998

PIN DESCRIPTION

PIN NO.	SYMBOL	DESCRIPTION
42-44, 47-51, 53-57, 60-62	A0 - A15	Address Inputs
115	CLK	Clock
105	ADSP#	Address Status Processor
106	ADSC#	Address Status Control
104	ADV#	Address Advance
121, 126, 124	CE1#, CE2, CE3#	Chip Enable
116	OE#	Output Enable
113	GW#	Global Write
114, 107-108, 111-112, 117-120	BWE#, BW1# - BW8#	Byte Write Enable
41	MODE	Burst Mode
63	ZZ	Snooze
66-76, 79-88, 91-101, 2-12, 15-24, 27-37	I/O1-I/O64	Data Inputs/Outputs
45, 58, 109, 122	VCC	Power Supply
46, 59, 110, 123	VSS	Ground
13, 25, 38, 64, 77, 89, 102, 128	VCCQ	Output Buffer Supply (For 2.5V I/O : 2.4V to VCC)
1, 14, 26, 39, 65, 78, 90, 103	VSSQ	Output Buffer Ground
40, 52, 125, 127	NC	No Connection

REV. 1.1
March 1998

TRUTH TABLE

OPERATION	ADDRESS USED	CE1#	CE2	CE3#	ADSP#	ADSC#	ADV#	WRITE#	OE#	CLK	I/O
Deselected Cycle. Power Down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle. Power Down	None	L	L	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle. Power Down	None	L	X	H	L	X	X	X	X	L-H	High-Z
Deselected Cycle. Power Down	None	L	L	X	H	L	X	X	X	L-H	High-Z
Deselected Cycle. Power Down	None	L	X	H	H	L	X	X	X	L-H	High-Z
READ Cycle. Begin Burst	External	L	H	L	L	X	X	X	L	L-H	Q
READ Cycle. Begin Burst	External	L	H	L	L	X	X	X	H	L-H	High-Z
WRITE Cycle. Begin Burst	External	L	H	L	H	L	X	L	X	L-H	D
READ Cycle. Begin Burst	External	L	H	L	H	L	X	H	L	L-H	Q
READ Cycle. Begin Burst	External	L	H	L	H	L	X	H	H	L-H	High-Z
READ Cycle. Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Q
READ Cycle. Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle. Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Q
READ Cycle. Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle. Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	D
WRITE Cycle. Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	D
READ Cycle. Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Q
READ Cycle. Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle. Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Q
READ Cycle. Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle. Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	D
WRITE Cycle. Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	D

Note: 1.X means "don't care." H means logic HIGH. L means logic LOW. WRITE = L means [BWE# + BW1# * BW2# *
   BW3# * BW4# * BW5# * BW6# * BW7# * BW8#] * GW# equals LOW. WRITE = H means [BWE# + BW1# * BW2# *
   BW3# * BW4# * BW5# * BW6# * BW7# * BW8#] * GW# equals HIGH.
   2.BW1# enables write to I/O1-I/O8.   BW2# enables write to I/O9-I/O16.   BW3# enables write to I/O17-I/O24.
   BW4# enables write to I/O25-I/O32. BW5# enables write to I/O33-I/O40. BW6# enables write to I/O41-I/O48.
BW7#
   enables write to I/O49-I/O56. BW8# enables write to I/O57-I/O64.
   3.All inputs except OE# must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
   4.Suspending burst generates wait cycle.
   5. For a write operation following a read operation. OE# must be high before the input data required setup time
   plus High-Z time for OE# and staying HIGH throughout the input data hold time.
   6.This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
   7.ADSP# LOW along with chip being selected always initiates a READ cycle at the L-H edge of CLK.   A WRITE
   cycle can be performed by setting WRITE LOW for the CLK L-H edge of the subsequent wait cycle. Refer to
   WRITE timing diagram for clarification.

PARTIAL TRUTH TABLE FOR WRITE

FUNCTION	GW#	BWE#	BW1#	BW2#	BW3#	BW4#	BW5#	BW6#	BW7#	BW8#
READ	H	H	X	X	X	X	X	X	X	X
READ	H	L	H	H	H	H	H	H	H	H
WRITE one byte	H	L	L	H	H	H	H	H	H	H
WRITE all bytes	H	L	L	L	L	L	L	L	L	L
WRITE all bytes	L	X	X	X	X	X	X	X	X	X

REV. 1.1
March 1998

INTERLEAVED BURST ADDRESS TABLE (MODE=NC/Vcc)

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A00	A...A11	A...A10
A...A10	A...A11	A...A00	A...A01
A...A11	A...A10	A...A01	A...A00

LINEAR BURST ADDERSS TABLE (MODE=GND)

FIRST ADDRESS (EXTERNAL)	SECOND ADDRESS (INTERNAL)	THIRD ADDRESS (INTERNAL)	FOURTH ADDRESS (INTERNAL)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A10	A...A11	A...A00
A...A10	A...A11	A...A00	A...A01
A...A11	A...A00	A...A01	A...A10

PASS-THROUGH TRUTH TABLE

PREVIOUS CYCLE		PRESENT CYCLE				NEXT CYCLE
OPERATION	BWN#	OPERATION	CE#	BWN#	OE#	OPERATION
Initiate WRITE cycle, all bytes Address=A(n-1). data=D(n-1)	All L[2, 3]	READ cycle. Register A(n). Q=D(n-1)	L	H	L	Read D(n)
Initiate WRITE cycle, all bytes Address=A(n-1). data=D(n-1)	All L[2, 3]	READ cycle. Register A(n). Q=HIGH-Z	L	H	H	Read D(n)
Initiate WRITE cycle, one byte Address=A(n-1). data=D(n-1)	One L[2, 3]	READ cycle. Register A(n). Q=D(n-1) for one byte	L	H	L	Read D(n)
Initiate WRITE cycle, all bytes Address=A(n-1). data=D(n-1)	All L[2]	Deselect cycle Q=HIGH-Z	H	X	X	No carry-over from previous cycle

Note: 1. Previous cycle may be any cycle (non-burst, burst, or wait) and next cycle is read cycle (non-burst, burst, or wait).
　　　2. BWE# is LOW for individual byte WRITE.
　　　3. GW# LOW yields the same result for all-byte WRITE operation.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	RATING	UNIT
Voltage on Vcc Supply Relative to Vss	-0.5 to +4.6	V
V_{IN}	-0.5 to +6	V
Storage Temperature (plastic)	-55 to +150	℃
Junction Temperature	+150	℃
Power Dissipation	1.6	W
Short Circuit Output Current	100	mA

*Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

REV. 1.1
March 1998

UTRON UT6164C64A
64K X 64 SYNCHRONOUS PIPELINED BURST CMOS SRAM

_____

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.3V -5% and +10%, T_A = 0℃ to 70℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT	NOTES
Input High (Logic 1) Voltage	V_{IH}		2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage	V_{IL}		- 0.3	0.8	V	1, 2
Input Leakage Current	IL_I	$0V \leq V_{IN} \leq V_{CC}$	- 1	1	μA	14
Output Leakage Current	IL_O	Output(s) disabled. $0V \leq V_{OUT} \leq V_{CC}$	- 1	1	μA	
Output High Voltage (3.3V I/O)	V_{OH}	I_{OH}= - 4mA	2.4	-	V	1, 11
Output Low Voltage	V_{OL}	I_{OL} = 8mA	-	0.4	V	1, 11
Supply Voltage	V_{CC}		3.1	3.6	V	1
I/O Supply Voltage (3.3V I/O)	V_{CCQ}		3.1	3.6	V	1
I/O Supply Voltage (2.5V I/O)	V_{CCQ}		2.4	3.6	V	1

DESCRIPTION	CONDITIONS	SYM	TYP	-5ns	-6ns	-7ns	UNIT	NOTES
Power Supply Current Operating	Device selected: all inputs $\leq V_{IL}$ or $\geq$ V_{IH} cycle time $\geq t_{KC}$ MIN; V_{CC}=MAX; outputs open	I_{CC}	180	360	315	270	mA	3, 12, 13
Power Supply Current Idle	Device selected: ADSC#, ADSP#, ADV#, GW#, BWE# $\geq V_{IH}$, all other inputs $\leq V_{IL}$ or $\geq V_{IH}$ V_{CC}=MAX; cycle time $\geq t_{KC}$ MIN; outputs open	I_{SB1}	30	60	55	50	mA	12, 13
CMOS Standby	Device selected: V_{CC}=MAX; all inputs $\leq V_{SS}$+0.2 or $\geq V_{CC}$-0.2; all inputs static; CLK frequency = 0	I_{SB2}	2	20	20	20	mA	12, 13
TTL Standby	Device selected: all inputs $\leq V_{IL}$ or $\geq V_{IH}$ all inputs static; V_{CC}=MAX; CLK frequency = 0	I_{SB3}	15	40	40	40	mA	12, 13
Clock Running	Device selected: all inputs $\leq V_{IL}$ or $\geq V_{IH}$; V_{CC}=MAX; CLK cycle time $\geq t_{KC}$ MIN	I_{SB4}	30	60	55	50	mA	12, 13
Power-Down Mode Current	ZZ $\geq V_{CC}$ - 0.2	I_{ZZ}	1	10	10	10	mA	12, 13

CAPACITANCE (T_A = 25℃, f = 1MHz)

PARAMETER	SYMBOL	TYP.	MAX.	UNIT	NOTES
Input Capacitance	C_{IN}	3	4	pF	4
Input/Output Capacitance	$C_{I/O}$	6	7	pF	4

_____

REV. 1.1
March 1998

64K X 64 SYNCHRONOUS PIPELINED BURST CMOS SRAM

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.3V -5% and +10%, T_A = 0℃ to 70℃)

PARAMETER	SYM	-5 MIN	MAX	-6 MIN	MAX	-7 MIN	MAX	UNITS	NOTES
Clock									
Clock cycle time	t_{KC}	10	-	12	-	15	-	ns	-
Clock HIGH time	t_{KH}	4	-	4	-	5	-	ns	-
Clock LOW time	t_{KL}	4	-	4	-	5	-	ns	-
Output Times									
Clock to output valid	t_{KO}	-	5	-	6	-	7	ns	-
Clock to output invalid	t_{KOX}	2	-	2	-	2	-	ns	-
Clock to output in Low-Z	t_{KOZ}	3	-	3	-	3	-	ns	6, 7
Clock to output in High-Z	t_{KOHZ}	-	5	-	5	-	6	ns	6, 7
OE# to output valid	t_{OEO}	-	5	-	5	-	5	ns	9
OE# to output in Low-Z	t_{OELZ}	0	-	0	-	0	-	ns	6, 7
OE# to output in High-Z	t_{OEHZ}	-	4	-	5	-	6	ns	6, 7
Setup Times									
Address setup	t_{AS}	2.2	-	2.5	-	2.5	-	ns	10
Address status setup	t_{ADSS}	2.2	-	2.5	-	2.5	-	ns	10
Address advance setup	t_{ADVS}	2.2	-	2.5	-	2.5	-	ns	10
Write setup	t_{WS}	2.2	-	2.5	-	2.5	-	ns	10
Data setup	t_{DS}	2.2	-	2.5	-	2.5	-	ns	10
Chip enable setup	t_{CES}	2.2	-	2.5	-	2.5	-	ns	10
Hold Times									
Address status hold	t_{ADSH}	0.5	-	0.5	-	0.5	-	ns	10
Address advance hold	t_{ADVH}	0.5	-	0.5	-	0.5	-	ns	10
Write hold	t_{WH}	0.5	-	0.5	-	0.5	-	ns	10
Data hold	t_{DH}	0.5	-	0.5	-	0.5	-	ns	10
Chip enable hold	t_{CEH}	0.5	-	0.5	-	0.5	-	ns	10
ZZ stand by	t_{ZZS}	-	100	-	100	-	100	ns	16
ZZ recovery	t_{ZZREC}	100	-	100	-	100	-	ns	16

AC TEST CONDITIONS

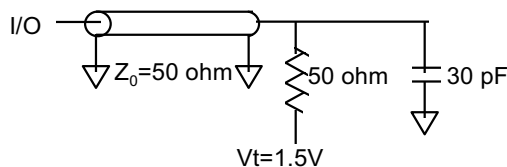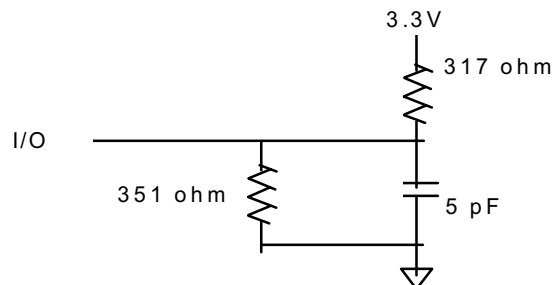| Input pulse levels	0V to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

OUTPUT LOADS

Fig.1 Output Load Equivalent

Fig.2 Output Load Equivalent

REV. 1.1
March 1998

NOTES:

1. All voltages referenced to Vss(GND).
2. Overshoot: $V_{IH} \leq V_{CC} + 0.6V$ for $t \leq t_{KC}/2$.
   Undershoot: $V_{IL} \leq Vss - 0.7V$ for $t \leq t_{KC}/2$.
3. I_{CC} is given with no output current. I_{CC} increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with $C_L=5pF$ as in Fig. 2.
7. At any given temperature and voltage condition. t_{KQHZ} is less than t_{KQLZ} and t_{OEHZ} is less than t_{OELZ}.
8. A READ cycle is defined by byte write enables all HIGH or ADSP# LOW along with chip enables being active for the required setup and hold times. A WRITE cycle is defined by at one byte or all byte WRITE per READ/WRITE TRUTH TABLE.
9. OE# is a "don't care" when a byte write enable is sampled LOW.
10. This is a synchronous device. All synchronous inputs must meet specified setup and hold time, except for "don't care" as defined in the truth table.
11. AC I/O curves are available upon request.
12. "Device Deselected" means the device is in POWER-DOWN mode as defined in the truth table. "Device Selected" means the device is active.
13. Typical values are measured at 3.3V, 25℃ and 20ns cycle time.
14. Capacitance derating applies to capacitance different from the load capacitance shown in Fig. 1.
15. Capacitance derating applies to capacitance different from the load capacitance shown in Fig. 1.
16. The assertion off ZZ allows the SRAM to enter a low power state than when deselected within the time specified.
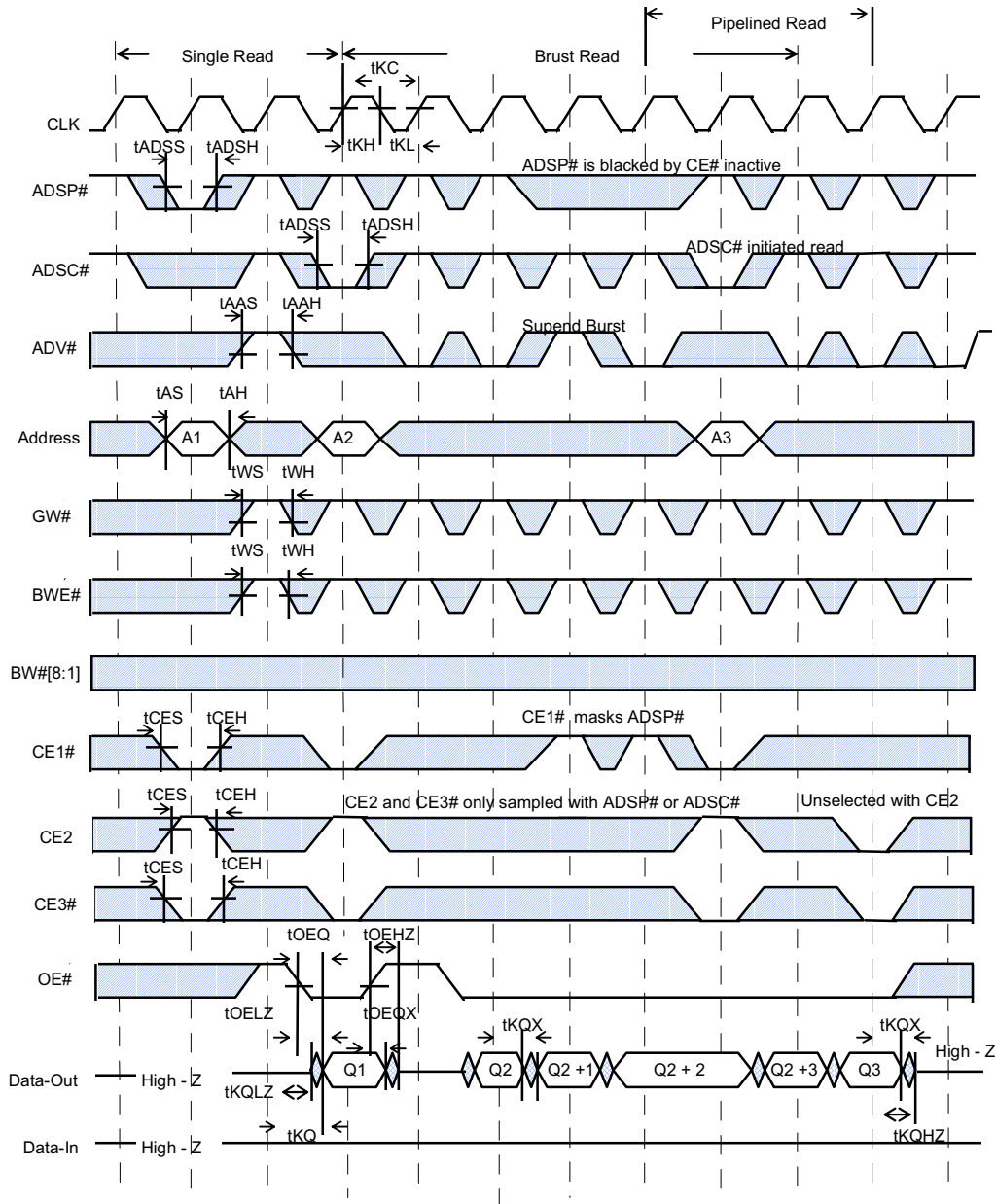
REV. 1.1
March 1998

TIMING WAVEFORMS

READ CYCLE

UTRON TECHNOLOGY INC.
1F, No. 11, R&D Rd. II, Science-Based Industrial Park, Hsinchu, Taiwan, R. O. C.
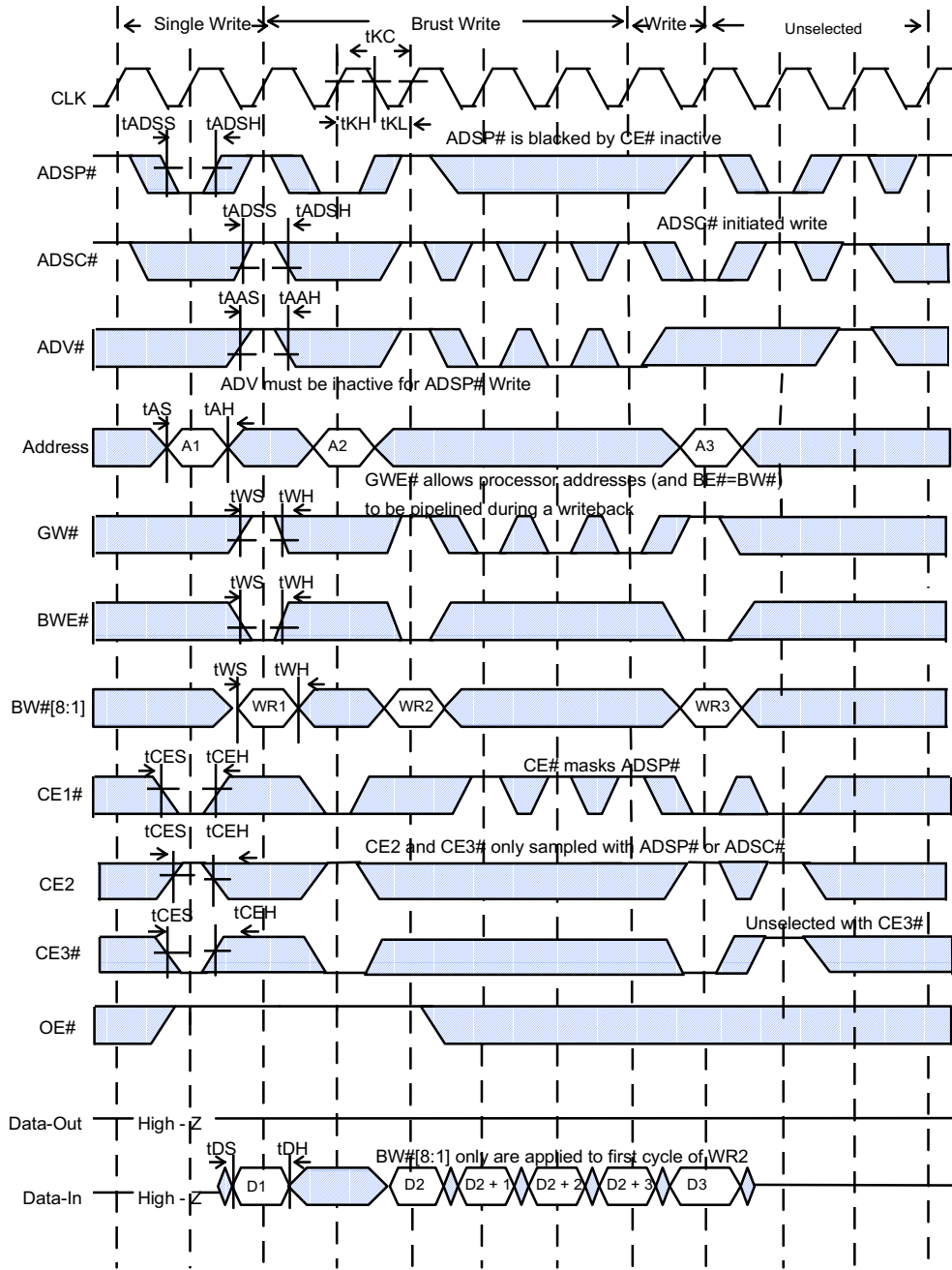TEL: 886-3-5777882   FAX: 886-3-5777919

REV. 1.1
March 1998

WRITE CYCLE

READ / WRITE CYCLE

REV. 1.1
March 1998
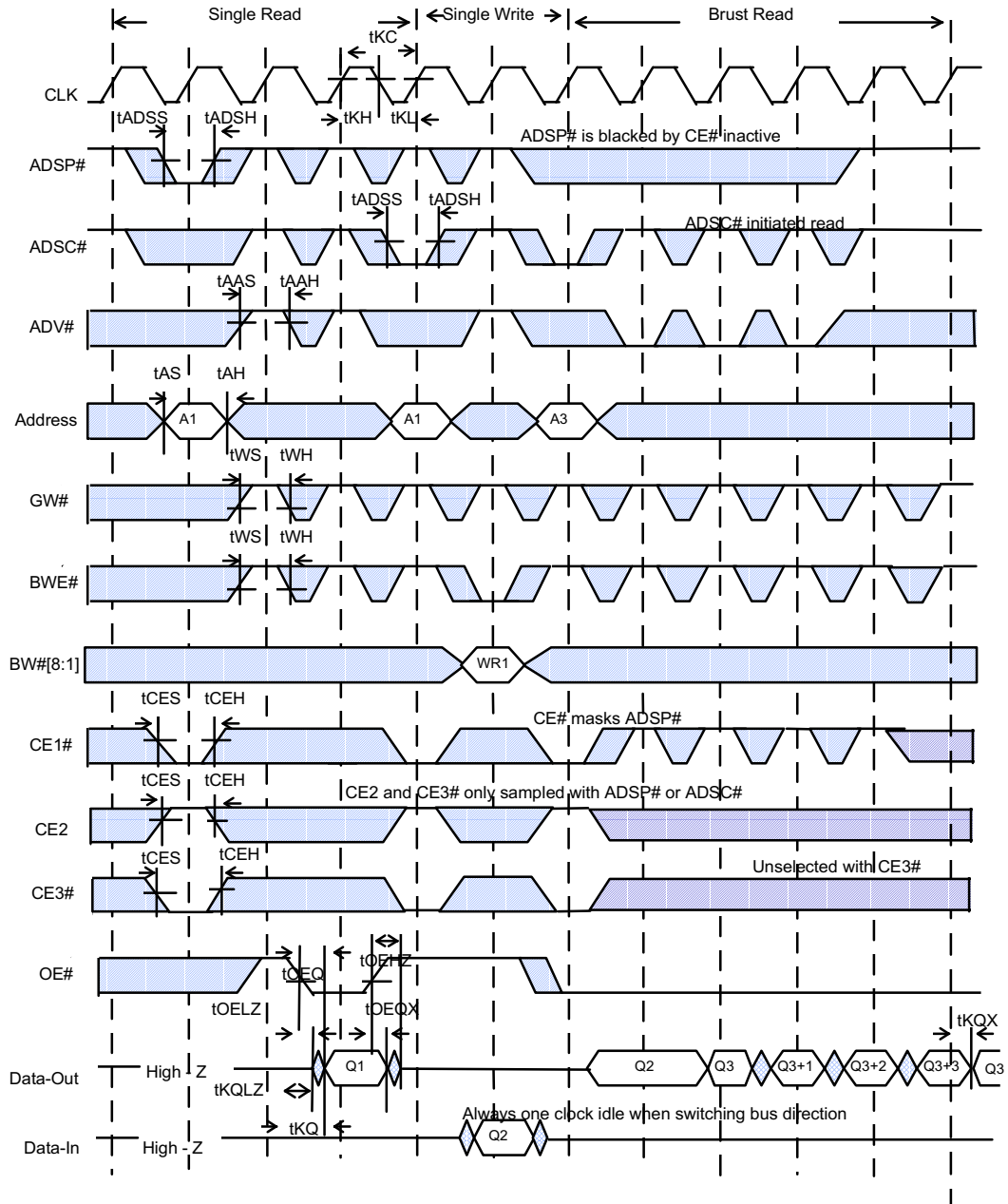
ZZ TIMING
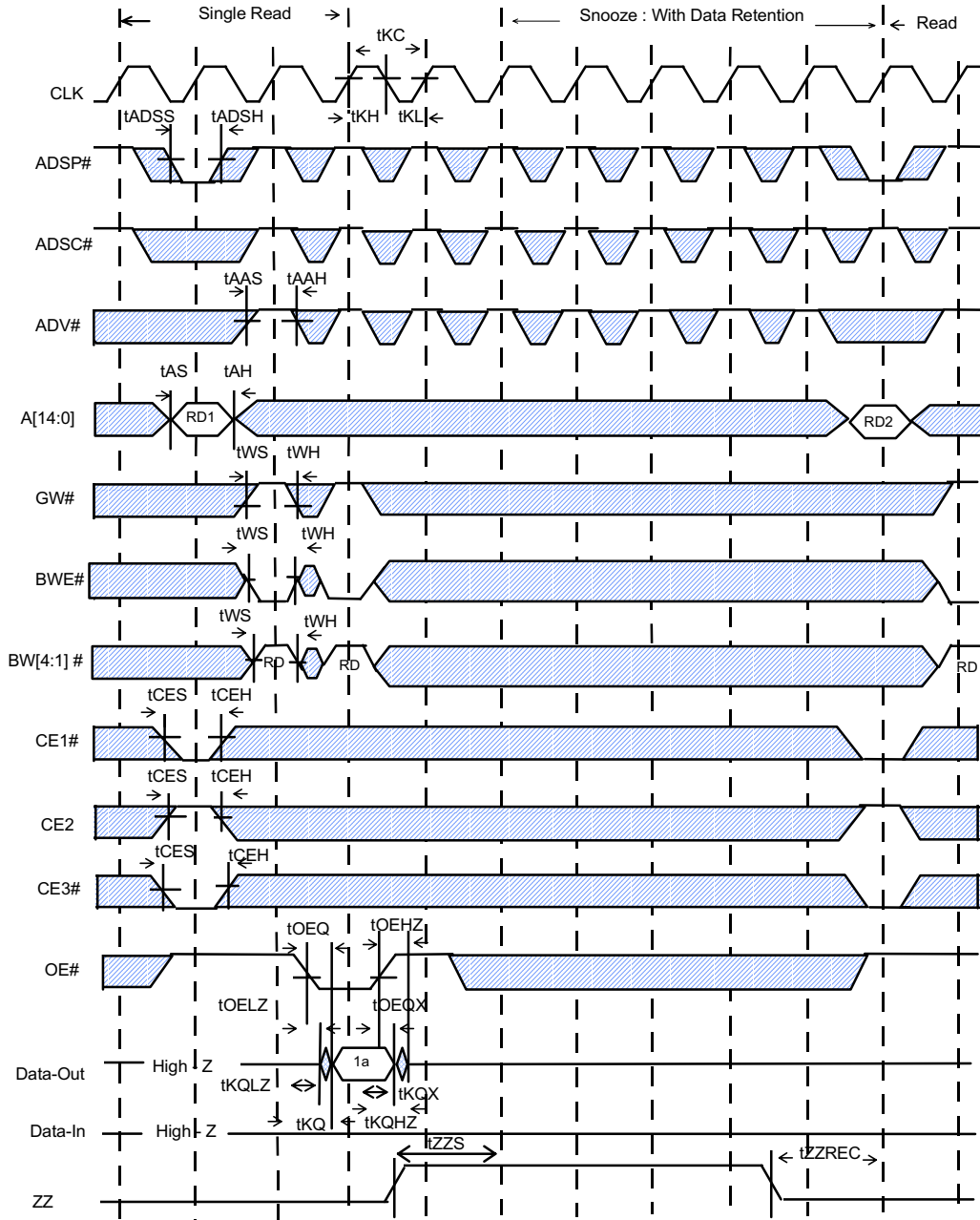
PACKAGE OUTLINE DIMENSION

128 QFP Package Outline Dimension
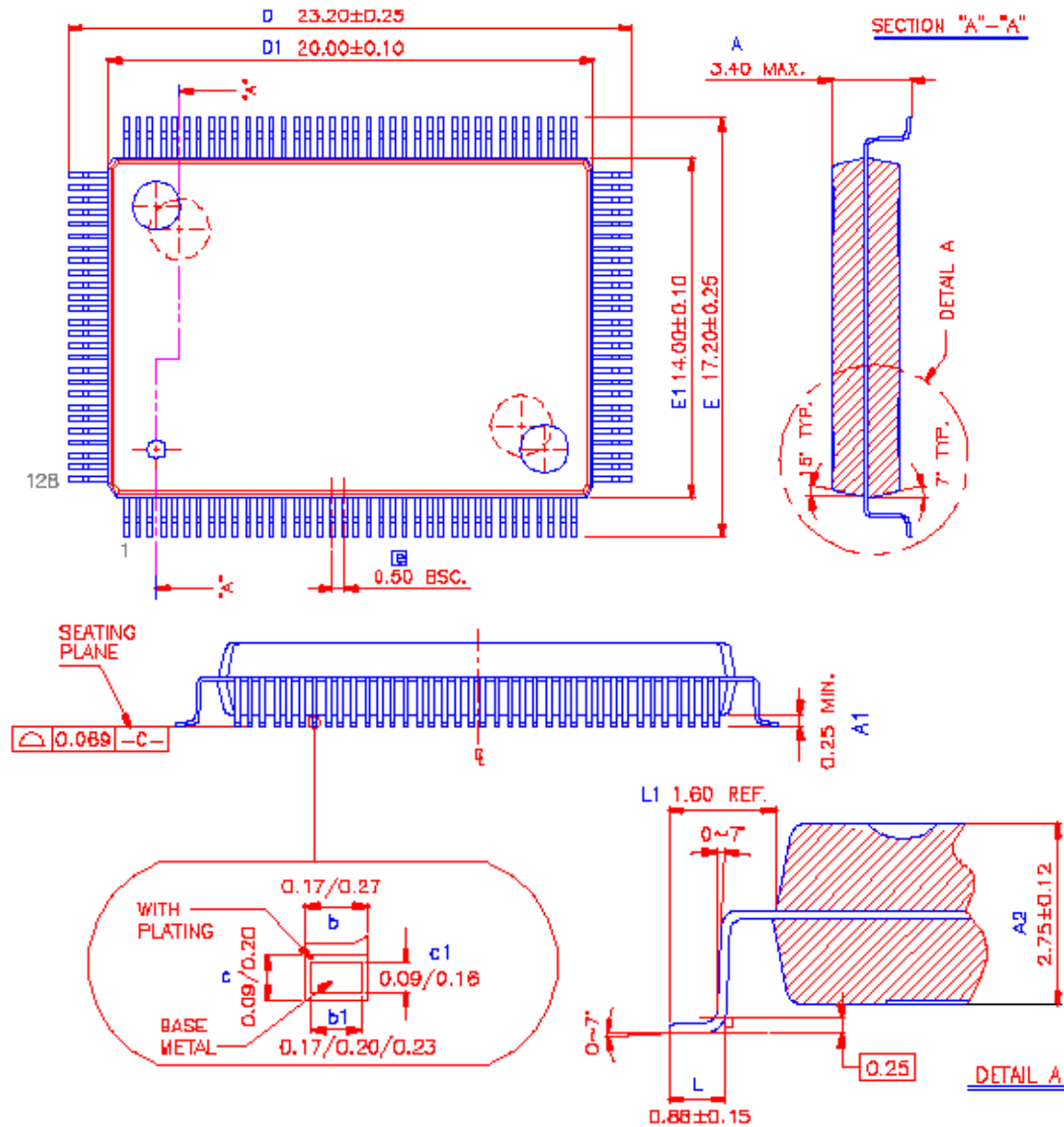
NOTE:
1. CONTROLLING DIMENSION ARE IN MILLMETERS(mm).
2. DIMENSION D1& D2 DOES NOT INCLUDE MOLD PROTRUSION.
3. COPLANARITY OF ALL LEADS SHALL BE 2.7 MILS MAX.
   (BEFORE TEST) FROM THE SEATING PLANE.
   UNLESS OTHERWISE SPECIFIED.
4. GENERAL PHYSICAL OUTLIN

REV. 1.1
March 1998

ORDERING INFORMAITON

PART NO.	ACCESS TIMES (ns)	PACKAGE
UT6164C64AQ-5	5	128 PIN PQFP
UT6164C64AT-5	5	128 PIN TQFP
UT6164C64AQ-6	6	128 PIN PQFP
UT6164C64AT-6	6	128 PIN TQFP

REV. 1.1
March 1998