



## 3.3V Low Phase Noise Clock Multiplier

## Applications

- Oscillator Replacement
- LCD monitor clock source

## General Description

The VT98521 is a 3.3V CMOS, clock multiplier integrated circuit. The device provides an excellent quality high frequency output clock from a lower frequency crystal or clock input. Tri-level selection inputs S0 and S1 are used to select any one of eight multipliers, stored in the on-board ROM, and apply it to the input to produce the desired output. The resulting output includes many commonly used frequencies up to 160 MHz. Phase Locked Loop (PLL) technology allows the device to use an input signal from an inexpensive crystal.

When Output Enable (OE) is low, the clock output is in high impedance state.

The VT98521, when used with an inexpensive crystal, provides a cost-effective clock source for most electronic systems.

## Features

- Low phase noise
- Zero ppm multiplication error
- Input clock frequency 2 - 50 MHz.
- Input crystal frequency 5 – 27 MHz
- Output clock frequencies up to 160 MHz.
- 5V-tolerant inputs and output
- Exceptionally low jitter: 25 ps one sigma
- Fully Compatible with all popular CPUs
- Duty Cycle of 45/55 up to 160 MHz.
- 25mA drive capability at TTL levels
- High-Z output for board level testing

Figure 1. Functional Block Diagram

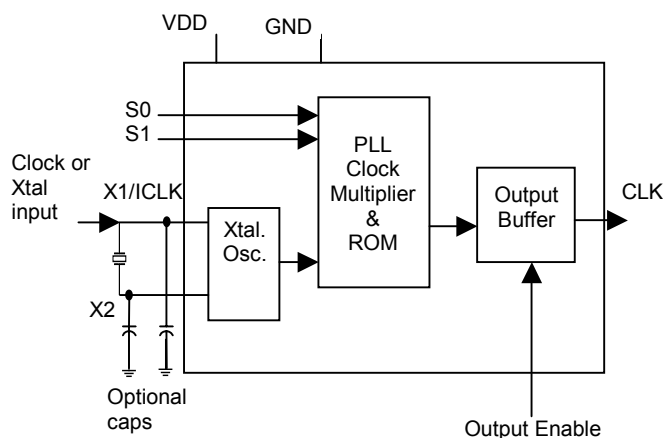
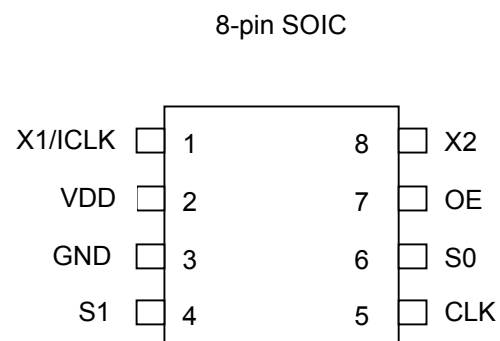


Figure 2. Pin Assignment



**Table 1. Clock Output Table**

S1	S0	CLK	Minimum Input
0	0	4 x input	See table 7
0	M	5.3125 x input	20 MHz
0	1	5 x input	See table 7
M	0	6.25 x input	4 MHz
M	M	Test*	
M	1	3.125 x input	8 MHz
1	0	6 x input	See table 7
1	M	3 x input	See table 7
1	1	8 x input	See table 7

0 = Connect to ground.

1 = Connect directly to VDD

M = Leave unconnected (floating)

\* = For Vaishali internal test purposes only

**Table 2. Examples of Common Output Frequencies.**

Output	20	24	30
Input	10	12	10
Selection (S1,S0)	M,M	M,M	1,M

Output	50	60	62.5	64	66.66	72	75	80
Input	16.66	10	20	16	16.66	12	12	10
Selection (S1,S0)	1,M	1,0	M,1	0,0	0,0	1,0	M,0	1,1

Output	83.33	90	100	106.25	120	125	155.52
Input	16.66	15	20	20	15	20	19.44
Selection (S1,S0)	0,1	1,0	0,1	0,M	1,1	M,0	1,1

**Table 3. Pin Description**

No.	Name	Type	Description
1	X1/ICLK	I	Xtal connection or clock input.
2	VDD	P	Connect to +3.3V
3	GND	P	Connect to ground.
4	S1	TI	Select 1 for output clock. Connect to ground or VDD or float
5	CLK	O	Clock output per table 2.
6	S0	TI	Select 0 for output clock. Connect to ground or VDD or float.
7	OE	I	Output Enable. Tri- states CLK output when low.
8	X2	O	Xtal connection. Leave unconnected for clock input.

Legend:

I = Input

TI = Tri-level Input

O = Output

P = Power supply connection

**Table 4. Absolute Maximum Ratings**

Parameter	Conditions	Min	Typ	Max	Units
Supply voltage, VDD	Referenced to GND			4.6	V
Inputs and Clock Outputs	Referenced to GND	-0.5		4.6	V
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C

**Table 5. Operating Conditions**

Parameter	Min	Typ	Max	Units
Ambient Operating Temperature	0		70	°C
Operating Voltage, VDD	3		3.6	V
Input High Voltage, $V_{IH}$ , X1 pin only	2.5	1.65		V
Input Low Voltage, $V_{IL}$ , X1 pin only		1.65	0.5	V
Input High Voltage, $V_{IH}$ , OE pin	2			V
Input Low Voltage, $V_{IL}$ , OE pin			0.8	V
Input High Voltage, $V_{IH}$ , trinary inputs	VDD-0.5			V
Input Low Voltage, $V_{IL}$ , trinary inputs			0.5	V

## DC Characteristics

**Table 6. DC Characteristics**

VDD = 3V to 3.6V

Parameter	Condition	Min	Typ	Max	Units
Output High Voltage, $V_{OH}$	$I_{OH}=-25mA$	2.4			V
Output Low Voltage, $V_{OL}$	$I_{OL}=25mA$			0.4	V
Operating Supply Current, $I_{DD}$ (20 MHz Xtal)	No Load, 100MHz		25		mA
Short Circuit Current	CLK output		±100		mA
Input Capacitance	S0, S1, OE		4		pF
Frequency synthesis error				0	ppm

## AC Characteristics

**Table 7. AC Characteristics**

VDD = 3V to 3.6V over the operating temperature range

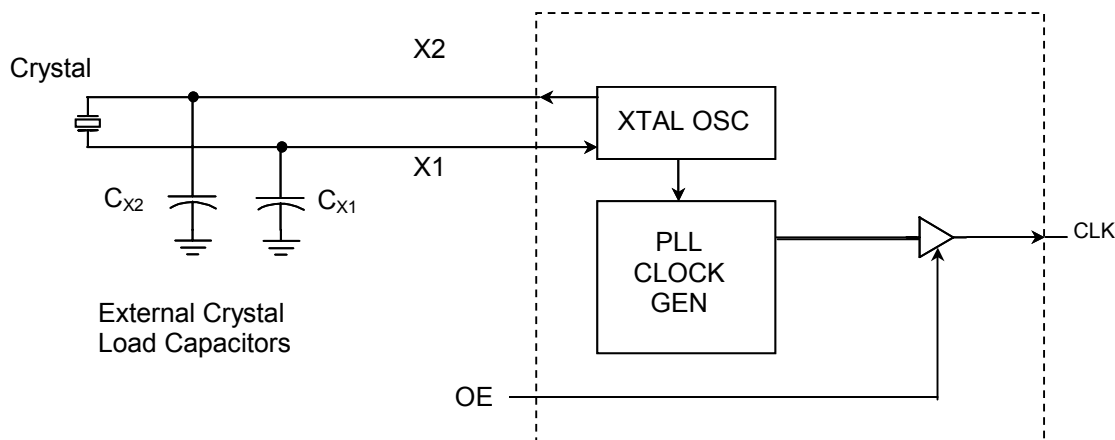
Symbol	Parameter	Condition	Min	Typ	Max	Units
$f_{osc}$	Input Crystal Frequency		5		27	MHz
$f_{in}$	Input clock frequency		2		50	MHz
$f_{out}$	Output Frequency,		14		160	MHz
$t_r$	Output Clock Rise Time	0.8 to 2.0V		1		ns
$t_f$	Output Clock Fall Time	2.0 to 0.8V		1		ns
$t_{od}$	Output Clock Duty Cycle	1.5 V, up to 160 MHz	45	49 to 51	55	%
	PLL Bandwidth		10			kHz
$T_{PZH}, T_{PZL}$	Output Enable Time, OE high to output on				50	ns
$T_{PHZ}, T_{PLZ}$	Output Disable time, OE low to Tri-state				50	ns
$t_{jit} (abs)$	Absolute Clock period Jitter	Deviation from mean		70		ps
$t_{jit} (sigma)$	One Sigma Clock Period Jitter			25		ps

### Note: External Crystal Connection.

The external crystal should be connected in as close physical proximity to the VT98501 as possible. The crystal should be a fundamental mode, parallel resonant. Do not use third overtone. Decoupling capacitors of 0.01  $\mu$ F and 0.1  $\mu$ F should be connected between VDD and Ground. Capacitors should be mounted as close to the chip as possible. A 33 $\Omega$  termination resistor may be mounted in series with the clock output in order to minimize ringing and reflections.

Precision tuning of the crystal can be achieved by connecting a capacitor from pin X1 to ground and another from pin X2 to ground. The value of these capacitors is determined by the crystal load capacitance. The value can be determined using the following equation, where  $C_L$  is the crystal load capacitance. Crystal capacitors (pF) =  $(C_L - 5) \times 2$ . For example, a crystal with a load capacitance of 16 pF should have 22 pF tuning capacitors.

**Figure 3. External Crystal Connection Block Diagram**



### Ordering Information

Part Number	Marking	Shipping/Packaging	No. of Pins	Package	Temperature
VT98521S1	VT98521S1	Tubes	8	SOIC	0°C to +70°C
VT98521S1X	VT98521S1	Tape & Reel	8	SOIC	0°C to +70°C
VT98521/D		Dice in waffle-packs			0°C to +70°C
VT98521/DW		Dice in wafer form			0°C to +70°C