VT86C100A

PCI FAST ETHERNET CONTROLLER

DATA SHEET
(Preliminary)

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VIA TECHNOLOGIES, INC.

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VT86C100A PCI FAST ETHERNET CONTROLLER FEATURES

* Single chip Fast Ethernet controller for PCI bus interface
    -- compliant to PCI v2.1 with optional delay transaction and sub-vendor, sub-system- ID
    -- Provides a direct connection to PCI bus
    -- Supports two network ports : 10/100 M MII interface
* High performance PCI mastering structure
    -- VIA self-define 128 bytes memory I/O or register I/O based command and status register
    -- Software oriented chain structure description to minimize hardware complexity
    -- Include on chip bus master DMA with programmable burst length for low CPU utilization
    -- Dynamic transmit packet auto queuing for back auto queuing for bac for back to back transmissin
    -- Programmable activity polling intervals for description DMA
    -- Programmable DMA arbitration priority to minimize overflow under flow condition
    -- Support early receive and early transmit interrupt for software parallel processing
    -- Interrupt controllable by receive/transmit descriptor list for saving interrupt service time
* Provides standard 100-M bits MII interface
    -- Support 100Base-TX with CAT5 UTP, STP and fiber cables
    -- Support 100Base-T4 with CAT3, CAT4, CAT 5 UTP, STP
* 10/100Mhz full duplex, half duplex operation
* Contains two deeper 2K bytes FIFO for receive and transmit controller both supports bursts of up to full Ethernet length
    -- Programmable receive and transmit FIFO threshold control for optimize PCI throughput
* Flexible dynamically load EEPROM algorithm.
    -- Load after power-up
    -- Dynamic auto reload
    -- Embedded programming for configure modification
    -- Dynamic direct programming for manufacturing
* Support physical, Broadcast, Multicast address filtering using hashing function
* Support Magic packet and wake on address filtering
* Support external Bootrom up to 64K bytes no external address latch
* Software controllable power down feature
* Single +5V supply, 0.5um standard CMOS technology
* 128 pin PQFP package

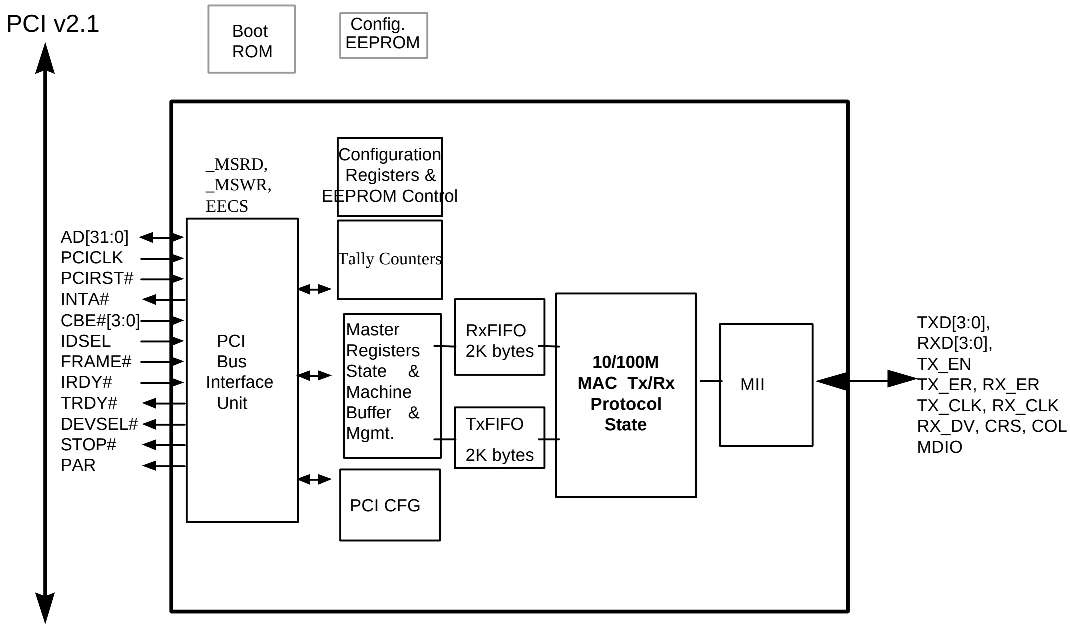
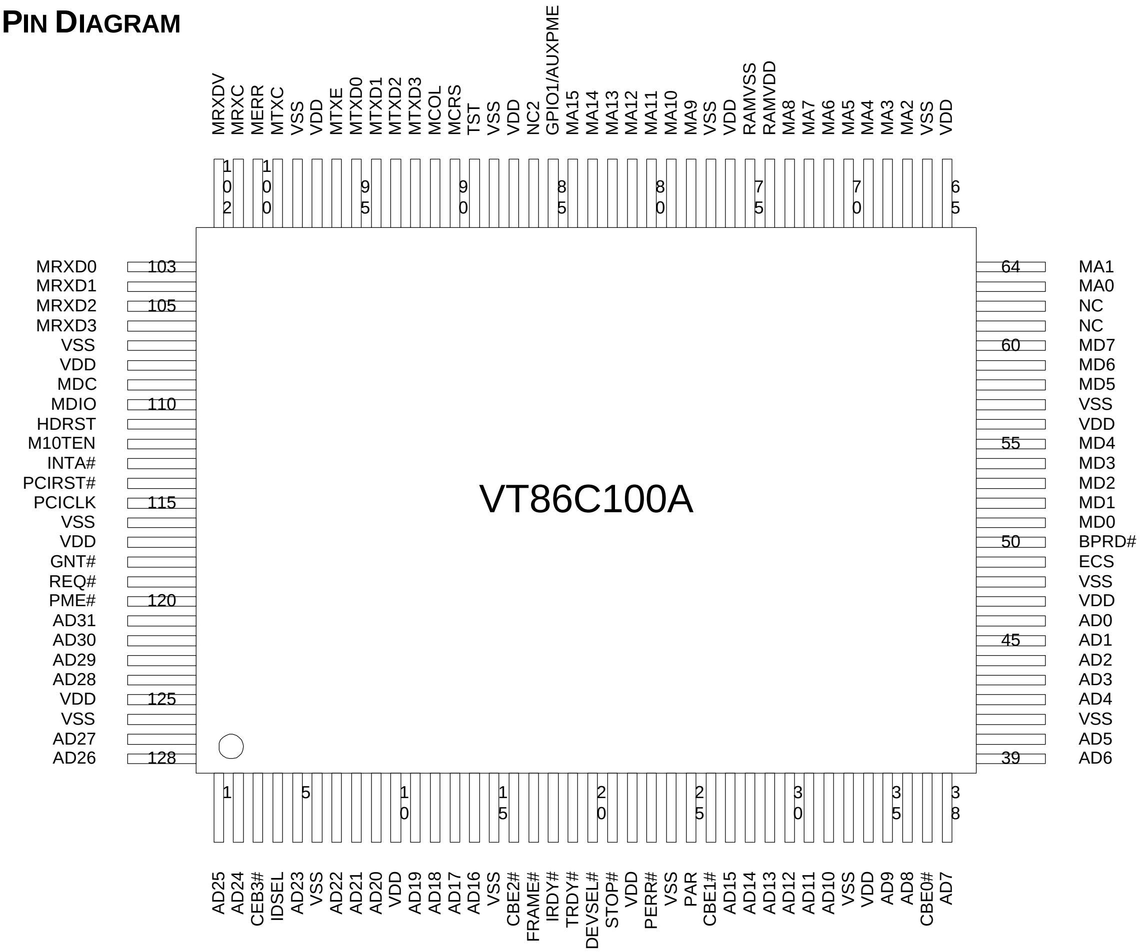


Figure 1: Application Diagram

PIN DIAGRAM


VT86C100A
MRXDV
MRXC
MERR
MTXC
VSS
VDD
MTXE
MTXD0
MTXD1
MTXD2
MTXD3
MCOL
MCRS
TST
VSS
VDD
NC2
GPIO1/AUXPME
MA15
MA14
MA13
MA12
MA11
MA10
MA9
VSS
VDD
RAMVSS
RAMVDD
MA8
MA7
MA6
MA5
MA4
MA3
MA2
VSS
VDD
MRXD0
MRXD1
MRXD2
MRXD3
VSS
VDD
MDC
MDIO
HDRST
M10TEN
INTA#
PCIRST#
PCICLK
VSS
VDD
GNT#
REQ#
PME#
AD31
AD30
AD29
AD28
VDD
VSS
AD27
AD26
MA1
MA0
NC
NC
MD7
MD6
MD5
VSS
VDD
MD4
MD3
MD2
MD1
MD0
BPRD#
ECS
VSS
VDD
AD0
AD1
AD2
AD3
AD4
VSS
AD5
AD6
AD25
AD24
CEB3#
IDSEL
AD23
VSS
AD22
AD21
AD20
VDD
AD19
AD18
AD17
AD16
VSS
CBE2#
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
VDD
PERR#
VSS
PAR
CBE1#
AD15
AD14
AD13
AD12
AD11
AD10
VSS
VDD
AD9
AD8
CBE0#
AD7
103
105
110
115
120
125
128
64
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50
45
39
1
5
10
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20
25
30
35
38
102
100
95
90
85
80
75
70
65

PIN DESCRIPTIONS

No.	Name	Type	Description
PCI Bus Interface			
121-124,127-128,1-2,5,7-9,11-14,27-32,35-36,38,39-40,42-46	AD31-0	I/O	Address/Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. The address phase is the clock cycle in which FRAME# is asserted. Write data is stable and valid when IRDYB is asserted and read data is stable and valid when TRDYB is asserted.
115	PCICLK	I	PCICLK provides timing for all transactions on PCI and is an input pin to every PCI device.
113	INTA#	OD	INTA# is an asynchronous signal which is used to request an interrupt
114	PCIRST#	I	When PCIRST# is asserted low, the VT86C100A chip performs an internal system hardware reset. PCIRST# may be asynchronous to CLK when asserted or deasserted. It is recommended that the deassertion be synchronous to guarantee clean and bounce free edge.
3,16,26,37	CBE#[3:0]	I	Bus Command/Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, CBE3-0B define the Bus Command. Burring the data phase, CBE3-0B are used as Byte Enables. The Byte Enables define which physical byte lanes carry meaningful data. CBE0B applies to byte 0 and CBE3B applies to byte 3.
4	IDSEL	I	Used as a chip select during PCI configuration cycle.
17	FRAME#	I/O	Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase.
18	IRDY#	I/O	Initiator Ready indicates the initiating agent's ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock when both IRDY# and TRDY# are asserted. During a write, IRDY# indicates that valid data is present on AD31-0. During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted simultaneously.
19	TRDY#	I/O	Target Ready indicates the target's agent's ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock when both IRDY# and TRDY# are asserted. During a read, TRDY# indicates that valid data is present on AD31-0. During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted simultaneously.
20	DEVSEL#	I/O	Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.
21	STOP#	I/O	VT86C100A drives STOP# to disconnect further traction.

25	PAR	T/S	Parity is even parity across AD31-0 and CBE3-0B. PAR is stable and valid one clock after the address phase. For data phases PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction.
118	GNT#	I	Bus grant asserts to indicate to the VT86C100A that access to the bus is granted.
119	REQ#	O	Bus request is asserted by the bus master indicate to the bus arbiter that it wants to use the bus.
23	PERR#	I/O	Parity error asserts when a data parity error is detected
120	PME#	O	Power management event interrupt
111	HDRST	O	When PCIRST# is asserted low, the VT86C100A chip performs an internal system hardware reset. Then HDRST is asserted high for external device reset signal like PHY device.
Network Interface			
91	MCOL	I	Collision detect when the external PHY device
90	MCRS	I	Carrier sense is asserted by the external PHY when the media is active
92-95	MTXD[3-0]	O	MII 4 parallel transmit data lines. This data be synchronized to assertion by the MTXC signal
96	MTXEN	O	Transmit enable signals that the transmit is active in the MII port to an external PHY device
99	MTXC	I	MII transmit clock supports the 25mhz or 2.5mhz transmit clock supplied by the external PMD device. This clock should always be active.
100	MERR	I	MII receive error asserts when a data decoding error is detected by external PHY device.
101	MRXC	I	MII receive clock supports the 25mhz or 2.5mhz clock. This clock is recovered by the PHY.
102	MRXDV	I	MII data valid
103-106	MRXD[0-3]	I	Four parallel receive data lines. This data be driven from external PHY be synchronized with MRXC signal.
109	MDC	O	MII management data clock be soured by VT86C100A MDC bit (MIIR:0) to the external PHY devices as timing reference for the MDIO signal.
110	MDIO	I/O	MII management data input/output, read from MDI bit (MIIR:1) or written from MDO bit (MIIR:2)
112	GPIO	I/O	GPIO
External Memory Support & General purpose I/O support			
49	EECS	O	EEPROM Chip Select: Chip select signal for the external EEPROM when a EEPROM is used to provide the configuration data and Ethernet Address. A 100K pull-up resistor is connected.
50	BPRD#	O	Boot PROM Read: Read the Boot ROM on the memory support data bus.
51	MD0/ EEDO	I/O	Bootrom data 0 Serial ROM Data output
52	MD1/ EEDI	O/O	Bootrom data 1 Serial ROM Data input
53	MD2/ EECLK	O/O	Bootrom data 2 Serial ROM Clock signal
54-55,58-60	MD3-7	I/O	Bootrom Data [3-7] :

63-64,67-73,78-84	MA0-MA15	O	Bootrom address line [0-15]
85	GPIO1/AUXPME	IO	General purpose input and output 1 : usually as Magic key interrupt line
112	GPIO2/LKC	IO	General purpose input and output 2, this pin usually as link change status from external PHY device.
Power Supply & Ground			
10,22,34,47,56,65,76,87,97,108,117,125	VDD, VDDA	P	Positive 5V Supply: Supply power to Internal digital logic, Digital I/O pads, and TD, TX pads. Double bonding may be required.
6,15,24,33,41,48,57,66,75,77,88,98,107,116,126	VSS, VSSA	G	Negative Supply: digital ground. Multiple bonding pads are required to separate core and I/O pads ground.

FUNCTIONAL DESCRIPTIONS

1. GENERAL DESCRIPTION

The VT86C100A Rhine ACPI **PCI bus master** 100 M FAST Ethernet controller is CMOS VLSI designed for easy implementation of CSMA/CD IEEE 802.3u 100M local area networks. Significant features include: twisted-pair interface, PCI Plug&Play compatibility, 32 bit bus mastering, powerful buffer management and Early Interrupt Receive/Transmit.

The VT86C100A integrates the entire bus interface of PCI systems. Setting hardware jumpers or software configures the VT86C100A bus interface. The VT86C100A also complies with PCI specification v2.1.. The VT86C100A supports the Media Independent Interface (MII) network interface.

1.1 FIFO AND CONTROL LOGIC

The VT86C100A incorporates two independent 2K bytes deeper FIFO for transmit or receive data from system interface or to the network interface, providing temporary storage of data, free host system from the real-time demands on network.
The VT86C100A enhanced the FIFO management logic to handle received data packets up to four packets before transfer to system data buffer. This ability reduce the packets losing due to PCI bus mastering abrition latency.

2. NETWORK INTERFACE

The VT86C100A Rhine ACPI support one MII interface

2.1 MII Interface

The MII interface is an IEEE 802.3 compliant interface that provides a simple and easy interconnection between the MAC layer and PHY device. This interface has support the following characteristics :

- Support both 10M and 100M data rate.
- Contains data and synchronous clock
- 4-bit independent receive and transmit data.
- Uses TTL signal levels and compatibles with common CMOS processes.

3. EEPROM Interface and Programming

VT86C100A uses an 93C46 to store configuration data and Ethernet address.

3.1. EEPROM Contents

	D15	D0
3FH	Reserved for 93C46	Reserved for 93C46
.	.	.
.	.	.
.	.	.
.	.	.
.	.	.
.	.	.
10H	.	.
0FH	73H	73H
0EH	CFG_D	CFG_C
0DH	CFG_B	CFG_A
0CH	BCR1	BCR0
0BH	MAX_LAT	MIN_GNT
0AH	Reserved	Reserved
09H	KEY5	KEY5
08H	KEY3	KEY2
07H	KEY1	KEY0
06H	Reserved	Reserved
05H	SUBVID1	SUBVID0
04H	SUBSID1	SUBSID0
03H	Reserved	Reserved
02H	Ethernet Address 5	Ethernet Address 4
01H	Ethernet Address 3	Ethernet Address 2
00H	Ethernet Address 1	Ethernet Address 0

Note 1. The word on location 03H is optional to user's application requirement.
Note 2. Programming 73H into the upper address is required to protect the Ethernet address from being destroyed accidentally
Note 3. The word on location 04H, 05H is sub-System ID, sub-Vendor ID in PCI specification 2.1.

3.2. DIRECT PROGRAMMING OF EEPROM

The VT86C100A features a easy way to program external EEPROM in-situ. When the RESET is active and if the upper byte of 0FH on EEPROM is not 73H, the EEPR bit will not be set to indicate that the current EEPROM has not been programmed yet. This will allow the VT86C100A to enter Direct Programming mode if EELOAD is also set. In this mode the user can directly control the EEPROM interface signals by writing to the ECSR Port and the value on the EECS, ESK and EDI bits will be driven onto the EECS, SK(MD2), and DI(MD1) outputs respectively. These outputs will be latched so the user can generate a clock on SK by repetitively writing 1 then 0 to the appropriate bit. This can be used to generate the EEPROM signals as per the 93C46 data sheet.

To read the EEPROM data, users have to generate EEPROM interface signals into EECS, DI and SK as described above and in the mean time read the data from DO(MD0) input via pin SD0. Reading Data Transfer Port during programming will not affect the latched data on EECS, SK, and DI outputs. When the

EEPROM has been programmed and verified (remember to program the upper byte of 0EH & 0FH with 73H), the user must give VT86C100A a power-on reset to return to normal operation and to read in the new data.

The Direct Programming mode is mainly used for production to program every bit of the EEPROM. Once the upper byte of 0EH has been programmed with 073H and a power-on reset has been performed, there is no way to change the contents of EEPROM except Configuration Registers A, B, and C, which will be discussed in the following paragraph. For more information, refer to EECSR.

3.3. EMBEDDED PROGRAMMING OF EEPROM

If the upper byte of 0FH of EEPROM has been programmed to 073H when VT86C100A is loading the EEPROM data during power-on reset, the EEPR bit of Signature Register will be set to prohibit the Direct Programming mode. However, the user can still program the configuration registers A, B, and C using the Embedded Programming mode by following the routine specified in the pseudo code below. This operation will work regardless of the value of EECONFIG. The setting of the EELOAD bit of Configuration Register B starts the EEPROM write process. Care should be taken not to accidentally modify the POL and GDLNK bits because these two bits return the value indifferent from the setting. This programming process is ended when the EELOAD bit goes to zero.

```
EEPROM_EMB_PROG ( )
{    // defined constant: CONFIG_B,  EELOAD
     // declared register: value, config_for_A, config_for_B, config_for_C
     // declared function: DISABLE_INTERRUPTS, ENABLE_INTERRUPTS, READ, WRITE, WAIT
     DISABLE_INTERRUPTS ( );
     value = READ (CONFIG_B);
     value = value | EELOAD;
     WRITE (CONFIG_B, value);
     READ (CONFIG_B);
     WRITE (CONFIG_B, config_for_A);
     WRITE (CONFIG_B, config_for_B);
     WRITE (CONFIG_B, config_for_C);
     while (value || EELOAD)
     {
          value = READ (CONFIG_B);
          WAIT ( );
     }
     ENABLE_INTERRUPTS ( );
}
```

4. PCI Configuration Space

<table>
<tr><td colspan="2">Device ID
(6100)</td><td colspan="2">Vendor ID
(1106)</td><td>00 h</td></tr>
<tr><td colspan="2">STATUS
(DEVS1, DEVS0) = (1 , 0)</td><td colspan="2">COMMAND
(MMSPACE, IOSPACE)</td><td>04 h</td></tr>
<tr><td colspan="3">CLASS CODE
(02_00_00)</td><td>Revision ID
(04)</td><td>08 h</td></tr>
<tr><td>BIST
(00)</td><td>Header type
(00)</td><td>Latency Timer
(R/W)</td><td>Cache Line
(R/W)</td><td>0c h</td></tr>
<tr><td colspan="4">CSR Memory Map Base Addr 000 | 0 | 0 | 0 | 1</td><td>10 h</td></tr>
<tr><td colspan="4">CSR IO MAP SPACE 000 | 0 | 0 | 0 | 0</td><td>14 h</td></tr>
<tr><td colspan="2">Sub-System ID</td><td colspan="2">Sub-Vendor ID</td><td>2c h</td></tr>
<tr><td colspan="2">EXP ROM BASE [31: 15]</td><td colspan="2">ROM14 | 0000_0000_00000 | EN</td><td>30 h</td></tr>
<tr><td colspan="2">Reserved</td><td colspan="2">Reserved</td><td></td></tr>
<tr><td>Max_LAT
(00)</td><td>Min_GNT
(00)</td><td>INT PIN
(01)</td><td>INTLINE
INTL [7:0]</td><td>3c h</td></tr>
<tr><td colspan="2">Reserved</td><td colspan="2">Reserved</td><td></td></tr>
<tr><td>MODE3</td><td>MODE2</td><td>FIFOTST</td><td>MODE0</td><td>50H</td></tr>
</table>

5. *MAGIC KEY FILTERING AND WAKE ON MAGIC KEY*

The VT86C100A provides an one level power down mode. The BIOS or Network OS device driver can configure Register A to diagnostic mode then set the Power-on bit of the diagnostic port to "on." When the VT86C100A is in Power down mode, all power to the PCI interface is cut off and the chip clock is stopped. Other registers are read only. Only the diagnostic port is read/writeable.

The VT86C100A can store one “Magic Key” (6 bytes Ethernet address) as external trigger event. When VT86C100A received one Magic Key address packet, the PME# or GPIO1 will be generated to system. These signal can be asserted to ATX power PS-ON (refere to ATX specification v2.01) or mother board wake up interrupt line like ring-in.

6. BUFFER MANAGEMENT & HOST COMMUNICATION

The VT86C100A provides an simply and effective buffer management and host communication method through the PCI Bus mastering : There are two descriptor lists, one for receive and one for transmit. The base of these two list are pointed into the CRDA (18h) and CTDA (1ch) registers.

The descriptor list reside in the host physical memory address space with **double word boundary**. And each descriptor lists just point to one single buffer, but a data buffer consists of either an entire frame or part of a frame. Data chain can be enabled or disabled by DES1 C bit. Data buffer also reside in host physical memory double word boundary space.

The device driver can make the last descriptors next link be point to first descriptor address, become a ring buffer structure.

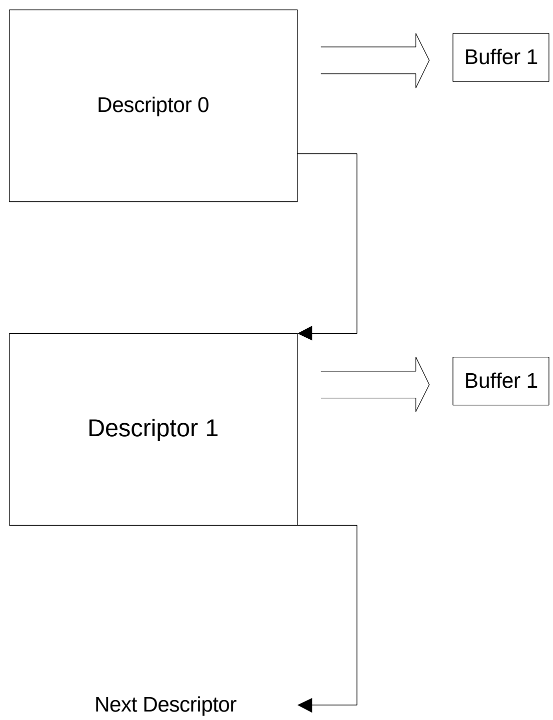

Figure 6-1 VT86C100A Buffer Management : Chain buffer Structure

6.1 DESCRIPTOR RING AND CHAIN STRUCTURE

6.1.1 RECEIVE DESCRIPTORS

Figure 6-2 shows the receive descriptor format :

Providing single buffer, one byte-count buffers, and next descriptor address. And Chain bit control span multiple data buffers data chain to be compatible various types of memory management schemes..

	31					23	15		7
RDES0	O	0	0	0	0	FLNG[10:0]	RSR1		RSR0
RDES1	Reserve					Reserve	C	0000	RLNG[10:0]
RDES2	Rx Data Buffer Start Address								
RDES3	Next Descriptor Address								

FIGURE 6-2 THE RECEIVE DESCRIPTOR FORMAT :

6.1.2. RECEIVE DESCRIPTOR 0 (RDES0)

RDES0 contain the received frame status, the frame length and the descriptor ownership information.

Bit		Sym	Description
31		OWN	**Owner** : This bit control by driver, 1 to identify this descriptor own by VT86C100A controller, 0 means this descriptor be a free descriptor; Driver must set this bit be zero when initialed.
30-27		0000	**Extend Frame Length** : Extend byte count for no-normal size Ethernet frame
26-16		FLNG	**Frame Length** : Received frame length,
15-8			
	15	RXOK	**Received OK :** The VT86C100A received a good packet from network.
	13	MAR	**Multicast Address Received :** VT86C100A MAC received multicast address packet
	12	BAR	**Boardcast Address Received :** VT86C100A MAC received boardcast address packet
	11	PHY	**Physical Address Received :** Physical address received
	10	CHN	**CHAIN :** means of chain buffer,
	9	STP	**Start of Packet :** In descriptor ring structure, STP=EDP=1 single buffer descriptor, or chained buffer structure be follows : STP EDP Description 1 1 Single buffer descriptor 1 0 First buffer descriptor, further buffer chained 0 1 Chained buffer packet end 0 0 X
	8	EDP	**End of Packet :** End of Packet buffer
7-0		RSR0	**Receive Status Register 0 :**
	7	BUFF	**Buffer Error :** Receive Buffer Error
	6	SERR	**System bus error :**
	5	RUNT	**Runt Packet Received :**
	4	LONG	**Long Packet Received :**
	3	FOV	**FIFO Overflow :**
	2	FAE	**Frame Align Error :**
	1	CRC	**CRC Error :** received frame CRC checksum error
	0	RERR	**Receive Error :** this bit be set by CRC error or frame alignmnet error or FIFO overflow or System bus error.

6.1.3. RECEIVE DESCRIPTOR 1 (RDES1)

RDES1 contain the interrupt control enable, the chained frame identical and the receive buffer fragment size information.

Bit	Sym	Description
31-24	Reserve	
23	IC	**Interrupt Control** : This bit support for interrupt PACEing , set 1 mean the VT86C100A received this descriptor will generate the interrupt.
23-16	Reserve	
15	C	**Chain** : Chain buffer , this bit be set to 1 means there are chained buffer in next descriptor
14-11	0000	**Extend Fragment of Frame Length** : must be zero now.
10-0	RLEN	**Rx buffer Size** : Receive buffer size for this descriptor, the total byte count of whole frame will be stored in last descriptors

6.2.1. TRANSMIT DESCRIPTORS

	31		23	15		7
RDES0	O	Reserve		TSR1		TSR0
RDES1	Reserve		TCR	C	0000	TLNG[10:0]
RDES2	Tx Data Buffer Start Address					
RDES3	Next Descriptor Address					

FIGURE 6-3 THE TRANSMIT DESCRIPTOR FORMAT

6.2.2. TRANSMIT DESCRIPTOR 0 (TDES0)

TDES0 contain the received frame status, the frame length and the descriptor ownership information.

Bit	Sym	Description
31	OWN	**Owner** : This bit control by driver, 1 to identify this descriptor own by VT86C100A controller, 0 means this descriptor be a descriptor waiting for transmit; Driver must set this bit be zero when initialed.
30-24	Reserve	
23-16	TCR	Transmit configure register
15-8	TSR1	**Transmit Status Register 1**
15	TXOK	**Transmit OK** : This bit be 1 for transmission error, the transmit include following - internal FIFO under-flow - excessive collision (ABT) - late collision (OWC) - carrier sense lost (CRS)
14	JAB	**Jabber :** This bit will set high if Jabber condition happens. Writing to this bit has no effect.
13	SERR	**System Error :** VT86C100A MAC experience error master abort, target abort, parity error.
12	Reserve	
11	Reserve	

10	CRS	**Carrier Sense lost** bit is set when the carrier is lost during the transmission of a packet.
9	OWC	**Late Collisions :** This bit is set when late collision occurred.
8	ABT	**Transmit Abort :** transmit module abort after excessive collision.
7-0	TSR0	**Transmit Status Register 0**
7	CDH	**CD heartbeat :** this bit only effective in 10Base-T mode. When set, this bit indicates a heartbeat collision check failure.
6-3	NCR[3:0]	**Collision retry count :** this 4-bits counter indicates the number of collisions that occurred
2	Reserve	Reserve
1	UDF	**FIFO under-flow :** this bit set indicates that the transmitter aborted by transmit FIFO encountered an empty while transmitting a frame.
0	DFR	**Deferred:** When set, indicates that the VT86C100A had to defer while ready to transmit a frame because carrier was asserted.

6.2.3. Transmit Descriptor 1 (TDES1)

TDES1 contain the transmit status, the frame length and the descriptor ownership information.

Bit	Sym	Description
31-24	Reserve	
23-16	TCR	**Transmit Configure Register**
23	IC	**Interrupt Control** : This bit support for interrupt PACEing , set 1 mean the VT86C100A received this descriptor will generate the interrupt.
22	EDP	**End of Packet :** End of Packet buffer
21	STP	**Start of Packet :** In descriptor ring structure, STP=EDP=1 single buffer descriptor, or chained buffer structure be follows : STP EDP Description 1 1 Single buffer descriptor 1 0 First buffer descriptor, further buffer chained 0 1 Chained buffer packet end 0 0 X
20-17	Reserve	Reserve
16	CRC	**CRC disable :** The VT86C100A transmitter will disable generated the CRC when this set 1.
15	C	**Chain** : Chain buffer
14-11	0000	**Extend Fragment of Frame Length** : must be zero now.
10-0	TLNG	**Transmit buffer size :** the fragment of frame buffer size

6.3 Buffer Structure and Interrupt Control

A data consists of an entire frame or part of a frame, but it cannot exceed a single Ethernet frame size. Buffers contain only data; All buffer status is maintained in the descriptor . Data chaining can be enable or disable by Chain bit in DES1[15]. The interrupt control also can be enable or disable by DES1[23]

6.3.1 Multiple Chained buffer structure

The VT86C100A can support multiple chain buffer for direct map to OS`s data buffer. The VT86C100A bus mastering module will direct move the data from network to the OS`s data buffer or direct transmit the data in OS`s buffer onto network not necessary move to a temperate data buffer. But the data buffer must be double word aligned. In this multiple chained buffer structure, the first data buffer descriptor Chain

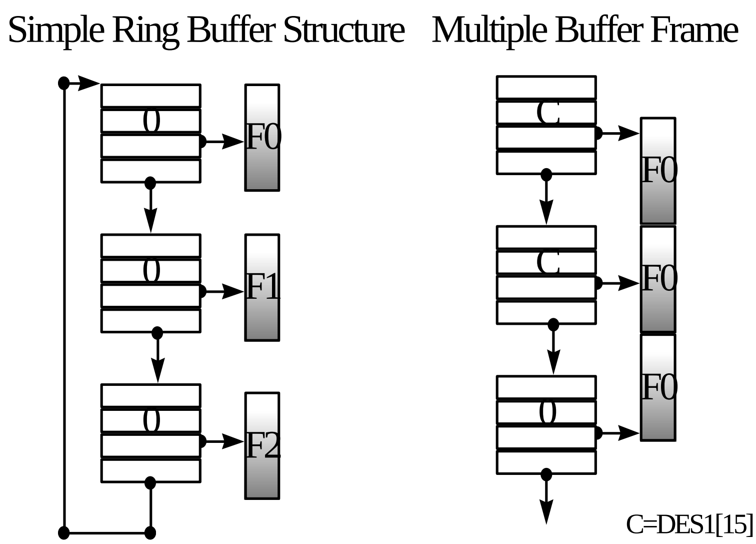

Figure 6 : Ring buffer and multiple buffer structure

6.3.2 Interrupt Control

The VT86C100A can controllable the receive descriptors and transmit descriptor for what the interrupt occurred.

The IC bit (DES1[23]) be set 1, the receive or transmit interrupt will be generate the interrupt no matter the frame been complete received or transmitted. This feature will enable the OS pre-fetch the frame header or saving the interrupt service overload.

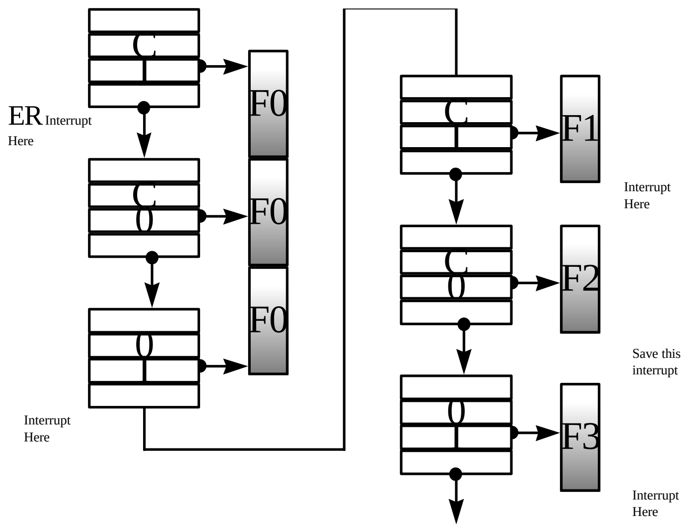

Figure 7. The Interrupt Control of VT86C100A

VT86C100A REGISTERS

Group 1 : Internal Command Status Register (CSR) Layout

NO	byte3	byte2	byte1	byte0	type
00	PAR3/KEY3	PAR2/KEY2	PAR1/KEY1	PAR0/KEY0	RW
04	TCR	RCR	PAR5/KEY5	PAR4/KEY4	RW
08			CR1	CR0	RW
0c	IMR2	IMR0	ISR1	ISR0	RW
10	MAR3	MAR2	MAR1	MAR0	RW
14	MAR7	MAR6	MAR5	MAR4	RW
18	Curr Rx Desc Addr				RW
1c	Curr Tx Desc Addr				RW
20	Current Rx Desc 0				RO
24	Current Rx Desc 1				RO
28	Current Rx Desc 2				RO
2c	Current Rx Desc 3				RO
30	Next Rx Desc 0				RO
34	Next Rx Desc 1				RO
38	Next Rx Desc 2				RO
3c	Next Rx Desc 3				RO
40	Current Tx Desc 0				RO
44	Current Tx Desc 1				RO
48	Current Tx Desc 2				RO
4c	Current Tx Desc 3				RO
50	Next Tx Desc 0				RO
54	Next Tx Desc 1				RO
58	Next Tx Desc 2				RO
5c	Next Tx Desc 3				RO
60	Current Rx DMA Pointer				RW
64	Current Tx DMA Pointer				RW
68	Tally counter test port				RW
6c	BCR1	BCR0	MIISR	PHY ADR	
70	MII DATA REG		MIIADR	MIICR	RW
74		GPIO	TEST	EECSR	RW
78	CFGD	CFGC	CFGB	CFGA	RW
7c	Tally counter_CRC		Tally counter_MPA		RW

Configuration and Diagnostic Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Read/ Write
Conf. A	EELOAD	JUMPER	MMIOEN	MIIOPT	AUTOOPT	MT10ENI	MT10ENO	MT10EOE	78H
Conf. B	QPKTDIS	TPACEN	MRDM	TXARBIT	RXARBIT	MWWAIT	MRWAIT	LATMEM	79H
Conf. C	RES	BROPT	DLYEN	DTSEL	BTSEL	BPS2	BPS1	BPS0	7AH
Conf. D	GPIOEN	DIAG	MRDLEN	MAGIC	CRADOM	CAP	MBA	BAKOPT	7BH

Note :

1. The shaded area denoted that those bits are also selective via external jumpers.
2. All reserved bit must be zero.

No.	Name	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	PAR0	R/W	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
01H	PAR1	R/W	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8
02H	PAR2	R/W	DA9	DA10	DA11	DA12	DA13	DA14	DA15	DA16
03H	PAR3	R/W	DA17	DA18	DA19	DA20	DA21	DA22	DA23	DA24
04H	PAR4	R/W	DA25	DA26	DA27	DA28	DA29	DA30	DA31	DA32
05H	PAR5	R/W	DA33	DA34	DA35	DA36	DA37	DA38	DA39	DA40
06H	RCR	R/W	RRFT2	RFT1	RFT0	PROM	AB	AM	AR	SEP
07H	TCR	R/W	RTSF	RTFT1	RTFT0		OFST	LB1	LB0	
08H	CR0	R/W		RDMD	TDMD	TXON	RXON	STOP	STRT	INIT
09H	CR1	R/W	SRST	RDMD1	TDMD1	KEYPAG	DPOLL	FDX	ETEN	EREN
0AH										
0BH										
0CH	ISR0	R/W	CNT	BE	RU	TU	TXE	RXE	PTX	PRX
0DH	ISR1	R/W	KEYI	SRCI	ABTI	NBFI	PRAI	OVFI	ETI	ERI
0EH	IMR0	R/W	CNTM	BEM	RUM	TUM	TXEM	RXEM	PTXM	PRXM
0FH	IMR1	R/W	KEYIM	SRCM	ABTM	NBFM	PRAIM	OVFM	ETM	ERM
10H	MAR0	R/W	FB7	FB6	FB5	FB4	FB3	FB2	FB1	FB0
11H	MAR1	R/W	FB15	FB14	FB13	FB12	FB11	FB10	FB9	FB8
12H	MAR2	R/W	FB23	FB22	FB21	FB20	FB19	FB18	FB17	FB16
13H	MAR3	R/W	FB31	FB30	FB29	FB28	FB27	FB26	FB25	FB24
14H	MAR4	R/W	FB39	FB38	FB37	FB36	FB35	FB34	FB33	FB32
15H	MAR5	R/W	FB47	FB46	FB45	FB44	FB43	FB42	FB41	FB40
16H	MAR6	R/W	FB55	FB54	FB53	FB52	FB51	FB50	FB49	FB48
17H	MAR7	R/W	FB63	FB62	FB61	FB60	FB59	FB58	FB57	FB56
18H	RDA0	R/W	AB7	AB6	AB5	AB4	AB3	AB2	AB1	AB0
19H	RDA1	R/W	AB15	AB14	AB13	AB12	AB11	AB10	AB9	AB8
1AH	RDA2	R/W	AB23	AB22	AB21	AB20	AB19	AB18	AB17	AB16
1BH	RDA3	R/W	AB31	AB30	AB29	AB28	AB27	AB26	AB25	AB24
1CH	TDA0	R/W	AB7	AB6	AB5	AB4	AB3	AB2	AB1	AB0
1DH	TDA1	R/W	AB15	AB14	AB13	AB12	AB11	AB10	AB9	AB8
1EH	TDA2	R/W	AB23	AB22	AB21	AB20	AB19	AB18	AB17	AB16
1FH	TDA3	R/W	AB31	AB30	AB29	AB28	AB27	AB26	AB25	AB24
6CH	MPHY	R/W	MPO1	MPO0		PHYAD4	PHYAD3	PHYAD2	PHYAD1	PHYAD0
6DH	MIISR	R/W	GPIO1POL	LEDPOL	MFDC	PHYOPT	MIIERR	MRERR	LNKFL	SPEED
6EH	BCR0	R/W		REQOPT	CRFT2	CRFT1	CRFT0	DMAL2	DMAL1	DMAL0

6FH	BCR1	R/W			CTSF	CTF1	CTF0	POT2	POT1	POT0
70H	MIICR	R/W	MAUTO	RCMD	WCMD	MDPM	MOUT	MDO	MDI	MDC
71H	MIIAD	R/W		MSRCEN	MDONE	MAD4	MAD3	MAD2	MAD1	MAD0
72H										
73H										
74H	EECSR	R/W	EEPR	EMBP	LOAD	DPM	ECS	ECK	EDI	EDO
75H	TEST	R/W	HBDIS	FCOL	BKOFF	TSTOVF	TSTUDF	TEST2	TEST1	TEST0
76H										
77H										
78H	CFGA	R/W	EELOAD	JUMPER	MMIOEN	MIIOPT	AUTOOPT	MT10ENO	MT10ENO	MT10EOE
79H	CFGB	R/W	QPKTDIS	TPACEN	MRDM	TXARBIT	RXARBIT	MWWAIT	MRWAIT	LATMEN
7AH	CFGC	R/W		BROPT	DLYEN	DTSEL	BTSEL	BPS2	BPS1	BPS0
7BH	CFGD	R/W	GPIOEN	DIAG	MRDLEN	MAGIC	CRADOM	CAP	MBA	BAKOPT
7CH	MPAC0	R/W	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
7DH	MPAC1	R/W	CD15	CD14	CD13	CD12	CD11	CD10	CD9	CD8
7EH	CRCC0	R/W	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
7FH	CRCC1	R/W	CD15	CD14	CD13	CD12	CD11	CD10	CD9	CD8

1.1 Configure Register Layout

Configuration Register A (0x78)

Bit	Symbol	Jumper	Function
0	GPIO2OE	MD3	**GPIO2OE** : Output enable of GPIO2 pin
1	GPIO2O	n/a	**GPIO2O :** Output to GPIO2 pin
2	GPIO2I	n/a	**GPIO2I :** GPIO2 input status
3	AUTOOPT	n/a	**AUTOOPT :** enable receive event auto transmit descriptor polling
4	MIIOPT	n/a	
5	MMIEN	n/a	**MMIEN :** Memory mapped IO enable, accept memory command
6	JUMPER	GPIO2	**JUMPER :** Jumper mode to select PHY and operation mode
7	EELOAD	n/a	**EELOAD :** Enable EEPROM embedded and direct programming

Configuration Register B (0x79)

Bit	Symbol	Jumper	Function
0	LATMEN	n/a	**LATMEN:** Latency timer effect enable
1	MRWAIT	n/a	**MRWAIT :** Master read insert one wait state 2-2-2-2
2	MWWAIT	n/a	**MWWAIT:** Master write insert one wait state 2-2-2-2
3	RXARBIT	n/a	**RXARBIT :** the receiving FIFO DMA will be interleave to transmitting FIFO DMA after 32 double words transaction.
4	TXARBIT	n/a	**TXARBIT** : the transmitting FIFO DMA will be interleave to receiving FIFO DMA after 32 double words transaction.
5	MRDM	n/a	**MRDM :** Memory read multiple capable
6	TPACEN	n/a	**TPACEN :** Tx descriptor pacing algorithm enable
7	QPKTDIS	n/a	**QPKTDIS :** disable transmit frame queuing.

Configuration Register C (0x7A)

Bit	**Symbol**	**Jumper**	**Function**
0-2	BPS0- BPS3	n/a	**Boot PROM Select:** Select size at which boot PROM begins and the size *Bit2 Bit1 Bit0 Size* 0 0 0 No Boot PROM 0 0 1 8K 0 1 0 16K 0 1 1 32K 1 X X 64K
3	BTSEL	n/a	**BTSEL :** Bootrom timing select
4	res	n/a	
5	DLYEN	n/a	**DLYEN** : Delay transaction while memory read Bootrom
6	BROPT	n/a	**BROPT** : set Bootrom address line above Bootrom size selected to logic 1 for small size Bootrom
7	res	n/a	

Configuration Register D (0x7B)

Bit	Symbol	Jumper	Function
0	BAKOPT	n/a	**BAKOPT :** Back-off algorithm optional

1	MBA	n/a	**MBA :** Modify back off algorithm
2	CAP	n/a	**CAP :** Capture effect back off
3	CRADOM	n/a	**CRADOM :** Random back off algorithm
4	MAGIC	n/a	**MAGIC :** Turn on Magic key
5	MRDLEN	n/a	MRDLEN : PCI memory read line capable
6	DIAG	n/a	**DIAG :**
7	GPIOEN	n/a	**GPIOEN :** Turn on GPIO2 input status change monitor

VT86C100A Command Status Registers

MAC command and status register Group

CR0: Command Register 0 (08H; Type=R/W)
This register is used to select register pages, enable or disable remote DMA operation and issue commands.

Bit	Symbol	Description
7	RES	Reserved
6	RDMD	This bit indicates that the VT86C100A receive poll demand enable
5	TDMD	This bit indicates that the VT86C100A transmit poll demand enable
4	TXON	This bit indicates that the VT86C100A start transmit state while STRT bit on
3	RXON	This bit indicates that the VT86C100A start receive state while STRT bit on
2	STOP	This bit indicates that the VT86C100A into STOP state , this bit set by SFRST bit or hardware reset
1	STRT	This bit indicates that VT86C100A enter the start command.
0	INIT	Initialize Start : When set on the VT86C100A start to set its bus master register the start

CR1: Command Register 1 (09H; Type=R/W)
This register is used to select register pages, enable or disable remote DMA operation and issue commands.

Bit	Symbol	Description
7	SRST	This bit is set when VT86C100A enters reset state and is cleared when a start command is issued to the CR1. It is also set when receive buffer overflows or system error.
6-4	RES	Reserved
3	DPOLL	Disable transmit auto polling
2	FDX	This bit set MAC to full duplex in 10BaseT or 100BaseT mode
1	ETEN	Early transmit mode enable while CFGD[1] be enable, this bit be clear while hardware reset only
0	EREN	Early receive mode enable while CFGD[0] be enable, this bit be clear while hardware reset only

RCR: Receive Configuration Register (06H; Type=R/W)
This register reflects the NIC receive configuration and reset by hardware reset and software reset

Bit	Symbol	Description
7	RRSF	Receive store and forward
6-5	RFT[1-0]	Receive FIFO Threshold. RRFT2 RRFT1 RRFT0 Threshold 0 0 0 64 bytes 0 0 1 32 0 1 0 128 0 1 1 256 1 0 0 512 1 0 1 768 1 1 0 1024 1 1 1 Receive store and forward
4	PRO	If PRO=1, all packets with physical destination address are accepted. If PRO=0, physical address must match the node address programmed in PAR0-5
3	AB	If AB=1, packets with broadcast destination address are accepted. If AM=0, packets with broadcast destination are rejected.
2	AM	If AM=1, packets with multicast destination address are accepted. If AM=0, packets with multicast destination are rejected.

1	AR	If AR=1, packets smaller than 64 bytes are accepted. If AR=0, packets smaller than 64 are rejected.
0	SEP	If SEP=1, packets with receive errors are accepted. If SEP=0, packets with receive errors are rejected.

TCR: Transmit Configuration Registers (07H, Type=R/W)

Bit	Symbol	Description
7	RTSF	Transmit and store and forward : till whole packet enter into FIFO then start transmit
6-5	RFT[1-0]	Transmit FIFO Threshold : RTSF RTF1 RTF0 Threshold 0 0 0 64 bytes 0 0 1 32 0 1 0 128 0 1 1 256 1 0 0 512 1 0 1 768 1 1 0 1024 1 1 1 Transmit store and forward
4	-	Reserve
3	OFSET	Back-off priority selection : change the back off algorithm as National specification
2-1	LB[1-0]	Loopback mode select for transmit : 0 0 Normal 0 1 Internal loopback 1 0 ENDEC loopback for 10Base-T or MII loopback 1 1 223 loopback or others
0	-	Reserved.

ISR: Interrupt Status Register (0CH; Type=R/W)
This register reflects the NIC status. The host reads it to determine the cause of the interrupt Individual bits are cleared by writing a "1" to the corresponding bit. It must be cleared after power up.

Bit	Symbol	Description
15	KEYI	Magic packet key received interrupt status
14	SRCI	Port status change interrupt status
13	ABTI	transmit abort interrupt status, this bit will be set while excessive collision
12	NORBF	No more receive buffer to use
11	PKRACE	FIFO overflow condition, next packet race into FIFO with current packet
10	OVFI	receiving FIFO overflow interrupt status
9	ETI	Transmit descriptor underflow while in early transmit mode or general I/O pin M10TENI status change interrupt while GPIOEN=1, this interrupt can be used as PHY report the link status change.
8	ERI	Indicates the received packet has filled the first data buffer.
7	CNT	CRC error or packet race tally counter overflow interrupt, software can maintain drivers CRC error counter above 32 bit
6	BE	PCI Bus error interrupt
5	RU	Receive buffer unavailable
4	TU	Transmit buffer underflow
3	TXE	Transmit error bit is set when a packet transmission is aborted due to excessive collisions.
2	RXE	This bit is set when a packet is received with one or more of the following errors: 1) CRC error, 2) Frame alignment error and 3) Missed packet.
1	PTX	This bit indicates that packet is transmitted with no errors.
0	PRX	This bit indicates that packet is received with no errors.

IMR Interrupt Mask Register (0EH; Type=R/W)
All bits correspond to the bits in the ISR register. Power up=all 0s. Setting individual bits will enable the corresponding interrupts.

EEPROM Configuration and status Register Group

EECSR EEPROM Command Status Register (74H, Type=R/W)

Bit	Symbol	Description
7	EEPR	EEPROM programming status
6	EMBP	EEPROM embedded program enable, the VT86C100A will set this bit to zero after programming complete.
5	LOAD	Dynamic reload EEPROM content, the PAR[5-0] will be update
4	DPM	Direct program EEPROM
3	ECS	EEPROM interface chip select status
2	ECK	EEPROM interface clock status
1	EDI	EEPROM interface data in status
0	EDO	EEPROM interface data out status

MII port control and status Register Group

MIICR MII interface control register (070H, Type=R/W)

Bit	Symbol	Description
7	MAUTO	MII management port auto polling enable, MIICR has no effect while this set on
6	RCMD	read enable to read PHY status, reset while complete and PHY status will be store in register MII data register 0x72
5	WCMD	write enable to program PHY, reset while PHY programmed completely
4	MDPM	direct program mode enable, while MDPM be set , the WCMD and RCMD have no effect
3	MOUT	MDIO output enable indicator while direct program mode
2	MDO	MII interface management port data output status
1	MDI	MII interface management port data input status
0	MDC	MII interface management port clock status

MIIAD MII CSR offset address register (071H, Type=R/W)

Bit	Symbol	Description
7	–	
6	MSRCEN	
5	MDONE	
4	MAD4	MII management port address bit 4
3	MAD3	MII management port address bit 3
2	MAD2	MII management port address bit 2
1	MAD1	MII management port address bit 1
0	MAD0	MII management port address bit 0

The MII management port address default value be (00001)b,

MIISR MII status register (06dH, Type=R/W)

Bit	Symbol	Description
7	GPIO1POL	**GPIO1POL** : General purpose I/O 1 pin output polarity, when this bit set as '1', the GPIO1 pin output active high; set as '0', the GPIO1 pin output active low.
6	res	Reserve
5	MFDC	**MFDC :** Accelerate the MDC speed when VT86C100A enter MII auto polling; MFDC set as '0', MDC be normal speed; or MFDC set as '1' , MDC be 4 times speed.
4	PHYOPT	**PHYOPT :** set 1 use default external PHY device address as 0001
3	MIIERR	**MIIERR :** PHY device coding error by insert RX_ERR, write to clear it.
2	MRERR	**MRERR :** MII Management read error, write to clear **it**
1	LNKFL	**LNKFL :** Link fail in 10 or 100MHz
0	SPEED	**SPEED :** Network speed, 0 as 100MHZ, 1 as 10MHz

PHYADR

MII configuration register (06cH, Type=R/W)

Bit	Symbol	Description

7-6	MPO[1-0]	MII management port polling timer interval, timer unit be MDC clock cycle MPO1 MPO0 clock 0 0 1024 0 1 512 1 0 128 1 1 64
5	res	
4-0	PHYAD[4-0]	**PHY[4-0] :** external PHY device address , these register bytes stored from EEPROM loading when power up or EEPROM auto-reloading or can be programmed by software, default as (00001)b

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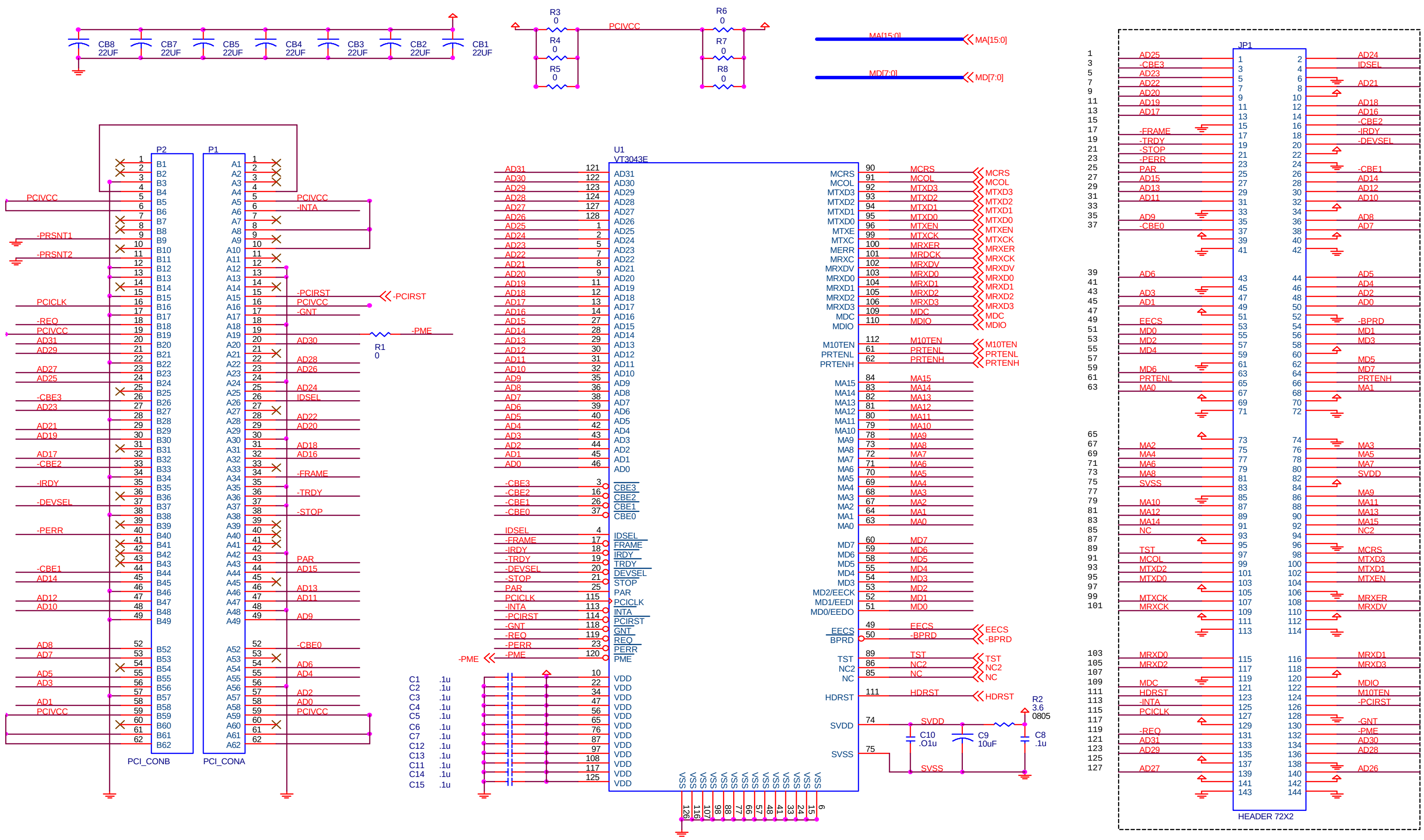

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Size C	Document Number VT5134A	Rev A
Date: Thursday, September 04, 1997	Sheet 1 of 3	

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|2.SCH
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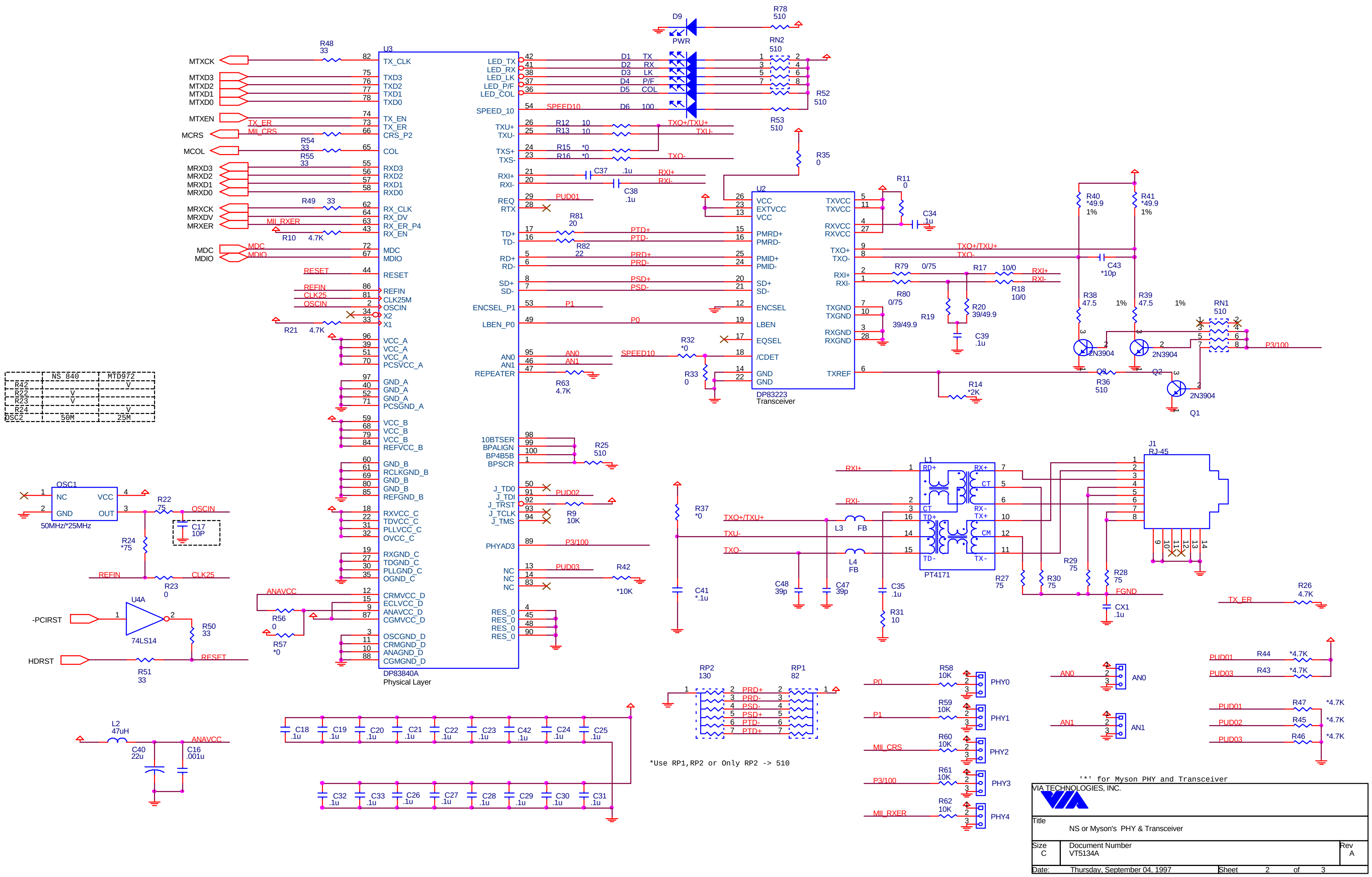

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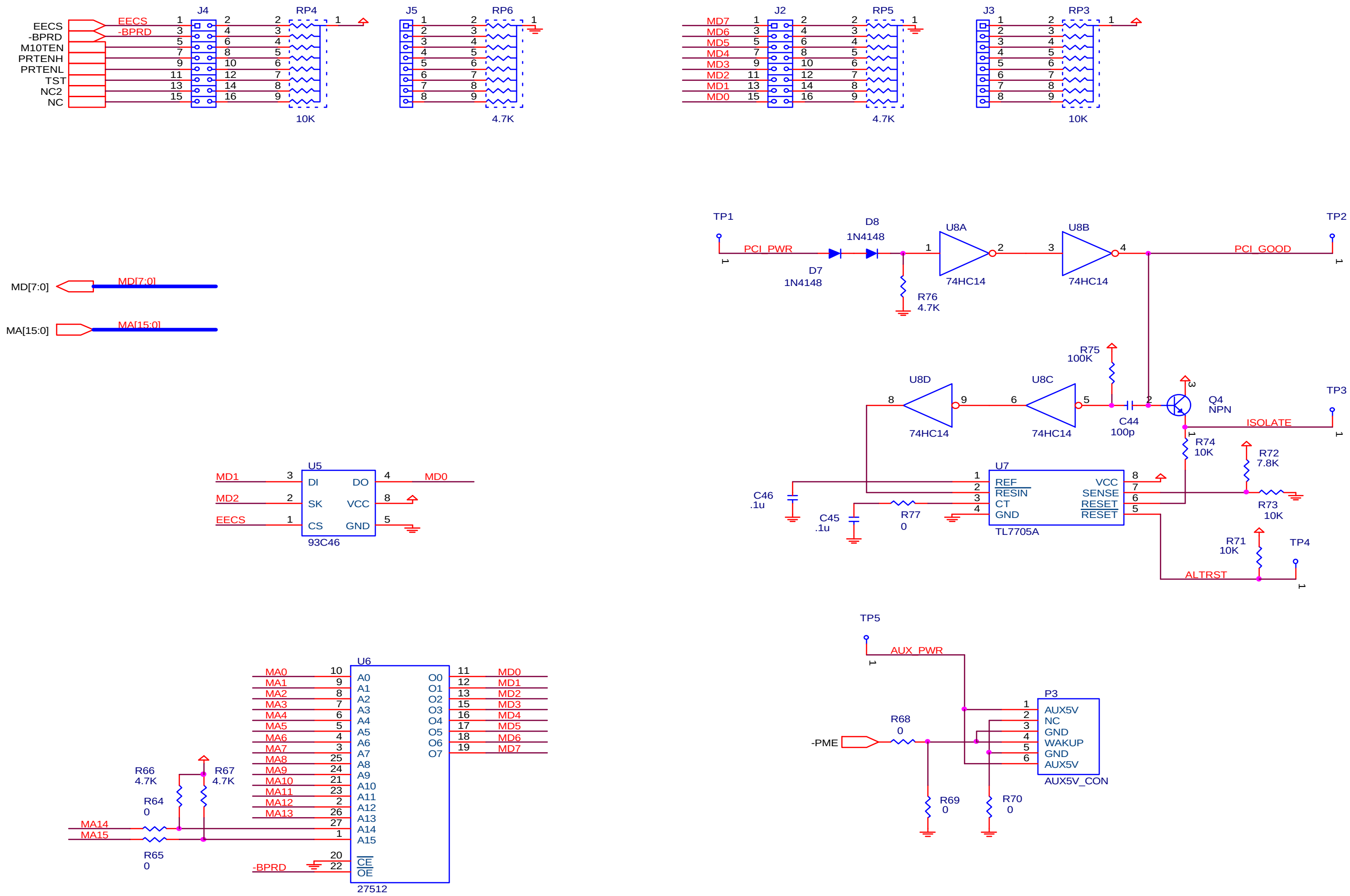
R22	V	
R23	V	
R24		V
OSC2	50M	25M



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