Advance Product Information

VSC7962

3.125Gb/s PECL Limiting Amplifier with LOS Detect and Laser Driver with Automatic Power Control

Features

- 3.3V Power Supply
- Laser Driver AC-Coupled to Laser Diode
- Programmable Laser Driver Modulation Current from 5mA to 60mA
- Programmable Laser Driver Bias Current from 1mA to 100mA
- Laser Driver Enable Control
- Automatic Optical Average Power Control
- Supply Current of 80mA
- PECL Limiting Amplifier Outputs
- 48-Pin TQFP Package

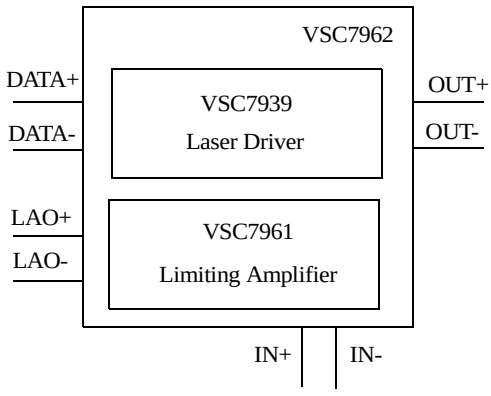
Applications

- SONET/SDH at 622Mb/s, 1.244Gb/s, 2.488Gb/s and 3.125Gb/s
- Full-Speed Fibre Channel (1.062Gb/s)

General Description

The VSC7962 is a single 3.3V supply combination limiting amplifier and laser diode driver for SONET/SDH applications up to 3.125Gb/s. The limiting amplifier features Loss of Signal (LOS) detect, output offset correction, and optional output squelch. Laser driver data inputs accept differential PECL signals and the output modulation and bias currents are easily controlled via external components. The laser diode driver Automatic Power Control (APC) loop maintains a constant average optical power over temperature and lifetime. The dominant pole of the APC loop can be controlled with an external capacitor. Other features include enable control, short-circuit protection for the modulation and bias inputs, short rise and fall times, and failure-monitor output to indicate when the APC loop is unable to maintain the average optical power. The VSC7962 is available in die form or in a 48-pin TQFP package. The VSC7960 provides similar features to the VSC7962 but the limiting amplifier has CML outputs.

Block Diagram



Electrical Characteristics

Table 1: Limiting Amplifier DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{CC}	Power Supply Range	3.135		5.5	V	
I_{CC}	Power Supply Current(1)		31		mA	V_{CC} = 3.3V
I_{EE}	Power Supply Current(1)		38		mA	V_{CC} = 3.3V
I_{CCSQ}	Power Supply Current when Squelched(1)		21		mA	V_{CC} = 3.3V
I_{EESQ}	Power Supply Current when Squelched(1)		24		mA	V_{CC} = 3.3V
I_{SQ}	Squelch Input Current	0		400	µA	
PSSR	Power Supply Rejection Ratio	20	30		dB	f < 2MHz

NOTE: (1) See Figure5 for supply current measurement setup.

Table 2: Laser Driver DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{CC}	Power Supply Voltage Range	3.125		3.465	V	
I_{CC}	Supply Current		TBD	45	mA	R_{MODSET}=7.3kΩ, $R_{BIASMAX}$=4.8kΩ I_{BIAS} and I_{MOD} excluded V_{CC}=5V
I_{BIAS}	Bias Current Range	1		100	mA	Voltage at BIAS pin=(V_{CC}-1.6)
$I_{BIAS-OFF}$	Bias Off Current			100	µA	ENABLE=low or DISABLE=high(1)
S_{BIAS}	Bias Current Stability		230		ppm/°C	APC open loop. I_{BIAS}=100mA
			900			APC open loop. I_{BIAS}=1mA
	Bias Current Absolute Accuracy		±15		%	Refers to part-to-part variation.
VR_{MD}	Monitor Diode Reverse Bias Voltage	1.5			V	
I_{MD}	Monitor Diode Reverse Current Range	18		1000	µA	
	Monitor Diode Bias Setpoint Stability	-480	50	480	ppm/°C	I_{MD}=1mA(1)
			90			I_{MD}=18µA(1)
	Monitor Diode Bias Absolute Accuracy	-15		15	%	Refers to part-to-part variation.
I_{MOD}	Modulation Current Range	5		60	mA	
$I_{MOD-OFF}$	Modulation Off Current			200	µA	ENABLE=low or DISABLE=high(2)
	Modulation Current Absolute Accuracy		±15		%	See Note 2
	Modulation Current Stability	-480	-50	480	ppm/°C	I_{MOD}=60mA
			250			I_{MOD}=5mA

NOTES: (1) Both I_{BIAS} and I_{MOD} will turn off if any of the current set pins are grounded. (2) Assumes laser diode to monitor diode transfer function does not change with temperature.

Table 3: Limiting Amplifier AC Specifications

Symbol	*Parameter*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
	Data Rate	3.125			Gb/s	
V_{IN}	Input Voltage Range	10		1200	mV	peak-to-peak
J_D	Deterministic Jitter			25	ps	See Note 1
J_R	Random Jitter			8	ps	rms, see Note 2
$t_{R,}$ t_F	Rise/Fall Times		55	100	ps	20%-80%
v_N	Input Referred Noise			230	µV	rms, IN+ to IN-
R_{DIFF}	Differential Input Resistance		100		W	IN+ to IN-
f_L	Low Frequency Cut-off		2		MHz	C_Z open
			2		kHz	C_Z=0.1µF
V_{SQ}	Output Signal when Squelched			20	mV	Outputs AC-coupled
V_{OH}	PECL Output High Voltage	-1025		-850	mV	
				-850	mV	Squelched
V_{OL}	PECL Output Low Voltage	-1810		-1620	mV	
				-1620	mV	Squelched
Z_O	Output Resistance		100		Ω	Single-ended

NOTES: (1) Deterministic Jitter measured peak-to-peak with K28.5 pattern. (2) Random Jitter measured with minimum input.

Table 4: Laser Driver AC Specifications

Symbol	*Parameter*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
t_{SU}	Input Latch Setup Time	100			ps	LATCH=high
t_H	Input Latch Hold Time	100			ps	LATCH=high
	Enable/Start-up Delay		250		ns	
t_R	Output Rise Time		60	80	ps	20% to 80%
t_F	Output Fall Time		60	80	ps	20% to 80%
PWD	Pulse Width Distortion		10	50	ps	See Notes 1, 2
CID_{MAX}	Maximum Consecutive Identical Digits	80			bits	
t_J	Jitter Generation		7	20	ps_{p-p}	Jitter BW=12kHz to 20MHz, 0-1 pattern.

NOTES: (1) Measured with 622Mb/s 0-1 pattern, LATCH=high. (2) PWD = (wider pulse - narrower pulse) / 2)

Table 5: PECL and TTL/CMOS Inputs and Outputs Specifications

Symbol	*Parameter*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{ID}	Differential Input Voltage	100		1600	mV_{p-p}	(DATA+) - (DATA-)
V_{ICM}	Common-Mode Input Voltage	V_{CC} - 1.49	V_{CC} - 1.32	V_{CC} - V_{ID}/4	V	PECL compatible
I_{IN}	Clock and Data Input Current	-1		10	µA	
V_{IH}	TTL Input High Voltage (ENABLE, LATCH, DISABLE)	2.0			V	
V_{IL}	TTL Input Low Voltage (ENABLE, LATCH, DISABLE)			0.8	V	
V_{OH}	TTL Output High Voltage ($\overline{FAIL}$)	2.4	V_{CC} - 0.3	V_{CC}	V	Sourcing 50µA
V_{OL}	TTL Output Low Voltage ($\overline{FAIL}$)	0.1		0.44	V	Sinking 100µA

Table 6: Limiting Amplifier Loss of Signal Specifications

Symbol	*Parameter*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
H_{LOS}	LOS Hysteresis	3.1	3.3	5.5	dB	H_{LOS}= 20 log (V_{THD} / V_{THA})
t_{LOS}	LOS Assert / Deassert Time	0.22	0.25	0.28	µs	
V_{THA}	LOS Assert Threshold		8.2		mV	R_{TH}=2.5kΩ
		12.8	19.8	21.8		R_{TH}=7kΩ
			57.2			R_{TH}=20kΩ
V_{THD}	LOS Deassert Threshold		11.4		mV	R_{TH}=2.5kΩ
		26.2	29	31.6		R_{TH}=7kΩ
			75.2			R_{TH}=20kΩ
V_{LOSH}	LOS Output High Voltage	3.3			V	I_{LOS}=-30µA
V_{LOSL}	LOS Output Low Voltage		0.168		V	I_{LOS}=+1.2µA

Table 7: Limiting Amplifier Loss of Signal Truth Table

SQUELCH	*LOS*	*Output*
High	High	Off
Low	High	On
High	Low	On
Low	Low	On

© ***VITESSE*** *SEMICONDUCTOR CORPORATION* • 741 Calle Plano • Camarillo, CA 93012
Tel: (800) VITESSE • FAX: (805) 987-5896 • Email: prodinfo@vitesse.com
Internet: www.vitesse.com

Absolute Maximum Ratings(1)

Power Supply Voltage (V_{CC}) ..... -0.5V to 6V
Current into BIAS ..... -20mA to +150mA
Current into OUT+, OUT- ..... TBD
Current into MD ..... -5mA to +5mA
Current into $\overline{FAIL}$ ..... -10mA to 30mA
Voltage at DATA+, DATA-, ENABLE, LATCH, $\overline{FAIL}$ ..... -0.5V to (V_{CC} + 0.5V)
Voltage at MODSET, BIASMAX, APCSET_MD ..... -0.5V to +3.0V
Voltage at BIAS ..... -0.5V to (V_{CC} + 0.5V)
Voltage at OUT+, OUT- ..... -0.5V to (V_{CC} + 1.5V)
Continouous Power Dissipation (T_A = +85°C, TQFP derate 20.8mW/°C above +85°C) 1350mW
Operating Junction Temperature Range ..... -55°C to +150°C
Storage Temperature Range ..... -55°C to +165°C

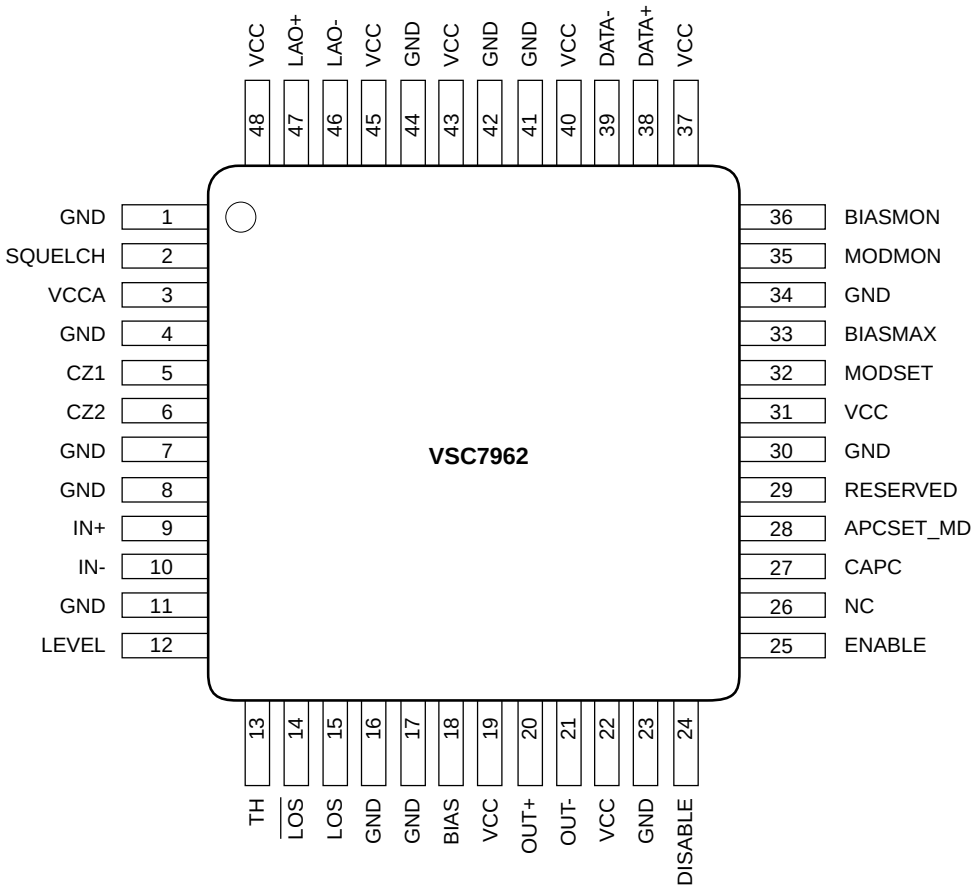
NOTE: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Positive Voltage Rail (V_{CC}) ..... +3.3V
Junction Temperature Range (T_J) ..... -40°C to +100°C
Ambient Temperature Range (T_A) ..... -40°C to +85°C

Package Pin Descriptions

Figure 1: Pin Diagram



© ***VITESSE*** *SEMICONDUCTOR CORPORATION* • 741 Calle Plano • Camarillo, CA 93012
Tel: (800) VITESSE • FAX: (805) 987-5896 • Email: prodinfo@vitesse.com
Internet: www.vitesse.com

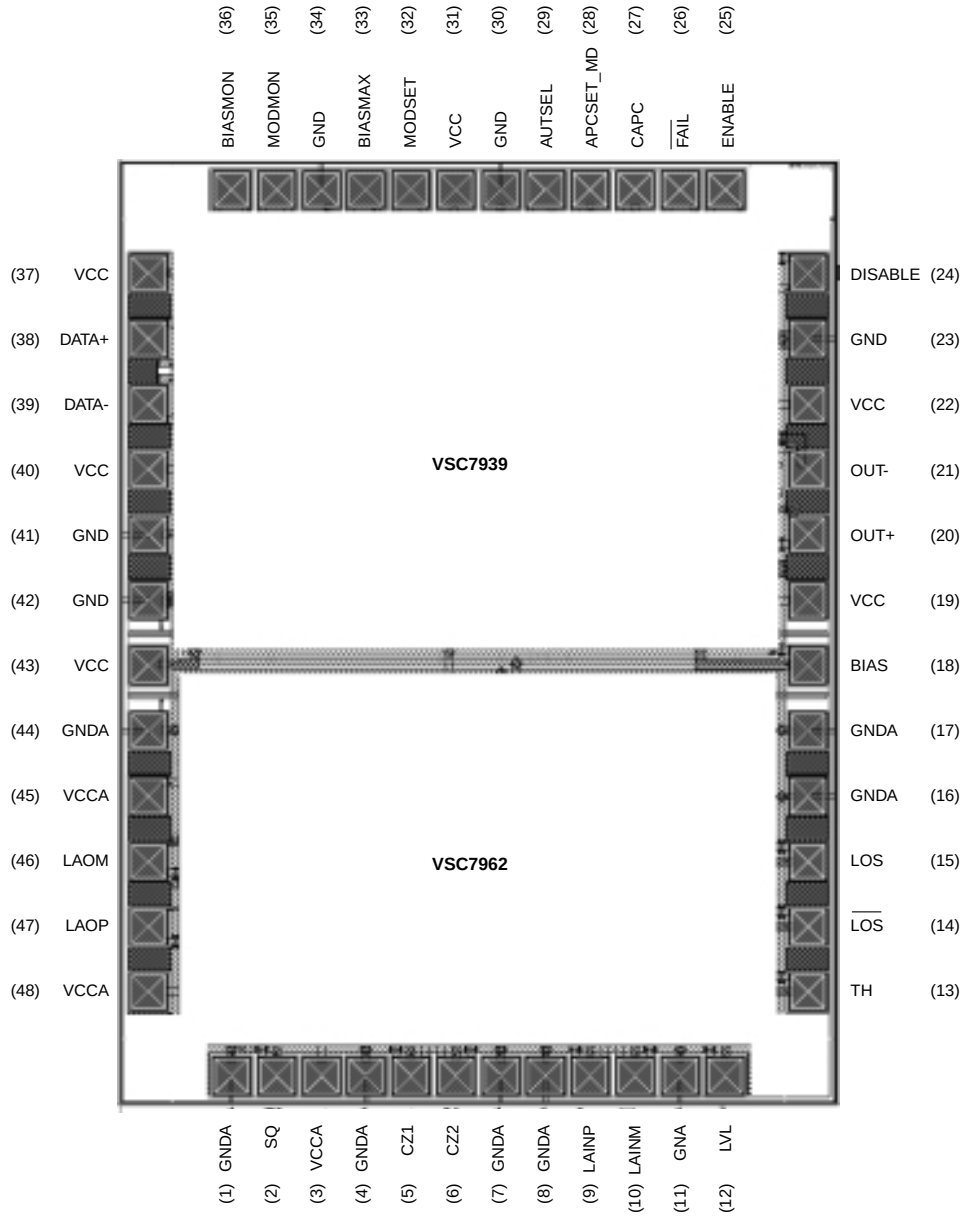
Table 8: Pin Description

Pin Name	*Pad Name*	*Pin/Pad Number*	*Section*	*Description*
GND	GNDA or GND	1, 4, 7, 8, 11, 16, 17, 23, 30, 34, 41, 42, 44	Both	Ground
VCC	VCC or VCCA	3, 19, 22, 31, 37, 40, 43, 45, 48	Both	3.3V Supply
SQUELCH	SQ	2	Limiting Amplifier	Squelch Input. Squelch is disabled if this pin in unconnected or set low. When SQUELCH is high, OUT+ and OUT- are forced to static levels. See *Detailed Description* section.
CZ1	CZ1	5	Limiting Amplifier	Offset Correction Loop Capacitor. Place capacitor between this pin and CZ2 to alter time constant of offset correction loop. See *Detailed Description* section.
CZ2	CZ2	6	Limiting Amplifier	Offset Correction Loop Capacitor. Place capacitor between this pin and CZ1 to alter time constant of offset correction loop. See *Detailed Description* section.
IN+	LAINP	9	Limiting Amplifier	Noninverted Limiting Amplifier Input Signal
IN-	LAINM	10	Limiting Amplifier	Inverted Limiting Amplifier Input Signal
LEVEL	LVL	12	Limiting Amplifier	Output Current Level. This pin may be either connected to GND or left unconnected. Connecting to GND causes output current to be 20mA. The output is 16mA when unconnected. See *Detailed Description* section.
TH	TH	13	Limiting Amplifier	Loss of Signal (LOS) Threshold. Connect a resistor from this pin to GND to set the input signal level at which LOS outputs will be asserted. See *Applications Information* section.
$\overline{\text{LOS}}$	$\overline{\text{LOS}}$	14	Limiting Amplifier	Inverted Loss of Signal Output. $\overline{\text{LOS}}$ is high for input signals above the threshold programmed by TH. See *Detailed Description* section.
LOS	LOS	15	Limiting Amplifier	Noninverted Loss-of-Signal Output. LOS is low for input signals above the threshold programmed by TH. See *Detailed Description* section.
BIAS	BIAS	18	Laser Driver	Laser Bias current output
OUT+	OUT+	20	Laser Driver	Noninverted Laser Modulation Current Output. I_{MOD} flows when input data is high.
OUT-	OUT-	21	Laser Driver	Inverted Laser Modulation Current Output. I_{MOD} flows when input data is low.

Pin Name	*Pad Name*	*Pin/Pad Number*	*Section*	*Description*
DISABLE	DISABLE	24	Laser Driver	Disable Input (TTL/CMOS). If used, leave ENABLE pin floating. Connect to GND for normal operation and V_{CC} to disable laser bias and modulation currents.
ENABLE	ENABLE	25	Laser Driver	Enable Input (TTL/CMOS). If used, connect DISABLE to GND. Connect to V_{CC} for normal operation and GND to disable laser bias and modulation currents.
$\overline{\text{FAIL}}$	$\overline{\text{FAIL}}$	26	Laser Driver	Output (TTL/CMOS). When low, indicates APC failure.
CAPC	CAPC	27	Laser Driver	Capacitor to GND sets dominant pole of the APC feedback loop.
APCSET_MD	APCSET_MD	28	Laser Driver	APCSET and Monitor Diode Input. Resistor to GND sets desired average laser optical power. If APC is not used connect 100kΩ resistor to GND. Connect to monitor photodiode anode. Connect capacitor to ground to filter high-speed AC monitor photocurrent.
RESERVED	AUTSEL	29	Laser Driver	Do not connect.
MODSET	MODSET	32	Laser Driver	Connect resistor to GND to set desired laser modulation current.
BIASMAX	BIASMAX	33	Laser Driver	Connect resistor to GND to set maximum laser bias current. The APC function can subtract from this value, but it cannot add to it.
MODMON	MODMON	35	Laser Driver	Modulation current monitor. Sink current source that is proportional to the laser modulation current.
BIASMON	BIASMON	36	Laser Driver	Bias current monitor. Sink current source that is proportional to the laser bias current.
DATA+	DATA+	38	Laser Driver	Laser Driver Noninverted Data Input (PECL)
DATA-	DATA-	39	Laser Driver	Laser Driver Inverted Data Input (PECL)
LAO-	LAOM	46	Limiting Amplifier	Inverted Limiting Amplifier Data Output (PECL)
LAO+	LAOP	47	Limiting Amplifier	Noninverted Limiting Amplifier Data Output (PECL)

© VITESSE SEMICONDUCTOR CORPORATION • 741 Calle Plano • Camarillo, CA 93012
Tel: (800) VITESSE • FAX: (805) 987-5896 • Email: prodinfo@vitesse.com
Internet: www.vitesse.com

Bare Die Pad Information



Die Size Not Including Scribe: 2076µm x 2740µm (0.08174” x 0.10788”)
Scribe Size: 157µm (0.00618”)
Pad Passivation Opening: 95µm x 95µm (0.00374” x 0.00374”)
Pad Pitch: 130µm
Die Thickness: 625µm (0.02461”)
The back side of the die may be either left floating or connected to ground.

Table 9: Pad Coordinates

Pad Name	*Pin Name*	*Pad/Pin Number*	*Section*	*X-Coordinate (µm)*	*Y-Coordinate (µm)*
GNDA	GND	1	Limiting Amplifier	322.500	80.950
SQ	SQUELCH	2	Limiting Amplifier	452.500	80.950
VCCA	VCC	3	Limiting Amplifier	582.500	80.950
GNDA	GND	4	Limiting Amplifier	712.500	80.950
CZ1	CZ1	5	Limiting Amplifier	842.500	80.950
CZ2	CZ2	6	Limiting Amplifier	972.500	80.950
GNDA	GND	7	Limiting Amplifier	1102.500	80.950
GNDA	GND	8	Limiting Amplifier	1232.500	80.950
LAINP	IN+	9	Limiting Amplifier	1362.500	80.950
LAINM	IN-	10	Limiting Amplifier	1492.500	80.950
GNDA	GND	11	Limiting Amplifier	1622.500	80.950
LVL	LEVEL	12	Limiting Amplifier	1752.500	80.950
TH	TH	13	Limiting Amplifier	1995.050	324.475
$\overline{\text{LOS}}$	$\overline{\text{LOS}}$	14	Limiting Amplifier	1995.050	514.475
LOS	LOS	15	Limiting Amplifier	1995.050	704.475
GNDA	GND	16	Laser Driver	1995.050	894.475
GNDA	GND	17	Laser Driver	1995.050	1084.475
BIAS	BIAS	18	Laser Driver	1995.050	1274.475
VCC	VCC	19	Laser Driver	1995.050	1464.475
OUT+	OUT+	20	Laser Driver	1995.050	1654.475
OUT-	OUT-	21	Laser Driver	1995.050	1844.475
VCC	VCC	22	Laser Driver	1995.050	2034.475
GND	GND	23	Laser Driver	1995.050	2224.475
DISABLE	DISABLE	24	Laser Driver	1995.050	2414.475
ENABLE	ENABLE	25	Laser Driver	1752.500	2659.050
$\overline{\text{FAIL}}$	$\overline{\text{FAIL}}$	26	Laser Driver	1622.500	2659.050
CAPC	CAPC	27	Laser Driver	1492.500	2659.050
APCSET_MD	APCSET_MD	28	Laser Driver	1362.500	2659.050
AUTSEL	RESERVED	29	Laser Driver	1232.500	2659.050
GND	GND	30	Laser Driver	1102.500	2659.050
VCC	VCC	31	Laser Driver	972.500	2659.050
MODSET	MODSET	32	Laser Driver	842.500	2659.050
BIASMAX	BIASMAX	33	Laser Driver	712.500	2659.050
GND	GND	34	Laser Driver	582.500	2659.050
MODMON	MODMON	35	Laser Driver	452.500	2659.050
BIASMON	BIASMON	36	Laser Driver	322.500	2659.050

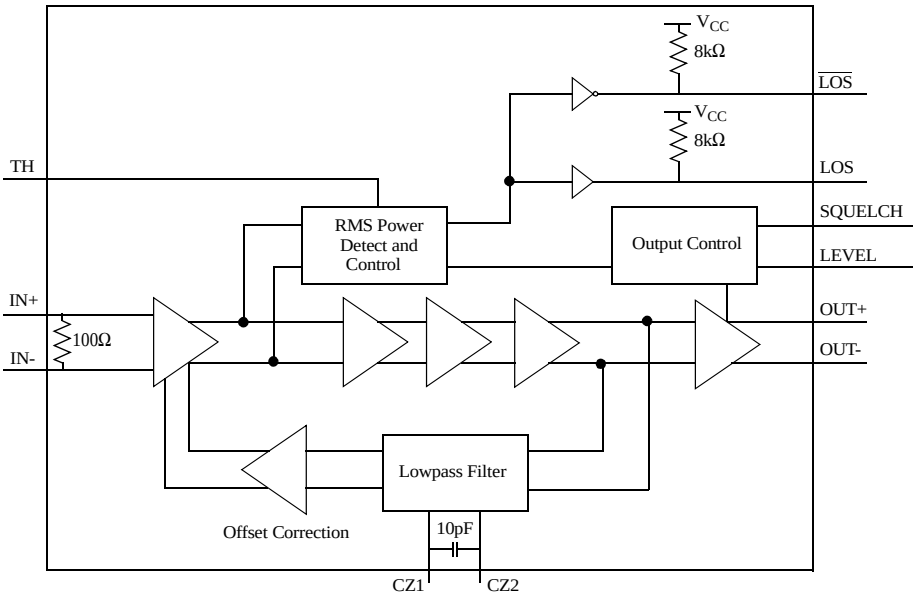
© ***VITESSE*** *SEMICONDUCTOR CORPORATION* • 741 Calle Plano • Camarillo, CA 93012
Tel: (800) VITESSE • FAX: (805) 987-5896 • Email: prodinfo@vitesse.com
Internet: www.vitesse.com

Pad Name	*Pin Name*	*Pad/Pin Number*	*Section*	*X-Coordinate (µm)*	*Y-Coordinate (µm)*
VCC	VCC	37	Laser Driver	80.975	2414.475
DATA+	DATA+	38	Laser Driver	80.975	2224.475
DATA-	DATA-	39	Laser Driver	80.975	2034.475
VCC	VCC	40	Laser Driver	80.975	1844.475
GND	GND	41	Laser Driver	80.975	1654.475
GND	GND	42	Laser Driver	80.975	1464.475
VCC	VCC	43	Laser Driver	80.975	1274.475
GNDA	GND	44	Limiting Amplifier	80.975	1084.475
VCCA	VCC	45	Limiting Amplifier	80.975	894.475
LAOM	LAO-	46	Limiting Amplifier	80.975	704.475
LAOP	LAO+	47	Limiting Amplifier	80.975	514.475
VCC	VCC	48	Limiting Amplifier	80.975	324.475

Detailed Description

The VSC7962 is a combination limiting amplifier and high-speed laser driver with Automatic Power Control (APC). The device is designed to operate up to 3.125Gb/s with a 3.3V supply. The limiting amplifier provides Loss of Signal (LOS) detect, output offset correction, and output squelch. The limiting amplifier of the VSC7962 has PECL outputs. The VSC7962 is identical to the VSC7960 except with CML limiting amplifier outputs. The laser driver data and clock inputs support PECL inputs as well as other inputs that meet the common mode voltage and differential voltage swing specifications. The differential pair output laser driver stage is capable of driving up to 60mA into the laser with typical rise and fall times of 60ps. To allow for larger output swings, the VSC7962 was designed to be AC-coupled to the laser cathode with a pull-up inductor for DC-biasing. This configuration will isolate laser forward voltage from the output circuitry and will allow the output at OUT+ to swing above and below the supply voltage V_{CC}. The laser driver output bias and modulation currents may be easily controlled via external circuitry. The key features of the VSC7962 are Automatic Power Control, Loss of Signal detect, low power supply current, and fast rise and fall times.

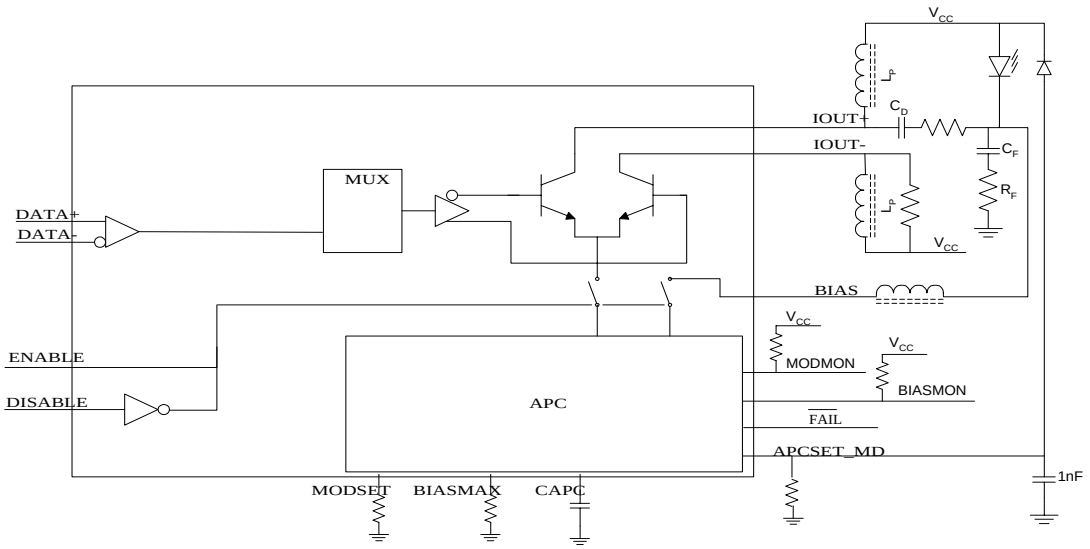
Figure 2: Limiting Amplifier Block Diagram



© ***VITESSE*** *SEMICONDUCTOR CORPORATION* • 741 Calle Plano • Camarillo, CA 93012
Tel: (800) VITESSE • FAX: (805) 987-5896 • Email: prodinfo@vitesse.com
Internet: www.vitesse.com

G52361-0, Rev 2.1
05/01/01

Figure 3: Laser Driver Block Diagram



Limiting Amplifier Squelch

Squelch is disabled when SQUELCH is not connected or is set to TTL low level. When SQUELCH is set to TTL high level and LOS is asserted, the data outputs, OUT+ and OUT- are forced to static levels. If LOS is not asserted, the outputs will not be squelched.

Limiting Amplifier Loss of Signal (LOS) Detect

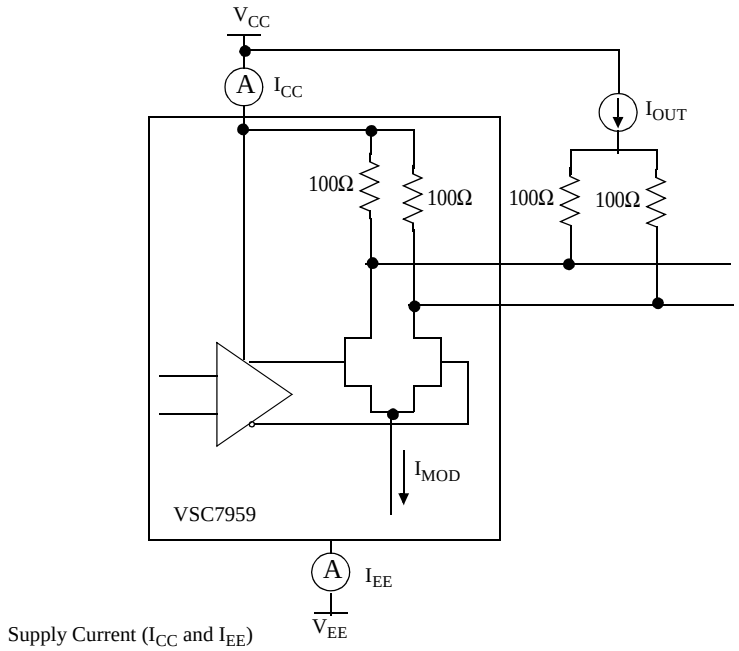
This features utilizes an RMS power detector with programmable LOS indicator to provide two outputs, LOS and $\overline{\text{LOS}}$. The input TH is used to set the threshold at which the loss of signal detector outputs, LOS and $\overline{\text{LOS}}$, change state. See Loss-of-Signal Specifications table (Table 6) for setting the resistor value between TH and ground. The Loss of Signal Truth Table (Table 7) clarifies how LOS and SQUELCH interact.

Limiting Amplifier Offset Correction

This feature is provided to ensure that the offsets in the limiting amplifier coupled with its gain do not cause the output buffer to give a false output. Because of the high gain of the amplifier, offset correction using a low-frequency feedback loop reduces input offset. If no component is placed between pins CZ1 and CZ2, the low frequency cut-off is 2MHz. If a 0.1µF capacitor is placed between CZ1 and CZ2, the low frequency cut-off is lowered to approximately 2kHz. For Fibre Channel and Gigabit Ethernet applications, leave pins CZ1 and CZ2 open. For ATM/SONET and other scrambled non-return-to-zero (NRZ) applications, place a 0.1µF capacitor between CZ1 and CZ2. This maintains a one-decade separation between the lowest input frequency and the low frequency cut-off. The low frequency cut-off of the offset correction loop is given by the following equation:

$$f_{OC} = 43 / [2\pi * 35k\ (C_Z + 100pF)]$$
$$= 196 * 10^{-6} / (C_Z + 100pF)$$
$$= 196 * 10^{-6} / (0.1\mu F + 100pF)$$
$$= 1.96kHz$$

Figure 4: Supply Current Measurement



Supply Current (I_{CC} and I_{EE})

Laser Driver Automatic Power Control

To ensure constant average optical power, the device utilizes an Automatic Power Control loop (APC). A photodiode mounted in the laser package provides optical feedback to compensate for changes in average laser output power due to changes that affect laser performance such as temperature and laser lifetime. The laser bias current is adjusted by the APC loop according to the reference current set at APCSET_MD by an external resistor. An external capacitor at CAPC controls the time constant for the APC feedback loop. The recommended value for CAPC is 0.1µF. This value reduces pattern-dependent jitter associated with the APC feedback loop and guarantees stability. If the APC loop cannot adjust the bias current to track the desired monitor current, $\overline{\text{FAIL}}$ is set low.

The device may be operated with or without APC. To utilize APC, a capacitor must be connected at CAPC (0.1µF) and a resistor must be connected at APCSET_MD to set the average optical power. For open-loop operation (no APC), a 100kΩ resistor should be connected between APCSET_MD and GND. CAPC has no effect on open-loop operation. In both modes of operation, resistors to ground should be placed at BIASMAX and MODSET to set the bias and modulation currents.

The device may be operated with or without APC. To utilize APC, a capacitor must be connected at CAPC (0.1µF) and a resistor must be connected at APCSET_MD to set the average optical power. For open-loop operation (no APC), a 100kΩ resistor should be connected between APCSET_MD and GND. CAPC has no effect on open-loop operation. In both modes of operation, resistors to ground should be placed at BIASMAX and MODSET to set the bias and modulation currents.

© VITESSE SEMICONDUCTOR CORPORATION • 741 Calle Plano • Camarillo, CA 93012
Tel: (800) VITESSE • FAX: (805) 987-5896 • Email: prodinfo@vitesse.com
Internet: www.vitesse.com

G52361-0, Rev 2.1
05/01/01

Laser Driver Short-Circuit Protection

If BIASMAX or MODSET are shorted to ground, the output modulation and bias currents will be turned off.

Laser Driver Enable/Disable

Two pins are provided to allow either ENABLE or DISABLE control. If ENABLE is used, connect disable to ground. If DISABLE is used, leave ENABLE floating. Both modulation and bias currents are turned off when ENABLE is low or DISABLE is high. Typically, ENABLE or DISABLE responds within approximately 250ns.

Controlling the Laser Driver Modulation Current

The output modulation current may be determined from the following equation where P_{p-p} is peak-to-peak optical power, P_{AVE} is average power, r_e is extinction ratio, and η is laser slope efficiency:

$$I_{MOD} = P_{p-p} / \eta = 2 * P_{AVE} * (r_e-1) / (r_e+1) / \eta$$

A resistor at MODSET controls the output bias current. Graphs of I_{MODSET} vs. R_{MODSET} in *Typical Operating Characteristics* describe the relationship between the resistor at MODSET and the output modulation current at 25°C. After determining the desired output modulation current, use the graph to determine the appropriate resistor value at MODSET.

Controlling the Laser Driver Bias Current

A resistor at BIASMAX should be used to control the output bias current. Graphs of $I_{BIASMAX}$ Vs. $R_{BIASMAX}$ in *Typical Operating Characteristics* describe the relationship between the resistor at BIASMAX and the output bias current at 25°C. If the APC is not used, the appropriate resistor value at BIASMAX is determined by first selecting the desired output bias current, and then using the graph to determine the appropriate resistor value at BIASMAX. When using APC, BIASMAX sets the maximum allowed bias current. After determining the maximum end-of-life bias current at 85°C for the laser, refer to the graph of $I_{BIASMAX}$ Vs. $R_{BIASMAX}$ in *Typical Operating Characteristics* to select the appropriate resistor value.

Controlling the Laser Driver APC Loop

To select the resistor at APCSET_MD, use the graph of I_{MD} vs. R_{APCSET} in *Typical Operating Characteristics.* The graph relates the desired monitor current to the appropriate resistance value at APCSET_MD. I_{MD} may be calculate from the desired optical average power, $P_{AVE,}$, and the laser-to-monitor transfer, ρ_{MON}, for a specific laser using the following equation:

$$I_{MD} = P_{AVE} * \rho_{MON}$$

Laser Diode Interface

An RC shunt network should be placed at the laser output interface. The sum of the resistor placed at the output and the laser diode resistance should be 25Ω. For example, if the laser diode has a resistance of 5Ω, a

20Ω resistor should be placed in series with the laser. For optimal performance, a bypass capacitor should be placed close to the laser anode.

A "snubber network" consisting of a capacitor C_F and resistor R_F should be placed at the laser output to minimize reflections from the laser (see Block Diagram, page 1). Suggested values for these components are 80Ω and 2pF, respectively. However, these values should be adjusted until a suitable optical output waveform is obtained.

Reducing Pattern-Dependent Jitter

Three design values significantly affect pattern-dependent jitter: the capacitor at CAPC, the pull-up inductor at the output (L_P), and the AC-coupling capacitor at the output (C_D). As previously stated, the recommended value for the capacitor at CAPC is 0.1µF. This results in a 10kHz loop bandwidth which makes the pattern-dependent jitter from the APC loop negligible.

For 2.5Gb/s data rates, the recommended value for C_D is 0.056µF. The time constant at the output is dominated by L_P. The variation in the peak voltage should be less that 12% of the average voltage over the maximum consecutive identical digit (CID) period. The following equation approximates this time constant for a CID period, t, of 100UI = 40ns:

$$\tau_{LP} = -t / \ln(1\text{-}12\%) = 7.8t = L_P / 25\Omega$$

Therefore, the inductor L_P should be a 7.8µH SMD ferrite bead inductor for this case.

Input/Output Considerations

Although the VSC7962 laser driver is PECL-compatible, this is not required to drive the device. The inputs must only meet the common-mode voltage and differential voltage swing specifications.

Laser Driver Power Consumption

The following equation provides the device supply current (I_S) in terms of quiescent current (I_Q), modulation current (I_{MOD}), and bias current (I_{BIAS}):

$$I_S = I_Q + 0.47 * I_{MOD} + 0.15 * I_{BIAS}$$

For 3.3V operation, I_Q is 15mA.

This equation may be used to determine the estimated power dissipation:

$$P_{DIS} = V_{CC} * I_S$$

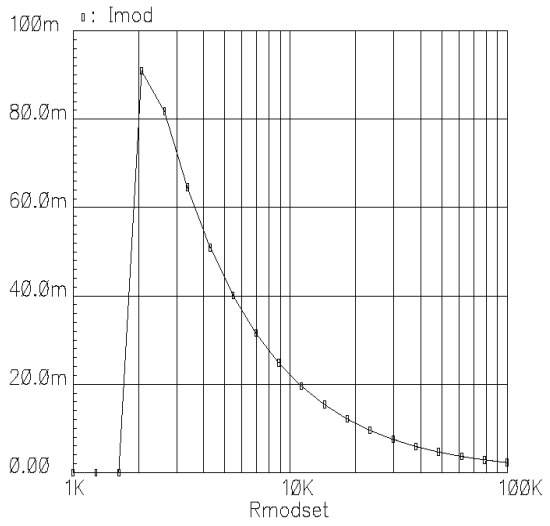
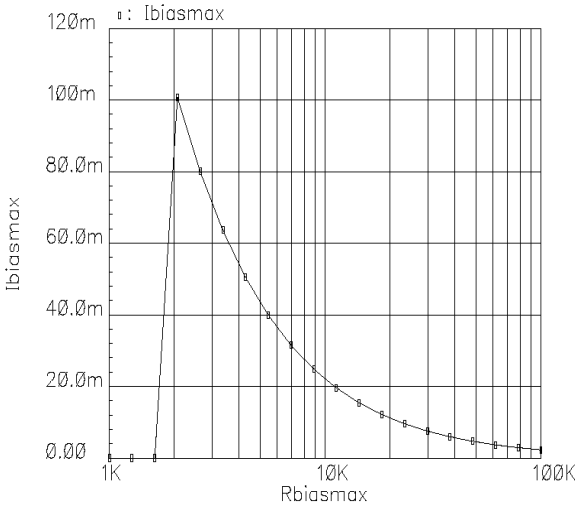
For example, the device operated at 3.3V with a 30mA modulation current and a 10mA bias current would have a supply current of:

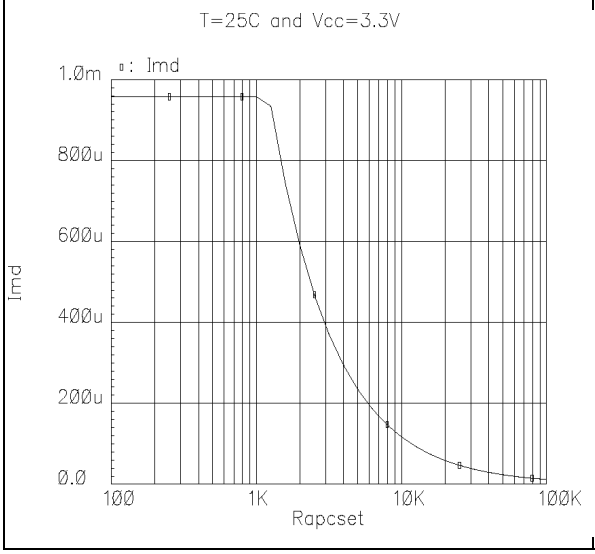
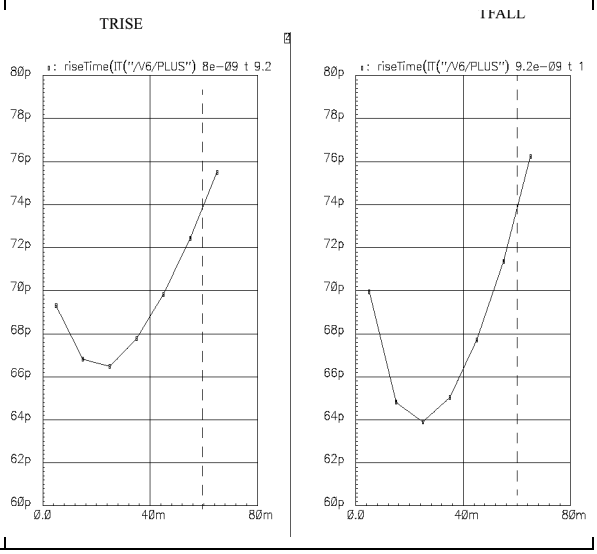
$$I_S = 15mA + 0.47 * 30mA + 0.15 * 10mA = 31mA$$

This corresponds to a power dissipation of 3.3V * 31mA = 102mW.

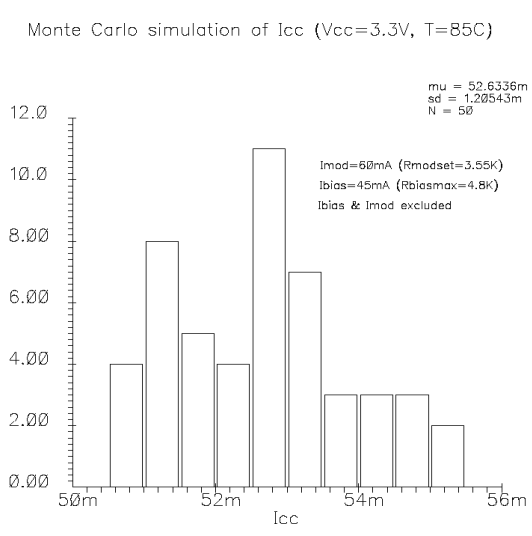
© VITESSE SEMICONDUCTOR CORPORATION • 741 Calle Plano • Camarillo, CA 93012
Tel: (800) VITESSE • FAX: (805) 987-5896 • Email: prodinfo@vitesse.com
Internet: www.vitesse.com
G52361-0, Rev 2.1
05/01/01

Typical Operating Characteristics

I_{MODSET} vs. R_{MODSET} T=25°C, V_{CC} = 3.3V	$I_{BIASMAX}$ vs. $R_{BIASMAX}$ T=25°C, V_{CC} = 3.3V
	

I_{MD} vs. R_{APCSET} T=25°C, V_{CC} = 3.3V	Rise and Fall Times T=85°C, V_{CC} = 3.3V
	

Monte Carlo Simulation of I_{CC}



Applications Information

The following is a typical design example for the laser driver of the VSC7962 assuming 3.3V operation with APC.

Select a Laser

The following table provides specifications for a typical communication-grade laser capable of operating at 2.5 Gb/s.

Table 10: Typical Laser Characteristics

Symbol	*Parameter*	*Value*	*Units*
λ	Wavelength	1310	nm
P_{AVE}	Average Optical Output Power	6	mW
I_{th}	Threshold Current	6	mA
ρ_{MON}	Laser to Monitor Transfer	0.04	mA/mW
η	Laser Slope Efficiency	0.4	mW/mA
T_C	Operating Temperature Range	-40 to +85	°C

Select Resistor for APCSET_MD

The monitor diode current is estimated by $I_{MD} = P_{AVE} * \rho_{MON} = 6mW * 0.04mA/mW = 0.24mA$. The I_{MD} vs. R_{APCSET} in *Typical Operating Characteristics* shows the resistor at APCSET_MD should be 5kΩ.

© ***VITESSE*** *SEMICONDUCTOR CORPORATION* • 741 Calle Plano • Camarillo, CA 93012
Tel: (800) VITESSE • FAX: (805) 987-5896 • Email: prodinfo@vitesse.com
Internet: www.vitesse.com

G52361-0, Rev 2.1
05/01/01

Select Resistor for MODSET

To ensure some minimum extinction ratio over temperature and lifetime, assume an optimal extinction ratio of 20 (13dB) at 25°C. The modulation current may be calculated from the following equation:

$$I_{MOD} = P_{p-p} / \eta = 2 * P_{AVE} * (r_e-1) / (r_e+1) / \eta = 2 * 6mA * (20-1) / (20 + 1) / 0.4 = 27.1mA$$

The graph of I_{MODSET} vs. R_{MODSET} in *Typical Operating Characteristics* shows the resistor for MODSET should be 8.5kΩ.

Select Resistor for BIASMAX

The maximum threshold current at +85°C and end-of-life must be determined. A graph of a typical laser's I_{th} versus T_C reveals a maximum threshold current of 30mA at 85°C. Therefore, the maximum bias can be approximated by:

$$I_{BIASMAX} = I_{TH-MAX} + I_{MOD} / 2 = 30mA + 27.1mA / 2 = 43.6mA$$

The graph of $I_{BIASMAX}$ vs. $R_{BIASMAX}$ in *Typical Operating Characteristics* shows the resistor for BIASMAX should be 5kΩ.

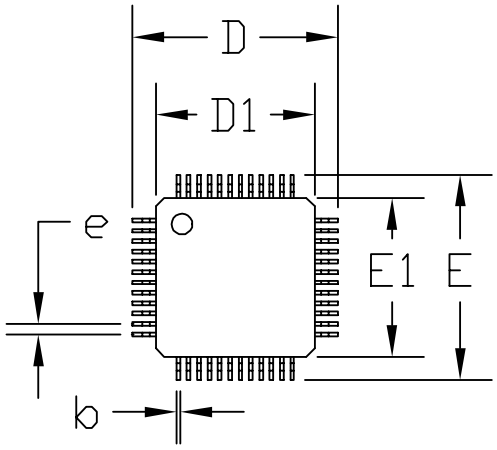
Wire Bonding

For best performance gold ball-bonding techniques are recommended. Wedge bonding is not recommended. For best performance and to minimize inductance keep wire bond lengths short.

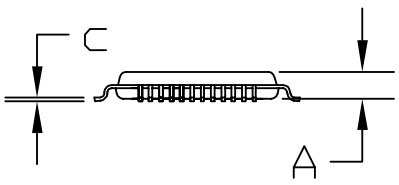
PCB Layout Guidelines

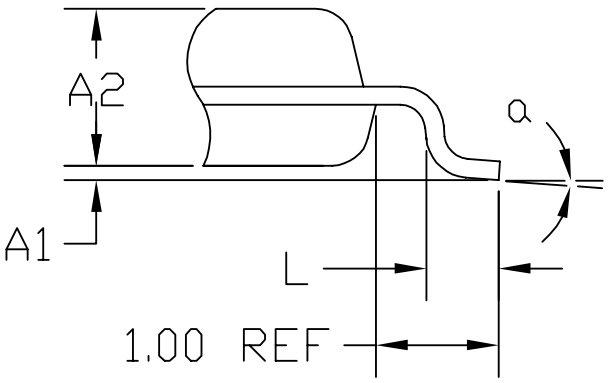
Use high frequency PCB layout techniques with solid ground planes to minimize crosstalk and EMI. Keep high speed traces as short as possible for signal integrity. The output traces to the laser diode must be short to minimize inductance. Short output traces will provide best performance.

Package Information - 48-pin TQFP



SYMBOL	JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
	TQPF		
	MIN.	NOM.	MAX.
A			1.60
A_1	0.05		0.15
A_2	1.35	1.40	1.45
D		9.00 BSC.	
D_1		7.00 BSC.	
E		9.00 BSC.	
E_1		7.00 BSC.	
L	0.45	0.60	0.75
N		48	
e		0.5 BSC.	
b	0.17	0.22	0.27
c	0.09		0.20
α	0		7





1. All dimensioning and tolerancing conform to ANSI Y14.5-1982.
2. Controlling dimension: millimeter.
3. This outline conforms to JEDEC Publication 95 Registration MS-026.

© ***VITESSE*** *SEMICONDUCTOR CORPORATION* • 741 Calle Plano • Camarillo, CA 93012
Tel: (800) VITESSE • FAX: (805) 987-5896 • Email: prodinfo@vitesse.com
Internet: www.vitesse.com

Ordering Information

The order number for this product is formed by a combination of the device type and package type.

VSC7962 XX

Device Type
3.125Gb/s PECL Limiting Amplifier with LOS Detect and Laser Driver with Automatic Power Control

Package Style:
W : Bare Die in Waffle Pack
RO : 48-pin TQFP

© ***VITESSE*** *SEMICONDUCTOR CORPORATION* • 741 Calle Plano • Camarillo, CA 93012
Tel: (800) VITESSE • FAX: (805) 987-5896 • Email: prodinfo@vitesse.com
Internet: www.vitesse.com