Preliminary Data Sheet

VSC7185

Quad Transceiver for Gigabit Ethernet and Fibre Channel

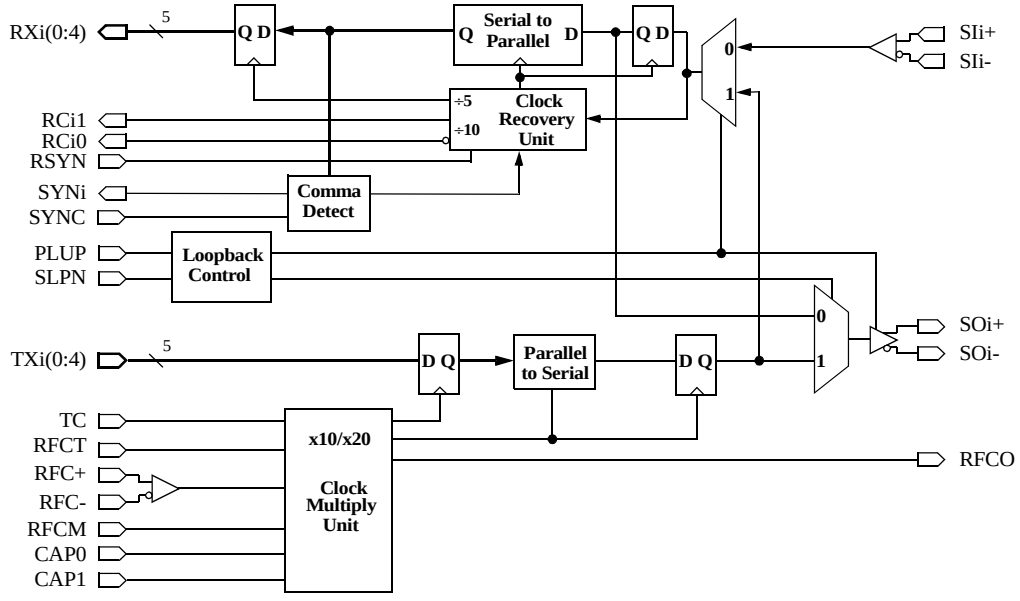
Features

- Four Complete Transceiver Functions in a Single Integrated Circuit
- SSTL-2 Compatible Parallel Data and Clocks
- 1.05Gb/s to 1.36Gb/s Operation per Channel
- Common Transmit Byte Clock
- TTL or PECL Reference Clock Input
- Per-Channel 1/10th Baud Rate Recovered Clocks and Comma Detect Outputs
- Common Comma Detect Enable Input
- Common Serial / Parallel Loopback Controls
- Cable Equalization in Receivers
- JTAG Access Port
- 3.3V Power Supply, 2.5W Dissipation, Typical
- 208 pin, 23mm BGA Package

General Description

The VSC7185 is a full-speed quad Gigabit Ethernet and Fibre Channel Transceiver IC. 8B/10B encoded (or equivalent scheme) transmit characters are serialized onto high-speed differential outputs (SOi+/-) at speeds up to 1.36Gb/s. Each of the four transmitters has a 5-bit wide parallel input bus. Parallel data is latched in by an internal clock running at up to 272MHz (2x the rate of the external common Transmit Byte Clock). Transmit data must be presented synchronously with the common transmit byte clock. Each receiver samples the serial receive data (SIi+/-), recovers the clock and data, deserializes it into 5-bit receive half-characters, outputs a recovered 2x or 1x clock and detects “Comma” characters. The VSC7185 contains on-chip PLL circuitry for synthesis of the baud-rate transmit clock and extraction of the clocks from the received serial streams.

VSC7185 Block Diagram (1 of 4 Channels)



Functional Description

Notation

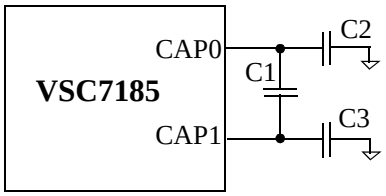
In this document, each of the four channels are identified as Channel 0, 1, 2 or 3. When discussing a signal on any specific channel, the signal will have the channel number embedded in the name, for example, "TX**3**(0:4)." When referring to the common behavior of a signal which is used on each of the four channels, the notation "i" is used. Differential signals, i.e. SOi+ and SOi-, may be referred to as a single signal, i.e. SOi, by dropping reference to the "+" and "-". RFC refers to the active reference clock input(s), RFCT or RFC+/RFC-.

Clock Synthesizer

To achieve a baud rate clock between 1.05GHz and 1.36GHz, the VSC7185 Clock Multiplier Unit (CMU) multiplies the reference frequency provided on the RFC input by 10 when RFCM=1, or by 20 when RFCM=0. The RFCT input is TTL, and the REF+/- inputs are PECL. The on-chip PLL uses a single external 0.1µF capacitor, connected between CAP0 and CAP1, to control the Loop Filter. This capacitor should be a multilayer ceramic dielectric, or better, with at least a 5V working voltage rating and a good temperature coefficient. NPO is preferred but X7R may be acceptable. These capacitors are used to minimize the impact of common-mode noise on the Clock Multiplier Unit, especially power supply noise. Higher value capacitors provide better robustness in systems. NPO is preferred because if an X7R capacitor is used, the power supply noise sensitivity will vary with temperature.

For best noise immunity, the designer may use a three capacitor circuit with one differential capacitor between CAP0 and CAP1, C1, a capacitor from CAP0 to ground, C2, and a capacitor from CAP1 to ground, C3 (see Figure 1). Larger values are better but 0.1µF is adequate. However, if the designer cannot use a three capacitor circuit, a single differential capacitor, C1, is adequate. These components should be isolated from noisy traces.

Figure 1: Loop Filter Capacitors (Best Circuit)



C1=C2=C3= >0.1uF
MultiLayer Ceramic
Surface Mount
NPO (Preferred) or X7R
5V Working Voltage Rating

Serializer

The VSC7185 accepts 5-bit parallel SSTL-2 input data on the four TXi(0:4) buses along with an SSTL-2 byte clock (TC) and serializes them into four high-speed serial streams. At the source, TXi(0:4) and TC switch synchronously with respect to an internal 5 bit-time clock. TC and RFC must be derived from the same frequency source so that TC and RFC have a fixed but arbitrary phase relationship when system clocks are stable. The 5-bit parallel transmission half-characters will be serialized and transmitted on the SOi+/- PECL differential outputs at the baud rate, with bit TXi0 (10B bit "a" or "i") transmitted first. User data should be encoded using 8B/10B or an equivalent code.

Clock Recovery

The VSC7185 accepts differential high-speed serial input from the selected source (either the PECL SIi+/ SIi- pins or the internal SOi+/- data), extracts the clock and retimes the data. Equalizers are included in the receiver to open the data eye and compensate for InterSymbol Interference (ISI) which may be present in the incoming data. The serial bit stream should be encoded so as to provide DC balance and limited run length by an 8B/10B encoding scheme. For proper operation, the baud rate of the data stream to be recovered should be within ±200 ppm of ten (or twenty) times the RFC frequency. For example, Gigabit Ethernet systems would use 125MHz oscillators with a ±100ppm accuracy resulting in ±200 ppm between VSC7185 pairs.

Deserializer

The recovered serial bit stream is converted into a 5-bit parallel output character. The VSC7185 provides complementary SSTL-2 recovered clocks, RCi0 and RCi1, which are at 1/10th of the serial baud rate. The clocks are generated by dividing down the high-speed recovered clock which is phase-locked to the serial data. The serial data is retimed, deserialized and output on RXi(0:4).

If serial input data is not present, or does not meet the required baud rate, the VSC7185 will continue to produce a recovered clock so that downstream logic may continue to function. The RCi0/RCi1 output frequency under these circumstances will differ from its expected frequency by no more than ±1%.

The receiver drives four sets of 5-pin RX data stable around the edges of RCi1 or RCi0. This is the case when RSYN=0 (see Figure 2). When RSYN=1, the receive side timing and the transmit side timing are symmetrical in that the ASIC section receiving data from the RXi(0:4) buses may alternatively receive data from the ASIC section driving the TXi(0:4) buses. In this mode, RXi(0:4) transition with the rising and falling edges of RCi0 and RCi1.

Word Alignment

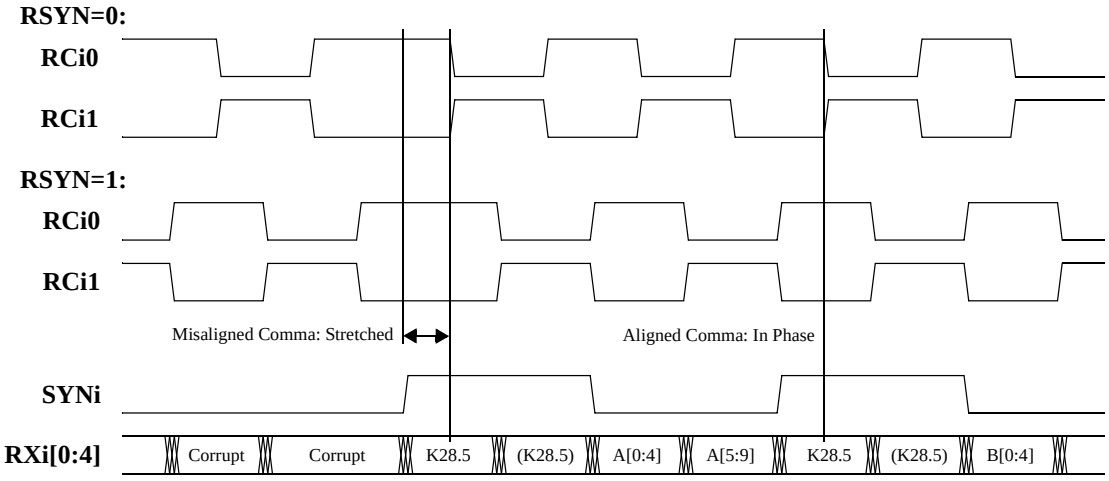
The VSC7185 provides 7-bit comma character recognition and data word alignment. Word synchronization is enabled on all channels when SYNC=1. The serial data is converted back into the original 10-bit wide data and recognizes the presence of the “Comma” pattern. This pattern is “0011111XXX”, where the leading zero corresponds to the first bit received. The comma sequence is not contained in any normal 8B/10B coded data character or pair of adjacent characters. It occurs only within special characters, known as K28.1, K28.5 and K28.7, which are defined for synchronization purposes. When SYNC=1 and an improperly aligned comma is encountered, the recovered clock is stretched, never slivered, so that the comma character and recovered clocks are aligned properly to RXi(0:4). This results in proper character and word alignment.

When the parallel data alignment changes in response to a improperly aligned comma pattern, data which would have been presented on the parallel output port prior to the comma character may be lost. The comma character itself and data subsequent to the comma character will always be output correctly and properly aligned. When SYNC=0, the current alignment of the serial data is maintained indefinitely, regardless of data pattern.

On encountering a comma character, SYNi is driven HIGH. The SYNi pulse is asserted during both 5-bit halves of the comma character. The SYNi signal is timed identically to data so that it can be captured by the adjoining protocol logic along with RXi(0:4). Functional waveforms for synchronization are shown in Figure 2. The first K28.5 shows the case where the comma is detected, but it is misaligned so a change in the output data alignment is required. Note that one or two half-characters prior to the comma character may be corrupted by the realignment process, but the comma character is always received and output correctly. The second K28.5 shows the case when a comma is detected and no phase adjustment is necessary. It illustrates the position of the SYNi pulse in relation to the comma character on RXi(0:4).

When RSYN=0, there will always be a rising edge on RCi1 when the first five bits of the K28.5 character are output. When RSYN=1, there will always be a rising edge on RCi1 between the first and second five bits of the K28.5 character, and there may or may not be a falling edge on RCi1 coincident with the assertion of SYNi (the first five bits of the K28.5 character). The behavior depends on the alignment of the new comma relative to the current RCi(0:1) phase.

Figure 2: Misaligned and Aligned K28.5 Characters



Loopback Operation

Loopback operation is controlled by PLUP (Parallel Loopback) and SLPN (Serial Loopback) as shown in Table 1. When PLUP=0 and SLPN=1 the part is configured for normal operation. When PLUP=1 and SLPN=1, SOi is internally looped to SIi and the SOi outputs are held HIGH. When PLUP=0 and SLPN=0, SIi is looped to SOi after retiming in the clock recovery unit. Although retiming removes much of the input jitter, the SOi outputs may not meet jitter specifications listed in the "Transmitter AC Specifications" due to low frequency jitter transfer from SIi to SOi. When PLUP=1 and SLPN=0 (both loopback paths are active) the clock recovery unit is used to retime the internally looped SOi data. The SIi inputs are looped directly to the SOi outputs without retiming. Jitter on SOi in this mode of operation will depend heavily on SIi jitter, and again the SOi outputs may not meet jitter specifications. The remote receiver will see the total jitter accumulation across both the incoming and outgoing serial links.

Table 1: Loopback Selection

PLUP	*SLPN*	*Transmitter Source*	*Receiver Source*
LOW	LOW	Receiver (Retimed)	Receiver
LOW	HIGH	Transmitter	Receiver
HIGH	LOW	Receiver (Not Retimed)	Transmitter
HIGH	HIGH	HIGH	Transmitter

JTAG Access Port

A JTAG access port is provided to assist in board-level testing. Through this port most pins can be observed or controlled and all TTL outputs can be tri-stated. A full description of the JTAG functions on this device is available in "VSC7185 JTAG Access Port Functionality." Circuits designed exclusively for the HDMP-1685A will automatically disable the JTAG port. Table 7 (Pinout Definitions) in this datasheet shows the proper connections for either HDMP-1685A emulation or for JTAG functionality (in parentheses).

AC Characteristics

Figure 3: Transmit Timing Waveforms

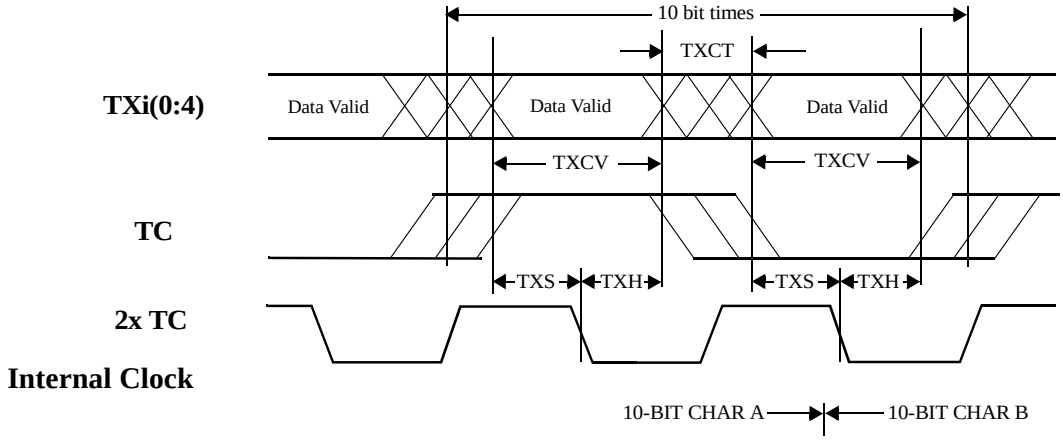


Table 2: Transmitter AC Characteristics

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
T_{TXCT}	TXi(0:4) Input Data and TC Clock Transition Range	—	—	2.0	bits	
T_{TXCV}	TXi(0:4) Input Data and TC Clock Valid Time	3.0	—	—	bits	
T_{TXS}	TXi(0:4) Input Data and TC Setup Time to Internal 2x Clock	700	—	—	ps	
T_{TXH}	TXi(0:4) Input Data and TC Hold Time to Internal 2x Clock	700	—	—	ps	
	TC Duty Cycle	35	—	65	%	
T_{TXLAT}	Transmitter Latency	11 bits + 1ns	—	11 bits + 2ns	—	

Figure 4: Receive Timing Waveforms

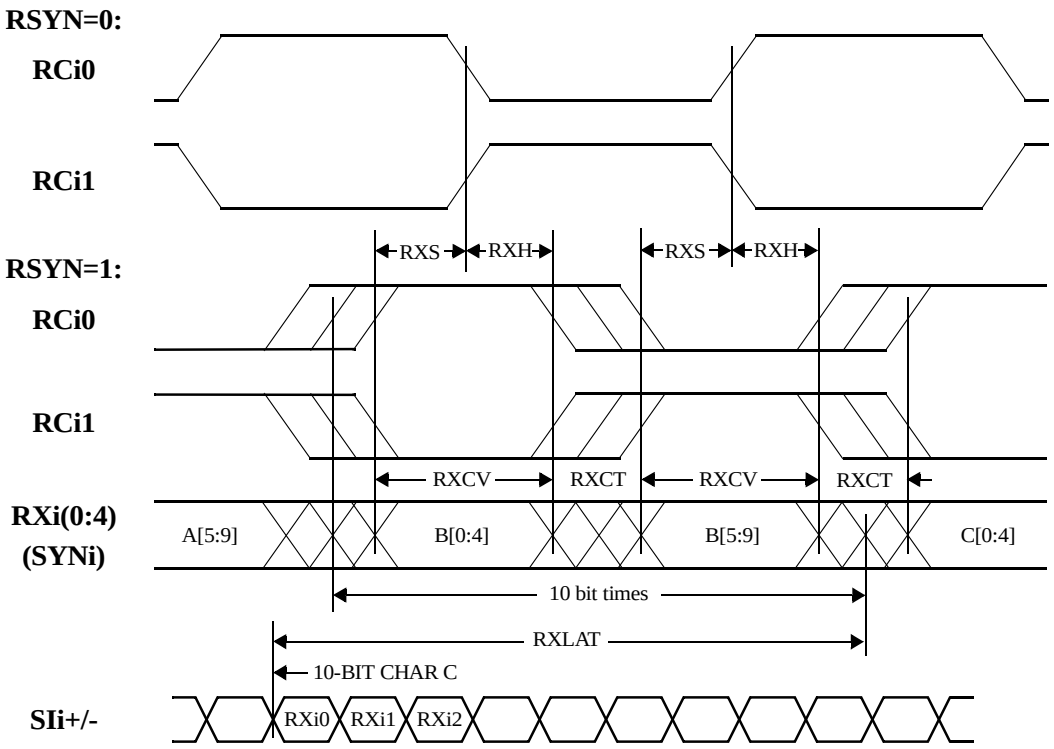


Table 3: Receive AC Characteristics

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
f_lock	Frequency Lock Time from Power On	—	—	500	µs	
B_sync	Bit Sync Time	—	—	2500	bits	
T_{RXS}	RXi(0:4) Setup Time (Data Valid Before Clock)	1.50	—	—	bits	RSYN=0
T_{RXH}	RXi(0:4) Hold Time (Data Valid After Clock)	1.50	—	—	bits	RSYN-0
T_{RXCT}	RXi(0:4) and RCi(0:1) Transition Range	—	—	1.25	bits	RSYN=1
T_{RXCV}	RX(0:4) and RCi(0:1) Valid Time	3.75	—	—	bits	RSYN=1
	RC0 to RC1 Skew	-0.5	—	+0.5	ns	
	RC0 or RC1 Duty Cycle	40	—	60	%	
T_{RXLAT}	Receiver Latency	18.5 bits + 2 ns	—	19.5 bits + 5 ns	—	

Figure 5: RFCT and TC Waveforms

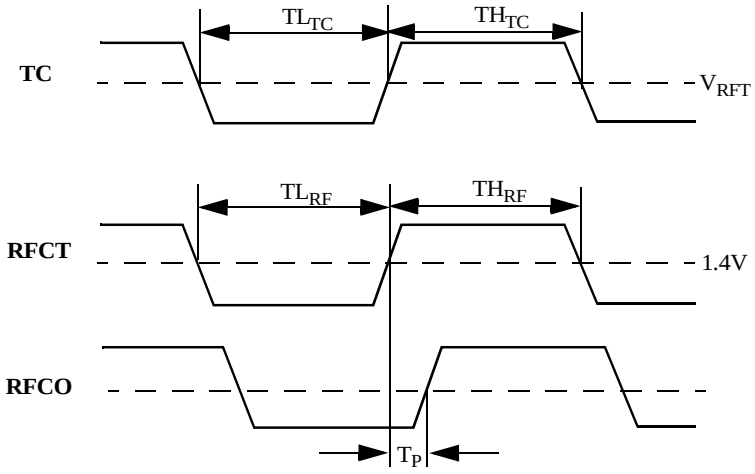


Table 4: Reference Clock Requirements

Parameters	*Description*	*Min*	*Typ*	Max	Units	*Conditions*
FR	Frequency Range	105	—	136	MHz	Range over which both transmit and receive reference clocks on any link may be centered (R_{FCM} = 1).
FO	Frequency Offset	–200	—	200	ppm	Maximum frequency offset between transmit and receive reference clocks on one link.
T_P	Delay from RFCT to RFCO	TBD	—	TBD	ns	
TL_{RO}/TH_{RO}	RFCO Duty Cycle	35	—	65	%	
TR_{RO}/TF_{RO}	RFCO Rise and Fall Time	0.25	—	1.5	ns	Between V_{RFT} ±180mV.
TL_{TC}/TH_{TC}	TC Duty Cycle	35	—	65	%	Measured at V_{RFT}
TL_{RF}/TH_{RF}	RFCT Duty Cycle	35	—	65	%	Measured at 1.4V
TR_{TC},TF_{TC}	TC Rise and Fall Time	—	—	0.45	ns	Between V_{RFT} ±180mV
TR_{RF},TF_{RF}	RFCT Rise and Fall Time	—	—	1.5	ns	Between V_{RFT} ±180mV

Table 5: DC Characteristics

Parameters	*Description*	*Min.*	*Typ*	*Max.*	*Units*	*Conditions*
SSTL-2 Inputs						
V_{RFT}	SSTL-2 input reference voltage	1.15	1.25	1.35	V	
V_{IH}	SSTL-2 input HIGH voltage	V_{RFT} + 0.18	—	V_{CC} + 0.30	V	
V_{IL}	SSTL-2 input LOW voltage	–0.30	—	V_{RFT}–0.18	V	
SSTL-2 Outputs						
VRFR	SSTL-2 output reference voltage	1.15	1.25	1.35	V	
V_{OH}	SSTL-2 output HIGH voltage	V_{RFR} + 0.35	—	2.70	V	Min: 50Ω to V_{RFR}
V_{OL}	SSTL-2 output LOW voltage	GND	—	V_{RFR}– 0.35	V	Max: 50Ω to V_{RFR}
TTL Inputs						
V_{IH}	TTL input HIGH voltage	2.0	—	5.5	V	5V Tolerant Inputs
V_{IL}	TTL input LOW voltage	0	—	0.8	V	
I_{IH}	TTL input HIGH current	—	50	500	µA	V_{IN} = 2.4V
I_{IL}	TTL input LOW current	—	—	–500	µA	V_{IN} = 0.5V
TTL Outputs						
V_{OH}	TTL output HIGH voltage	2.4	—	—	V	I_{OH} = –1.0mA
V_{OL}	TTL output LOW voltage	—	—	0.5	V	I_{OL} = +1.0mA
PECL Inputs (RFC+/RFC–)						
V_{IH}	PECL input HIGH voltage	V_{CC} – 1.1	—	V_{CC} – 0.7	V	
V_{IL}	PECL input LOW voltage	V_{CC} – 2.0	—	V_{CC} – 1.5	V	
I_{IH}	PECL input HIGH current	—	—	200	µA	V_{IN} =$V_{IH(MAX)}$
I_{IL}	PECL input LOW current	–50	—	—	µA	V_{IN} =$V_{IL(MIN)}$
ΔV_{IN}	PECL input differential peak-to-peak voltage swing	400	—	—	mV	$V_{IH(MIN)} - V_{IL(MAX)}$
High-Speed Outputs						
ΔV_{OUT75}(1)	TX Output differential peak-to-peak voltage swing	1200	—	2200	mV p-p	75Ω to V_{CC} – 2.0 V (TX+) – (TX–)
ΔV_{OUT50}(1)	TX Output differential peak-to-peak voltage swing	1000	—	2200	mV p-p	50Ω to V_{CC} – 2.0 V (TX+) – (TX–)
High-Speed Inputs						
ΔV_{IN}(1)	PECL differential peak-to-peak input voltage swing	200	—	2600	mV	SIi+ – SIi–
Miscellaneous						
V_{CC}	Power supply voltage	3.14	—	3.47	V	3.3V ±5%
P_D	Power dissipation	—	—	2.7	W	V_{DD} = 3.47V, Freq = 1.36Gb/s, outputs open, temp = 100°C case
I_{DD}	Supply current (all supplies)	—	—	779	mA	
I_{DDA}	Supply current on V_{CCA}	—	100	—	mA	

Note: (1) Refer to Application Note, AN-37, for differential measurement techniques.

Absolute Maximum Ratings (1)

Power Supply Voltage (V_{CC})..... -0.5V to +4V
DC Input Voltage (PECL inputs)..... –0.5V to V_{CC}+0.5V
DC Input Voltage (TTL inputs)..... –0.5V to +5.5V
DC Input Voltage (SSTL-2 inputs)..... –0.5V to V_{CC}+0.5V
DC Output Voltage (TTL outputs)..... –0.5V to V_{CC}+0.5V
DC Output Voltage (SSTL-2 outputs)..... –0.5V to V_{CC}+0.5V
Output Current (PECL outputs)..... ±50mA
Output Current (TTL outputs)..... ±50mA
Output Current (SSTL-2 outputs)..... ±50mA
Case Temperature Under Bias..... -55^{o} to $+125^{o}$C
Storage Temperature..... -65^{o}C to $+150^{o}$C

NOTES: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltage ($V_{CC)}$).....+3.3V ±5%
Operating Temperature Range ..... 0^{o}C Ambient to $+100^{o}$C Case Temperature

Table 6: Pin Table

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	GND	VCC	GND	SYN1	RC10	RX10	RX14		VCR1	VCC	GND	RX21	VCR2		GND	VCR2	GND
B				GND	RC11	RX11	VCR1		GND	SYN2	RX20	RX22			SYN3	RC30	RC31
C	RX04			VCR0	VCR1	RX12	GND		SLPN	RC20	VCR2	RX23		VCC	VCR3	GND	RX30
D	RX00	RX01	VCR0	GND	GND	RX13	VRFR		NC (TMS)	RC21	GND	RX24		RX31	RX32	RX33	RX34
E	RC00	RC01	RX02	RX03										VCR3	GND		
F		SYN0	VCR0	GND													GND
G			GND	VCC										TX22	TX21	TX20	VCR3
H	TX14															TX24	TX23
J	TX10	TX11	TX12	TX13										VCC			
K		NC (TDO)	GND	GND										GND	GND	VCC	TC
L			GND	VCC										TX33	TX32	TX31	TX30
M	TX04																TX34
N	TX00	TX01	TX02	TX03										PLUP	VCC		
P	VRFT	RFCM	RFC-	GND	SO0-	GND	SO1-	GND	CAP0	GND	SO2+	GND	SO3+		NC (TDI)	RFCO	RSYN
R	RFCT	RFC+	GND	VCC	SO0+	GND	SO1+	GNDA	CAP1	GND	SO2-	GND	SO3-	VCC	GND (TRSTN)	VCCTR	SYNC
T		GND	VCC	VCC	VCP0	GND	VCP1	GND	VCCA	GND	VCP2	GND	VCP3	VCC	GND	GND	NC (TCK)
U	GND	GND	SI0-	SI0+	VCC	SI1-	SI1+	GND	GND	SI2-	SI2+	GND	SI3-	SI3+	GND	GND	GNDTR

NOT POPULATED

Table 7: Pin Description

Pin	*Name*	*Description*
N1, N2 N3, N4 M1	TX00, TX01 TX02 TX03 TX04	INPUT - SSTL-2: 5-Bit Transmit bus for Channel 0. Input timing is referenced to the TC input. TX00 is transmitted first.
J1, J2 J3, J4 H1	TX10, TX11 TX12, TX13 TX14	INPUT - SSTL-2: 5-Bit Transmit Bus for Channel 1. Input timing is referenced to the TC input. TX10 is transmitted first.
G16, G15 G14, H17 H16	TX20, TX21 TX22, TX23 TX24	INPUT - SSTL-2: 5-Bit Transmit Bus for Channel 2. Input timing is referenced to the TC input. TX20 is transmitted first.
L17, L16 L15, L14 M17	TX30, TX31 TX32, TX33 TX34	INPUT - SSTL-2: 5-Bit Transmit Bus for Channel 3. Input timing is referenced to the TC input. TX30 is transmitted first.
K17	TC	INPUT - SSTL-2: Transmit Low-Speed Input Clock for TXi(0:4).
R1	RFCT	INPUT - TTL: TTL Reference Clock. The rising edge of RFCT provides the reference clock, at 1/10th or 1/20th of the baud rate (depending on RFCM) to the clock multiplying PLL. If RFCT is used, pull RFC+ HIGH and leave RFC- open. If RFC+ and RFC- are used, pull RFCT HIGH or leave open.
R2 P3	RFC+ RFC-	INPUT - PECL: PECL Differential Reference Clock. The rising edge of RFC+ (falling edge of RFC-) provides the reference clock, at 1/10th or 1/20th of the baud rate (depending on RFCM) to the clock multiplying PLL. If RFC+ and RFC- are used, pull RFCT HIGH or leave open. If RFCT is used, pull RFC+ HIGH and leave RFC- open.
P2	RFCM	INPUT - SSTL-2: Reference Clock Mode Select. When LOW, REF is at 1/20th of the transmit baud rate (e.g., 62.5MHz for 1.25Gb/s). When HIGH, REF is at 1/10th the baud rate (e.g., 125MHz for 1.25Gb/s).
P17	RSYN	INPUT - SSTL-2: Receive Byte Clock Synchronization Control. When LOW, RXi(0:4) and SYNi data transitions are centered around RCi(0:1) clock transitions. When HIGH, RXi(0:4) and SYNi data transitions are aligned with RCi(0:1) transitions, so that receive interface timing resembles transmit interface timing.
P16	RFCO (NC)	OUTPUT - TTL: This is an identical copy of the transmit baud rate clock divided by 10. (NC for HDMP-1685 socket.)
R5, P5 R7, P7 P11, R11 P13, R13	SO0+, SO0- SO1+, SO1- SO2+, SO2- SO3+, SO3-	OUTPUT - Differential PECL: AC-Coupling recommended. These pins output the serialized transmit data for Channel x when PLUP is LOW. When PLUP is HIGH, SO+ is HIGH and SO- is LOW.

Pin	Name	Description
D1, D2 E3, E4 C1	RX00, RX01 RX02, RX03 RX04	OUTPUT - SSTL-2: 5-Bit Receive Bus for Channel 0. Parallel data on this bus is synchronous to RC00 and RC01. RX00 is the first bit received.
A6, B6 C6, D6 A7	RX10, RX11 RX12, RX13 RX14	OUTPUT - SSTL-2: 5-Bit Receive Bus for Channel 1. Parallel data on this bus is synchronous to RC10 and RC11. RX10 is the first bit received.
B11, A12 B12, C12 D12	RX20, RX21 RX22, RX23 RX24	OUTPUT - SSTL-2: 5-Bit Receive Bus for Channel 2. Parallel data on this bus is synchronous to RC20 and RC21. RX20 is the first bit received.
C17, D14 D15, D16 D17	RX30, RX31 RX32, RX33 RX34	OUTPUT - SSTL-2: 5-bit Receive bus for Channel 3. Parallel data on this bus is synchronous to RC30 and RC31. RX30 is the first bit received.
E1 E2	RC00 RC01	OUTPUT - SSTL-2: Recovered complementary clocks for Channel 0 at $1/10^{th}$ the incoming baud rate. Synchronous to RX0(0:4) and SYN0.
A5 B5	RC10 RC11	OUTPUT - SSTL-2: Recovered complementary clocks for Channel 1 at $1/10^{th}$ the incoming baud rate. Synchronous to RX1(0:4) and SYN1.
C10 D10	RC20 RC21	OUTPUT - SSTL-2: Recovered complementary clocks for Channel 2 at $1/10^{th}$ the incoming baud rate. Synchronous to RX2(0:4) and SYN2.
B16 B17	RC30 RC31	OUTPUT - SSTL-2: Recovered complementary clocks for Channel 3 at $1/10^{th}$ the incoming baud rate. Synchronous to RX3(0:4) and SYN3.
U4, U3 U7, U6 U11, U10 U14, U13	SI0+, SI0- SI1+, SI1- SI2+, SI2- SI3+, SI3-	INPUT - Differential PECL (AC-Coupling recommended): Serial receive data inputs for Channel x which are selected when PLUP is LOW. [Internally biased to VCC/2]
N14	PLUP	INPUT - SSTL-2: Parallel Loopback Enable input. SIi is input to the CRU for Channel x (normal operation) when PLUP is LOW. When HIGH, internal loopback paths from SOi to SIi are enabled. Refer to Table 1.
C9	SLPN	INPUT - SSTL-2: Serial Loopback Enable Input. Normal operation when HIGH. When LOW, SIi is looped back to SOi internally for diagnostic purposes. Refer to Table 1 and related description.
R17	SYNC	INPUT - SSTL-2: Enables SYNi and Word Alignment when HIGH. When LOW, keeps current word alignment and disables SYNi (always LOW).
F2 A4 B10 B15	SYN0 SYN1 SYN2 SYN3	OUTPUT - SSTL-2: Comma Detect for Channel i. This output goes HIGH for both half-characters to indicate that a comma character (‘0011111XXX’) has been detected. SYNi is enabled when SYNC is HIGH.
P9 R9	CAP0 CAP1	ANALOG: Loop Filter capacitor for the Clock Multiply Unit. Typically 0.1µF connected between CAP0 and CAP1. Amplitude is less than 3.3V.

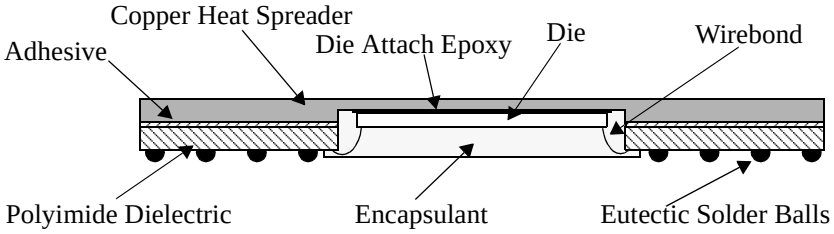
Pin	*Name*	*Description*
T17	TCK (NC)	INPUT - TTL: JTAG Test Clock (NC for Non-JTAG operation)
D9	TMS (NC)	INPUT - TTL: JTAG Test Mode Select (NC for Non-JTAG operation)
R15	TRSTN (GND)	INPUT - TTL: JTAG Test Reset, Active Low (Gnd for Non-JTAG operation)
P15	TDI (NC)	INPUT - TTL: JTAG Test Data Input (NC for Non-JTAG operation)
K2	TDO (NC)	OUTPUT - TTL: JTAG Test Data Output (NC for Non-JTAG operation)
T9	VCCA	Analog Power Supply
R8	GNDA	Analog Ground. Tie to common ground plane with GND.
A2, A10, C14 G4, J14, K16 L4, N15, R4 R14, T3, T4 T14, U5	VCC	Digital Logic Power Supply
C4, D3, F3 A9, B7, C5 A13, A16, C11 C15, E14, G17	VCR0 VCR1 VCR2 VCR3	RX TTL Output Power Supply
D7	VRFR	RX Parallel Interface SSTL-2 Reference Voltage
P1	VRFT	TX Parallel Interface SSTL-2 Reference Voltage
T5 T7 T11 T13	VCP0 VCP1 VCP2 VCP3	PECL I/O Power Supply for Channel x
R16	VCCTR (VCC)	TTL Output Power Supply for RFCO (V_{CC} for HDMP-1685 socket)
U17	GNDTR (GND)	TTL Ground for RFCO (GND for HDMP-1685 socket)
A1, A3, A11 A15, A17, B4 C7, C16, D4 D11, E15, F4 B9, F17, G3, K3 K14, K15, L3 P6, P8, P10, P12 R6, R10, R12 T2, T6, T8, T10 T12, T15, T16 U1, U2, U8, U9 U12, U15, U16 R3, P4, K4, D5	GND	Ground

Pin	*Name*	*Description*
M2, M3, M4 L1, L2, H2, H3 H4, G1, G2 H15, H14, J17 J16, J15, M16 M15, M14, N17 N16, K1, F1, C2 C3, B1, B2, B3 A8, B8, C8, D8 B13, C13, D13 A14, B14, E16 E17, F14, F15 F16, P14, T1	N/C	No Connects

Package Thermal Characteristics

The VSC7185 is packaged in a 23mm BGA package with 1.27mm eutectic ball spacing. The construction of the package is shown in Fugure 6.

Figure 6: Package Cross Section



The VSC7185 is designed to operate with a case temperature up to 100°C. In order to comply with this target, the user must guarantee that the case temperature specification of 100°C is not violated. With the Thermal Resistances listed in Table 8, the VSC7185 can operate in still air ambient temperatures of 40°C [40°C = 100°C - 2.5W * 24°C/W]. If the ambient air temperature exceeds these limits, then some form of cooling through a heatsink or an increase in airflow must be provided.

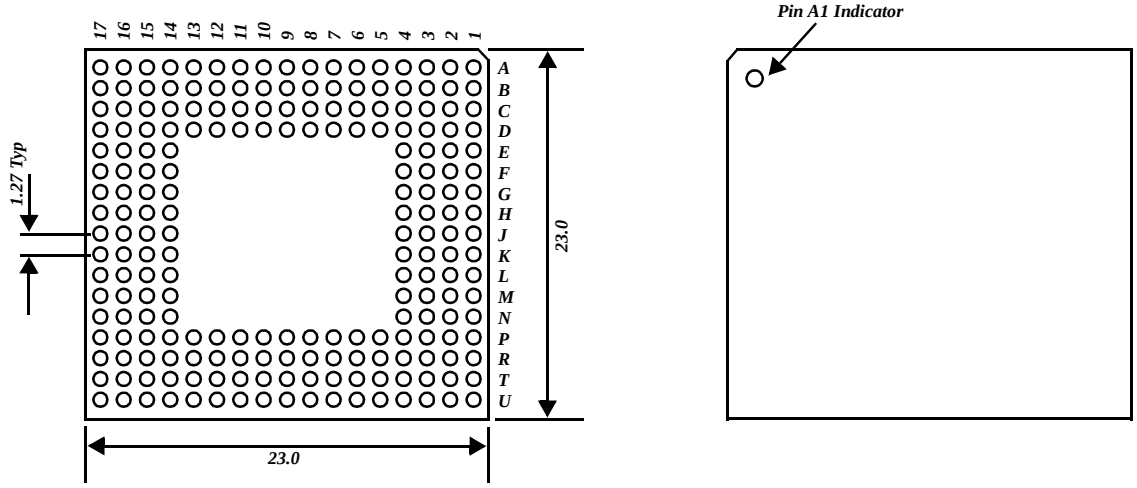
Table 8: Thermal Resistance

Symbol	*Description*	*Value*	*Units*
θ_{jc}	Thermal resistance from junction-to-case	~1.0	°C/W
θ_{ca}	Thermal resistance from case-to-ambient in still air including conduction through the leads.	24	°C/W
$\theta_{ca\text{-}100}$	Thermal resistance from case-to-ambient with 100 LFM airflow	21	°C/W
$\theta_{ca\text{-}200}$	Thermal resistance from case-to-ambient with200 LFM airflow	18.5	°C/W
$\theta_{ca\text{-}400}$	Thermal resistance from case-to-ambient with 400 LFM airflow	17	°C/W
$\theta_{ca\text{-}600}$	Thermal resistance from case-to-ambient with 600 LFM airflow	15	°C/W

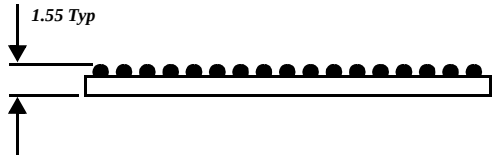
Moisture Sensitivity Level

This device is rated at a Moisture Sensitivity Level 3 rating with maximum floor life of 168 hours at 30ºC, 60% relative humidity. Please refer to Application Note AN-20 for appropriate handling procedures.

Package Information

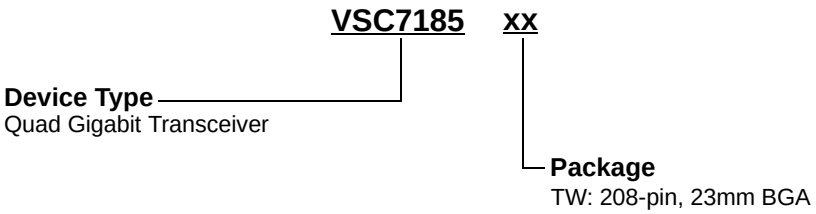


BOTTOM VIEW ***TOP VIEW***



Ordering Information

The part number for this product is formed by a combination of the device number and the package style:



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