Advance Product Information

VSC6511

SMPTE-292M Serializer, Deserializer, and Deserializer/Reclocker at 1.485Gb/s

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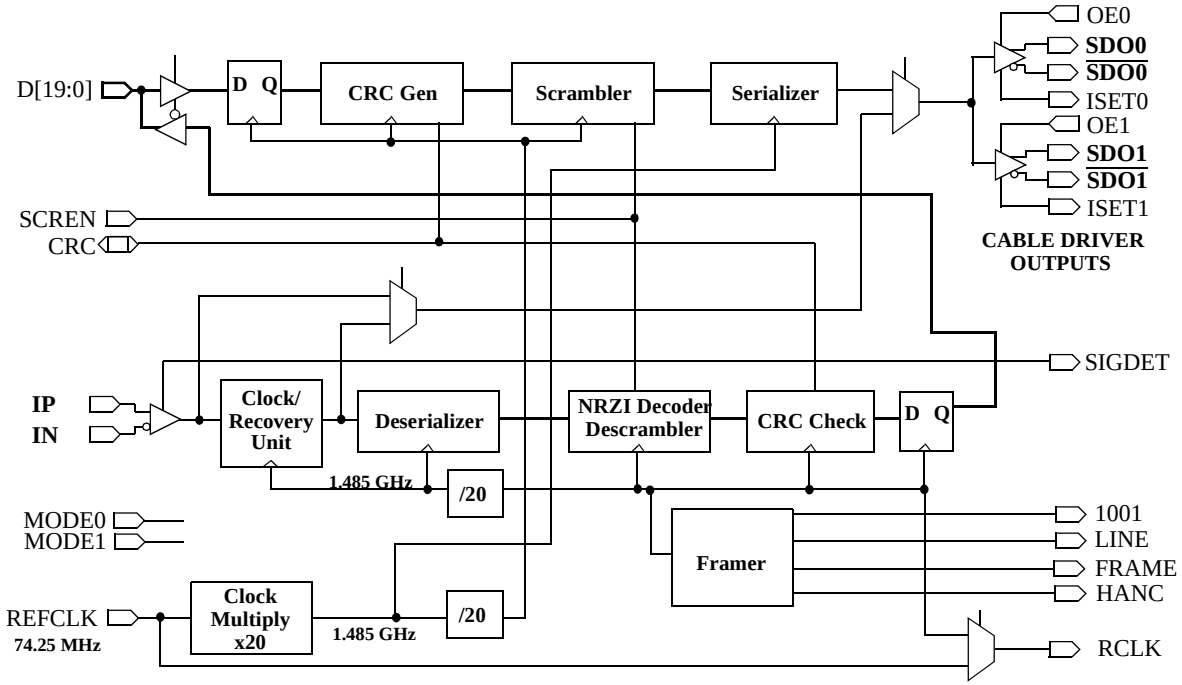
Features

- Compliant with SMPTE-292M @ 1.485Gb/s
- Multiple Functions: Serializer, Deserializer, and Deserializer with Reclocker
- 20 Bit TTL Interface @ 74.25 MHz
- Scrambler / Descrambler with ENABLE
- CRC Generator/Checker with ENABLE
- Data Framer aligns data and provides TRS on SAV/EAV events
- Clock Multiplier and Recovery Units
- 2 or 4 configurable 75ohm cable driver o/ps
- 3.3V, Low power--700-1500mW typical
- 64-pin, 10x10x1.0mm Exposed Pad TQFP

General Description

The VSC6511 multi function SMPTE-292M compatible IC with Serializer, Deserializeror, or Deserializer with reclocker modes which operate at 1.485Gb/s. As a Serializer, 20-bits of data (D19:0) are latched into the part on the rising edge of REFCLK then scrambled and serialized out SDO0/$\overline{\text{SDO0}}$ and/or SDO1/$\overline{\text{SDO1}}$. An optional CRC Generator may be enabled. As a Deserializer, serial data on SDI/$\overline{\text{SDI}}$ is recovered, de-scrambled and deserialized onto D[19:0]. Frame alignment on SAV/EAV, line detection and frame detection outputs are provided. As a Deserializer with reclocker, the device functions as ain the deserializer mode above and serial data on SDI/$\overline{\text{SDI}}$ is recovered and retransmitted on SDO0/$\overline{\text{SDO0}}$ and/or SDO1/$\overline{\text{SDO1}}$.

VSC6511 Block Diagram



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Functional Description

The VSC6511 is a multifunction SMPTE-292M device which can be configured for different modes of operation: Serializer, Deserializer, or Deserializer/Reclocker. Only one mode is available at a time. A discussion of the individual building blocks of the device will be followed with specific configurations.

Clock Multiplier Unit (CMU)

The CMU generates the internal 1.485 GHz baud rate clock from the 74.25 MHz TTL REFCLK input. The rising edges of the REFCLK are used by a PLL which multiplies the frequency by a factor of 20. This internal baud rate clock is used by the Serializer, Deserializer and Reclocker. An off-chip 0.1uF capacitor sets the loop bandwidth of the CMU. REFCLK should be a high quality, low jitter signal with sharp rise times in order to minimize the amount of jitter transferred from the REFCLK through the CMU to the serializer. This optimizes the signal quality at the output of the serializer.

A secondary function of the CMU is to divide the baud rate clock by 20 to produce an internal 74.25 MHz clock which is frequency locked and phase aligned to REFCLK. This internal clock is used to latch the 20-bit data bus D[19:0] into the input register of the Serializer.

REFCLK is also buffered onto the RCLK output when in Serializer or Reclocker mode. This allows multiple devices to be daisy-chained in order to simplify REFCLK distribution to an array of devices.

CRC Generator

The twenty bits of transmit data from the input register is fed into a CRC Generator which calculates the CRC and substitutes the value into the proper location within the video line. The CRC polynomial is CRC(X)= $(X^{18} + X^5 + X^4 + 1)$. A controller monitors SAV/EAV position and uses this to control the CRC generator and insertion of the CRC result into the line. The CRC Generator is enabled only in Serializer Mode when CRC is HIGH. In other modes, or if CRC is LOW, the CRC Generator is disabled and powered down. CRC is a bidirectional pin.

Scrambler and NRZI Encoder

The twenty bits out of the CRC Generator are sent to the parallel Scrambler where the data is scrambled and NRZI encoded using the combined generator polynomial of $G(x)=(x^9 + x^4 +1)(x+1)$. Scrambling is enabled only when in Serializer Mode if SCREN is HIGH. Scrambling is disabled when SCREN is LOW and in other modes.

Serializer

The data from the Scrambler is converted from 20-bits at 74.25 Mb/s to 1 bit at 1.485 Gb/s by the Serializer with D0 being transmitted first. Two differential PECL-style serial outputs are provided for transporting the 1.485 Gb/s signal. These outputs SDO0/$\overline{\text{SDO0}}$ and SDO1/$\overline{\text{SDO1}}$ are supplied data from the serializer (in Serializer mode) or the CRU of the Reclocker (in Deserializer/Reclocker mode). Each output, SDO0 and SDO1, have independent TTL inputs, OE0 and OE1, which when HIGH enable the outputs and when LOW disable the outputs. When disabled, the output buffer will be powered down and both legs will float HIGH.

Each output is compliant with the SMPTE-292M cable driver specification when driving 75 ohm loads. In this application, a TBD ohm resistor should be connected from the ISET0/ISET1 pin to ground in order to control the current in the differential output amplifier. By lowering the ISET resistor, higher output swings may be realized.

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Serial Input

The differential PECL-style input, SDI/$\overline{\text{SDI}}$, is the input source for 1.485 Gb/s SMPTE-292M data in the Deserializer and Reclocker modes. This input is ignored in Serializer mode.

Clock Recovery Unit

The serial data on the SDI/$\overline{\text{SDI}}$ input is sent to the digital Clock Recovery Unit (CRU) which extracts the clock and retimes the data. This digital CRU is completely monolithic and requires no external components. Furthermore, it automatically locks onto data when present and locks to REFCLK when data is not present. This eliminates the need for the system to control the CRU. The CRU is enabled only in the Deserializer and Deserializer/Reclocker modes.

Deserializer

The reclocked serial bit stream is deserialized into a 20-bit parallel character. D0 is serially received prior to D1. The VSC6511 provides a TTL recovered clock, RCLK at one twentieth of the serial baud rate. This clock is generated by dividing down the high-speed clock from the CRU which is phase locked to the serial data. The deserializer is enabled only in the Deserializer and Deserializer/Reclocker modes.

If serial input data is not present, or does not meet the required baud rate, the VSC6511 will continue to produce a recovered clock so that downstream logic may continue to function. The RCLK output frequency under these circumstances will differ from their expected frequency by less than $\pm$1%.

Descrambler and NRZI Decoder

The VSC7152 contains a descrambler/NRZI Decoder which processes the recovered serial data and outputs unscrambled and NRZI decoded serial data from the deserializer. The serial scrambled data is descrambled/NRZI decoded assuming data has been scrambled/NRZI encoded with the following combined generator polynomial: $G(x)=(x^9+x^4+1)(x+1)$. Descrambling is enabled with the SCREN input is HIGH and disabled when LOW. The descrambler is enabled only in the Deserializer mode.

CRC Checker

The 20-bit data from the Descrambler is sent to the CRC Checker where a running CRC checksum is continuously calculated. As 20-bit data is sent out of the chip, the CRC output pin is asserted if the checksum did not meet the value expected. This error is asserted from the first CRC Error until the end of the line. A controller monitors the 20-bit data out of the serializer for SAV/EAV frames in order to control the CRC Checker. The CRC Checker is enabled only in Deserializer and Deserializer/Reclocker modes.

Frame Aligner

The VSC6511 monitors the serial data stream for SAV/EAV characters. These characters should be located within each line of video data. If SAV/EAV is not detected within the period of one line, the Framer sends a signal to the Deserializer to shift the data one bit. The Framer then looks for SAV/EAV and the process repeats until properly detected. Without these patterns, serial data is not aligned in any way with the parallel outputs. The Framer outputs a once-per-line (LINE), Horizontal ANCilliary period (HANC), 1.001/1.000 output (1.001) and a once-per-frame (FRAME) signal indicating the detection of the proper synchronization pulse in the data. Framing is enabled only in Deserializer mode.

The Frame Aligner also outputs the LINE, FRAME and HANC outputs signals. The timing of these signals is indicated below.

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Table 1: Frame Aligner Output Timing

	D10-19	*D0-9*	*LINE*	*FRAME*	*HANC*	*CRCERR*
ACTIVE VIDEO	DATA	DATA	0	0	0	0
	---	---	0	0	0	0
	DATA	DATA	0	0	0	0
EAV	3FF	3FF	0	0	0	0
	000	000	0	0	0	0
	000	000	0	0	0	0
	XYZ	XYZ	0	0	0	0
LINE	LN0	LN0	0	0	0	0
	LN1	LN1	1	1*	0	0
CRC	CRC0	CRC0	0	0	0	0
	CRC1	CRC1	0	0	0	0 or 1
HORIZ BLANK	DATA	DATA	0	0	1	0
	---	---	0	0	1	0
	DATA	DATA	0	0	1	0
SAV	3FF	3FF	0	0	0	0
	000	000	0	0	0	0
	000	000	0	0	0	0
	XYZ	XYZ	0	0	0	0
ACTIVE VIDEO	DATA	DATA	0	0	0	0
	DATA	DATA	0	0	0	0
	---	---	0	0	0	0

* FRAME is HIGH only if LN0/LN1 indicates the first line of a frame.
** CRCERR is HIGH only during CRC1 if the CRC is incorrect.

D[19:0] Databus

As mentioned previously, in Serializer mode D[19:0] is configured as a input. In Deserializer mode, D[19:0] is configured as an output.

Application Information

The VSC6511 cable driver output is intended to fully comply with the SMPTE-292M cable driver specifications. This includes an 800mV swing and a return loss of more than 15dB. The circuit shown below shows how to connect the output of the VSC6511 to the 75 ohm cable and downstream device. The output of the VSC6511 is actually 1200mV. The output termination circuit shown below attenuates the output signal to 800mV and ensures a return loss better than -15dB. The ISET resistor is 1.78K

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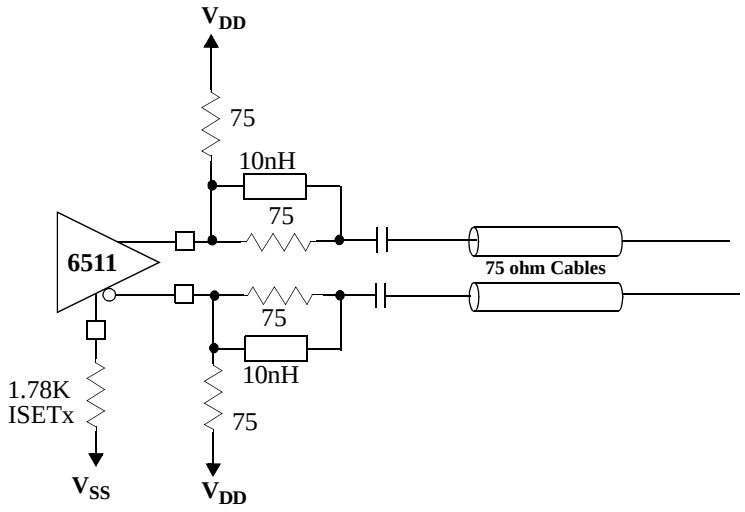
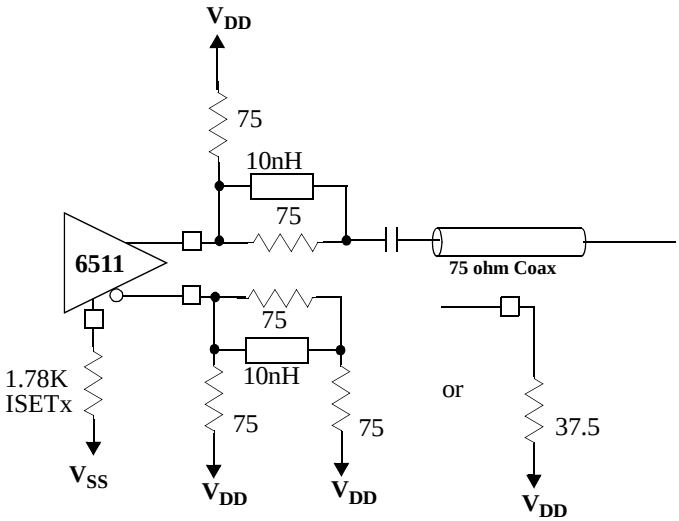
Figure 1: High Speed Interconnect Example (Differential)



NOTE: All resistors are 1%
WARNING: SUBJECT TO CHANGE

Figure 2: High Speed Interconnect Example (Single Ended)



NOTE: All resistors are 1%
Optional use of external Voltage Reference provides tighter swing tolerance

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The output swing of the VSC6511 is controlled through the ISETx pins and a VREF input. By connecting an 1.78K ohm resistor, 1%, between VSS and ISETx the output swing will be controlled to within 800mV +/- 7%. An optional bandpass voltage reference may be used to further tighten the output swings by accurately driving the VREF input.

Configuration Modes:

The MODE(1:0) inputs configure the VSC6511 into its different modes of operation. The table below summarizes the different signals and circuits in the VSC6511 that change function in the different modes.

Table 2: Mode Configuration Features: Serializer Mode

SIGNAL/CIRCUIT	*DESERIALIZER MODE*	*DESERIALIZER/ RECLOCKER MODE*	*SERIALIZER MODE*
MODE1 MODE0	HIGH HIGH	LOW HIGH	LOW LOW
D[19:0] Data Bus	20-BIT OUTPUT	20-BIT OUTPUT	20-BIT INPUT
SDO0/SDO1 Serial Outputs	NOT USED, DISABLED	SOURCE IS CRU OUTPUT OR SDI/$\overline{\text{SDI}}$	SOURCE IS SERIALIZER
RCLK Output	RECOVERED CLOCK FROM CRU	RECOVERED CLOCK FROM CRU	BUFFERED REFCLK
CRU Bypass Mux	NOT ACTIVE	CRU OUTPUT GOES TO SDO0/SDO1	CRU NOT ACTIVE
SDI Serial Input	ACTIVE	ACTIVE	IGNORED
CRC	CRC is an error output	CRC is an error output	Enables CRC Generator
SIGDET Output	ACTIVE	ACTIVE	DISABLED LOW
1.001 Output	ACTIVE	ACTIVE	DISABLED LOW
FRAME Output	ACTIVE	ACTIVE	DISABLED LOW
LINE Output	ACTIVE	ACTIVE	DISABLED LOW
HANC Output	ACTIVE	ACTIVE	DISABLED LOW

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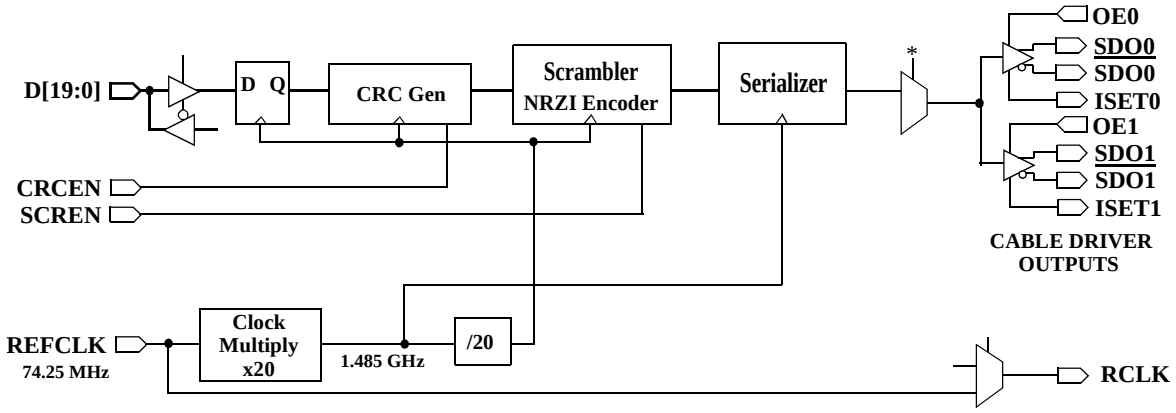
Features: Serializer Mode

1. 20 Bit TTL Interface @ 74.25 MHz
2. On-chip Clock Multiplier Unit
3. On-Chip Scrambler and NRZI Encoder with ENABLE
4. CRC Generator with ENABLE
5. 2 or 4 user configurable 75ohm cable driver outputs
6. Output Signal Detect indicators
7. Buffered REFCLK output for easy clock distribution
8. 700 mW Typical Power

Description

The VSC6511 can be configured as a 20-bit HDTV Serializer using the MODE[1:0] pins. A 74.25 MHz TTL REFCLK is multiplied by 20 in the Clock Multiplier Unit (CMU) to generate a 1.485 GHz bit rate clock. The CMU aligns a divided-by-20 clock with REFCLK in order to latch the 20-bit TTL data bus D[19:0] into the Input Register. When enabled by CRC being HIGH, the data is monitored for SAV/EAV and a CRC checksum is calculated and inserted into the data stream at the appropriate point in each video line. The data is then scrambled and NRZI encoded, only if this stage is enabled by SCREN=HIGH. The data is then serialized and output on the differential outputs, SDO0/$\overline{\text{SDO0}}$ and SDO1/$\overline{\text{SDO1}}$, which are compliant with the SMPTE 292M cable driving specifications. The scrambler and NRZI encoder can be disabled by setting the TTL input, SCREN to LOW. The SDO0/$\overline{\text{SDO0}}$ output can be disabled and forced HIGH by setting the TTL input OE0 to LOW. Similarly, the SDO1/$\overline{\text{SDO1}}$ output can be disabled and forced HIGH by setting the TTL input OE1 to LOW.

Figure 3: Serializer Mode



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Functional Description: Serializer Mode

The following functional blocks are used in the Serializer mode of operation. Please refer to the Functional Description at the beginning of this document for the a description of each of these blocks.

Clock Multiplier Unit (CMU)
CRC Generator
Scrambler and NRZI Encoder
Serializer
Cable Driver Outputs

Table 3: Transmit AC Characteristics (Serializer Mode)

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
T_1	D[0:19] Setup time to the rising edge of REFCLK	2.0	—	ns.	Measured from the valid data level of D[0:19] to the crossing of REFCLK
T_2	D[0:19] hold time after the rising edge of REFCLK	1.5	—	ns.	
T_R,T_F	SDO0, SDO1 rise/fall time	150	270	ps.	20% to 80%, 75 Ohm load to Vdd, Tested on a sample basis
T_{RJ}	SDO0/SDO1 output jitter	—	0.20	UI	

Figure 4: Transmit Timing Waveforms (Serializer mode)

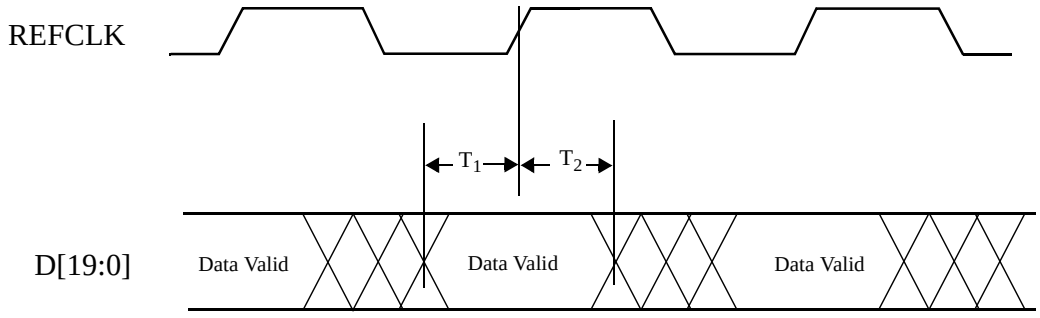

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Table 4: Transmit AC Characteristics (Serializer Mode)

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
T_1	D[0:19] Setup time to the rising edge of REFCLK	2.0	—	ns.	Measured from the valid data level of D[0:19] to the crossing of REFCLK
T_2	D[0:19] hold time after the rising edge of REFCLK	1.5	—	ns.	
T_R,T_F	SDO0, SDO1 rise/fall time	150	270	ps.	20% to 80%, 75 Ohm load to Vdd, Tested on a sample basis
T_{RJ}	SDO0/SDO1 output jitter	—	0.20	UI	

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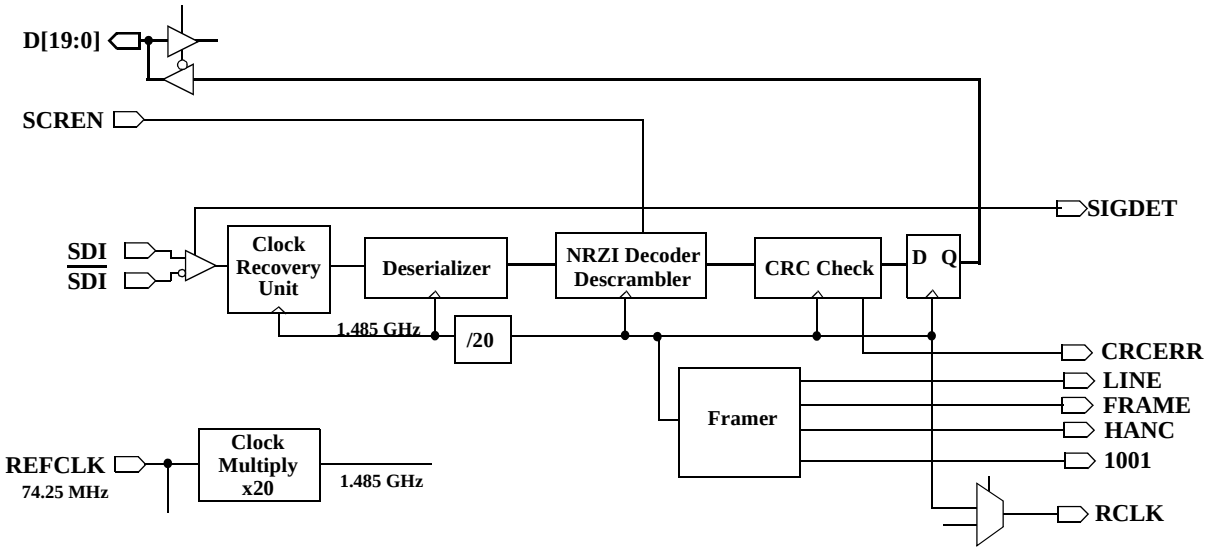
Features: Deserializer Mode

1. Compliant with SMPTE-292M @ 1.485Gb/s
2. Clock and Data Recovery
3. 1:20 Deserializer
4. Descrambler and NRZI Decoder with ENABLE
5. Data Framer aligns data to SAV/EAV
6. On-chip Clock Multiplier Unit
7. CRC Checker
8. LINE, FRAME, HANC Indication
9. 3.3V, 800 mW -- typical power
10. 20 Bit TTL Interface @ 74.25 MHz

General Description

The VSC6511 can be configured as a 20-bit HDTV Deserializer using the MODE[1:0] pins. Serial data from SDI/$\overline{\text{SDI}}$ is sent to the Clock Recovery Unit (CRU) for clock extraction and data resynchronization. Then the serial data is descrambled/NRZI decoded, deserialized and output on D[19:0] synchronously by a divided-by-twenty recovered clock, RCLK. A CRC Checker monitors the output data and indicates any CRC errors on the CRC pin. Descrambling is enabled by SCREN being HIGH. Data framing aligns the SAV/EAV patterns in the data with the data bus and RCLK and generates a once-per-line and once-per-frame synchronization output. A signal detect function on SDI/$\overline{\text{SDI}}$ monitors the quality of the serial input.

Figure 5: Deserializer Mode



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Functional Description: Deserializer Mode

The following functional blocks are used in the Deserializer mode of operation. Please refer to the Functional Description at the beginning of this document for the a description of each of these blocks.

Clock Multiplier Unit (CMU)
Serial Input
Clock Recovery Unit
Deserializer
Descrambler and NRZI Decoder
CRC Checker
Frame Aligner and SAV/EAV output

Figure 6: Receive Timing Waveforms (Deserializer Mode)

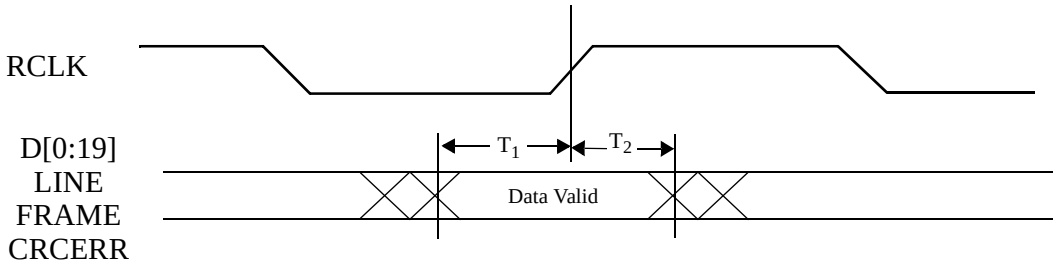

Table 5: Receive AC Characteristics (Deserializer Mode)

Parameters	*Description*	*Min.*	*Max.*	*Units*	*Conditions*
T_1	TTL Outputs alid prior to RCLK rise	3.0	—	ns.	
T_2	TTL Outputs valid after RCLK rise	2.0	—	ns.	
T_R, T_F	TTL Output rise and fall time	—	2.0	ns.	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$, into 10 pf. load.
T_{LOCK}	Data acquisition lock time @ 1.485 Gb/s	—	TBC	ms.	

Note: The RCLK output from the CRU is 40% high and 60% low by design.

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Features: Deserializer / Reclocker Mode

1. Compliant with SMPTE-292M @ 1.485Gb/s
2. Clock and Data Recovery
3. 1:20 Deserializer
4. Descrambler and NRZI Decoder with ENABLE
5. Data Framer aligns data to SAV/EAV
6. 2 or 4 User Configurable 75 ohm cable driver outputs
7. On-chip Clock Multiplier Unit
8. LINE, FRAME, HANC Indication
9. CRC Checker
10. 20 Bit TTL Interface @ 74.25 MHz
11. On-chip Clock Multiplier and Recovery Unit
12. 3.3V, 900mW -- typical power.

General Description

In the Deserializer/Reclocker Mode, both the Deserializer and the Reclocker are active. All the features of each function are available with the exception of the reclocker status/control pins on the databus D0 and D2. In this mode, D[0:19] is used solely for the deserialized recovered data. Also, RCLK is used for the deserializer's recovered clock and will not provide a buffered version of REFCLK and the BYPASS capability is also not available.

Figure 7: Block Diagram: Deserializer/Reclocker Mode

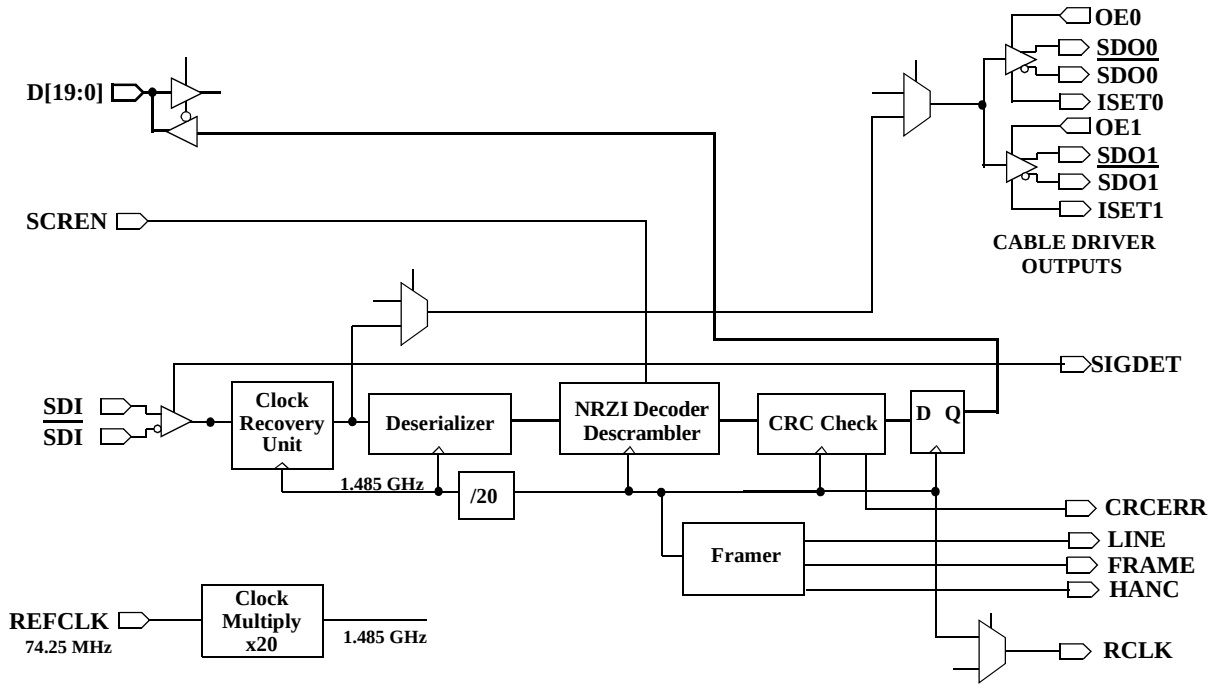

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Figure 8: REFCLK Timing Waveforms: All Modes

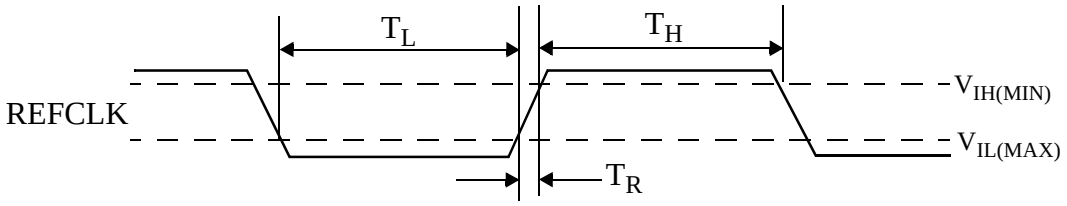

Table 6: Reference Clock Requirements *

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
FR	Frequency Range	73.75	74.50	MHz	Will accept both 74.176/74.25MHz
FO	Frequency Offset	-1000	1000	ppm.	Difference in REFCLK frequencies between the transmitting and receiving VSC6511s.
DC	REFCLK duty cycle	-15	+15	%	Measured at 1.5V
T_H, T_L	REFCLK high/low times	3.0	—	ns.	Measured between $V_{IL(MAX)}$ to $V_{IL(MAX)}$ or $V_{IH(MIN)}$ to $V_{IH(MIN)}$
T_R	REFCLK rise	—	2.0	ns.	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$

Note: The PLL locks to the rising edge of REFCLK.

Figure 9: RCLK Timing Waveforms*

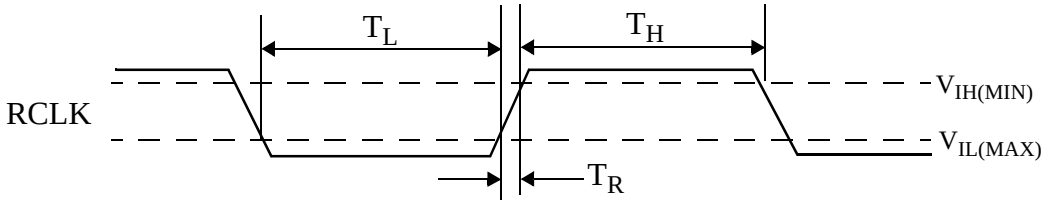

Table 7: RCLK Performance - Deserializer and Deserializer/Reclocker Mode

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
F_{OFFSET}	RCLK Frequency offset from REFCLK	-1.0	+1.0	%	Maximum deviation when the CRU is not locked. Deserializer Mode.
DC	RCLK duty cycle - 40% / 60%	-5	+5	%	Measured at 1.5V. Deserializer Mode and Deserializer/Reclocker Mode.
T_H	RCLK high times	3	—	ns.	Measured between $V_{IH(MIN)}$ to $V_{IH(MIN)}$
T_L	RCLK low times	5.9	—	ns.	Measured between $V_{IL(MAX)}$ to $V_{IL(MAX)}$
T_R	RCLK rise/fall time	—	1.5	ns.	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$

Note: The RCLK output from the CRU is 40% high and 60% low by design.

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Table 8: RCLK Performance - Serializer & Reclocker Modes

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
DC	RCLK duty cycle - 50% / 50%	-5	+5	%	Measured at 1.5V. Serializer & Reclocker Modes (REFCLK=50/50)
T_H, T_L	RCLK high/low times	3.5	—	ns.	Measured between $V_{IL(MAX)}$ to $V_{IL(MAX)}$ or $V_{IH(MIN)}$ to $V_{IH(MIN)}$
T_R	RCLK rise/fall time	—	1.5	ns.	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$

Note: The RCLK output is a buffered version of the REFCLK input. The above specifications assume a 50% duty cycle on the REFCLK input.

Absolute Maximum Ratings (1)

Power Supply Voltage (V_{DD}) .....-0.5V to +4V
PECL DC Input Voltage ..... -0.5V to V_{DD} +0.5V
TTL DC Input Voltage..... -0.5V to 5.5V
DC Voltage Applied to TTL Outputs ..... -0.5V to V_{DD} + 0.5V
TTL Output Current .....+/-50mA
PECL Output Current .....+/-50mA
Case Temperature Under Bias .....-55° to +125°C
Storage Temperature.....-65° to + 150°C
Maximum Input ESD (Human Body Model)..... 1500 V

Recommended Operating Conditions

Power Supply Voltage..... ....3.3V +/- 5%
Ambient Operating Temperature Range.....0°C Ambient to +95°C Case

Notes:

1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

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DC Characteristics *(Over recommended operating conditions).*

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{IH}	Input HIGH voltage (TTL)	2.0	—	5.5	V	
V_{IL}	Input LOW voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH current (TTL)	—	—	500	µA	V_{IN} = 2.4 V, 6.8Kohm Pull-up resistor on all inputs.
I_{IL}	Input LOW current (TTL)	—	—	-500	µA	V_{IN} = 0.5 V, 6.8Kohm Pull-up resistor on all inputs.
V_{OH}	Output HIGH Voltage (TTL)	2.4	—	—	V	I_{OH} = -1.0mA
V_{OL}	Output LOW Voltage (TTL)	—	—	0.5	V	I_{OL}= +1.0mA
V_{DD}	Supply voltage	3.14	—	3.47	V	V_{DD} = 3.3V $\pm$ 5%
P_D	Power Dissipation: (Estimated) Serializer Mode Deserializer Mode Deserializer/Reclocker Mode	 — — —	 700 800 900		mW	Outputs open, V_{DD} = V_{DD} max (These are estimates)
ΔV_{IN}	PECL input swing:	200	—	1200	mVp-p	AC Coupled. Internally biased at $V_{DD}/2$
ΔV_{OUT75}	PECL output swing:	750	—	850	mVp-p	Using appropriate matching network

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Package Pin Descriptions

Figure 10: Pin Diagram

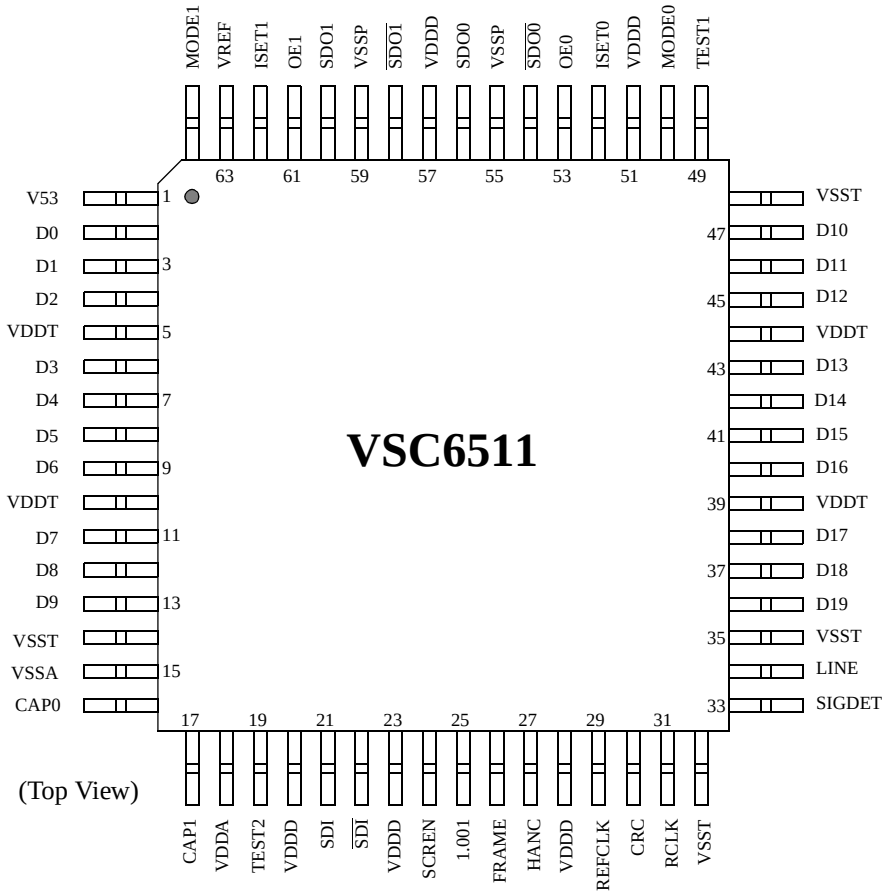

Table 9: Pin Identification

Pin #	*Name*	*Description*
2,3,4,6 7,8,9,11 12,13,47,46 45,43,42,41 40,38,37,36	D0-D3 D4-D7 D8-D11 D12-D15 D16-D19	INPUT/OUTPUT - TTL Bidirectional data bus. In Serializer mode, this is a 20-bit input bus timed to REFCLK. In Deserializer mode, this is a 20-bit output bus timed to RCLK. In Reclocker and Cable Driver mode, several of these bits are defined as status outputs.
50 64	MODE0 MODE1	INPUT - TTL: Mode select inputs. See Table #2.
24	SCREN	INPUT - TTL: When HIGH, enables scrambling in Serializer/Deserializer modes

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Pin #	*Name*	*Description*
30	CRC	BIDIRECTIONAL - TTL: In Serializer Mode, CRC Generation is enabled when this input is HIGH and disabled when LOW. In Deserializer Mode and Deserializer/Reclocker Mode, this is an output which indicates a CRC error has occurred.
26	FRAME	OUTPUT - TTL: In Deserializer and Deserializer/Reclocker modes, this is an output which, when HIGH, indicates that a FRAME synchronization event is on D[0:19].
34	LINE	OUTPUT - TTL: In Deserializer and Deserializer/Reclocker modes, this is an output which, when HIGH, indicates that a LINE synchronization event is on D[0:19].
27	HANC	OUTPUT- TTL: Output which is HIGH during the Horizontal Blanking period between EAV and SAV.
25	1.001	OUTPUT - TTL: When HIGH, indicates that a valid receive signal is present on SDI/$\overline{\text{SDI}}$ and that the SMPTE-292M incoming data is greater than 500ppm from 20xREFCLK.
21,22	SDI, $\overline{\text{SDI}}$	INPUT - Differential. Serial input to CRU.
56,54 60,58	SDO0, $\overline{\text{SDO0}}$ SDO1, $\overline{\text{SDO1}}$	OUTPUT - Differential. High Speed Cable Driver output. Serial output from the Serializer, Reclocker or SDI/$\overline{\text{SDI}}$ input buffer.
52,62	ISET0, ISET1	Connect resistor to ground to set the output swing of SDO0, and SDO1
53,61	OE0, OE1	INPUT - TTL. Output enable pins for SDO0, and SDO1. Enabled when high for each output.
29	REFCLK	INPUT - TTL. REFerence CLocK at 74.25 MHz. This is the input to the CMU and times D(19:0) in Serializer Mode.
31	RCLK	OUTPUT - TTL: Output clock. In Serializer and Reclocker Mode, this is a buffered version of REFCLK. In Deserializer Mode, this is the recovered clock used to time D(19:0).
33	SIGDET	OUTPUT - TTL. An analog signal detect output which, when HIGH, indicates that the IP/IN input contains a valid SMPTE-292M amplitude signal.
16,17	CAP0, CAP1	Analog I/O: Loop Filter Capacitor, 0.1uF nominal, 3V swing maximum
49,19	TEST1, TEST2	INPUT - TTL. LOW for factory test, HIGH for normal operation.
1	V53	INPUT - POWER: This power supply would normally be 3.3V. If 5V tolerance is required, this pin should be connected to 5V supply.
20,23,28,57,51	VDDD	Power Supply. 3.3V Supply for digital logic.
5,10,39,44	VDDT	TTL I/O Power Supply.
63	VREF	Voltage Reference Input. If used, this is biased to 1.25V.
18	VDDA	Analog Power Supply. 3.3V for Clock Multiplier PLL. Bypass to pin 15.
55,59	VSSP	Ground for High Speed Outputs
14,32,35,48	VSST	TTL I/O Ground
15	VSSA	Analog Ground Bypass to pin 18.

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Package Thermal Characteristics

The VSC6511 is packaged in an exposed pad, thin quad flat pack (TQFP) which adheres to industry standard EIAJ footprints for a 10x10x1.0mm body, 64 lead TQFP. The package construction is shown below. The bottom of the lead frame is exposed so that it can be soldered to the printed circuit board and connected to the ground plane. This provides excellent thermal characteristics and reduces electrical parasitics as well.

Figure 11: Package Cross Section

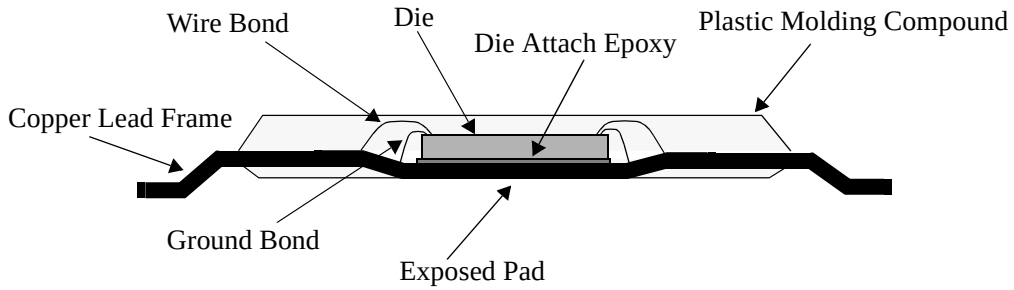

Table 10: 64-pin, Exposed Pad TQFP Thermal Resistance

Symbol	*Description*	*Value*	*Units*
θ_{ca-0}	Thermal resistance from case to ambient, still air	30	^{o}C/W
θ_{ca-100}	Thermal resistance from case to ambient, 100 LFPM air	25	^{o}C/W
θ_{ca-200}	Thermal resistance from case to ambient, 200 LFPM air	23	^{o}C/W
θ_{ca-400}	Thermal resistance from case to ambient, 400 LFPM air	21	^{o}C/W
θ_{ca-600}	Thermal resistance from case to ambient, 600 LFPM air	20	^{o}C/W

The VSC6511 is designed to operate with a case temperature up to 95^{o}C. The user must guarantee that the case temperature specification is not violated. With the thermal resistances shown above, the VS6511 can operate in still air ambient temperatures of 70^{o}C [~70^{o}C = 95^{o}C - 0.8W * 30]. If the ambient air temperature exceeds these limits then some form of cooling through a heatsink or an increase in airflow must be provided. Additional heat can be transferred to the printed circuit board by not using thermal reliefs on the power and ground plane vias as well as using multiple vias to the power and ground planes.

If the exposed pad is not soldered to the printed circuit board and grounded, both thermal and electrical performance will be degraded significantly.

Moisture Sensitivity Level

This device is rated with a Moisture Sensitivity Level 3 rating. Refer to Application Note AN-20 for appropriate handling procedures.

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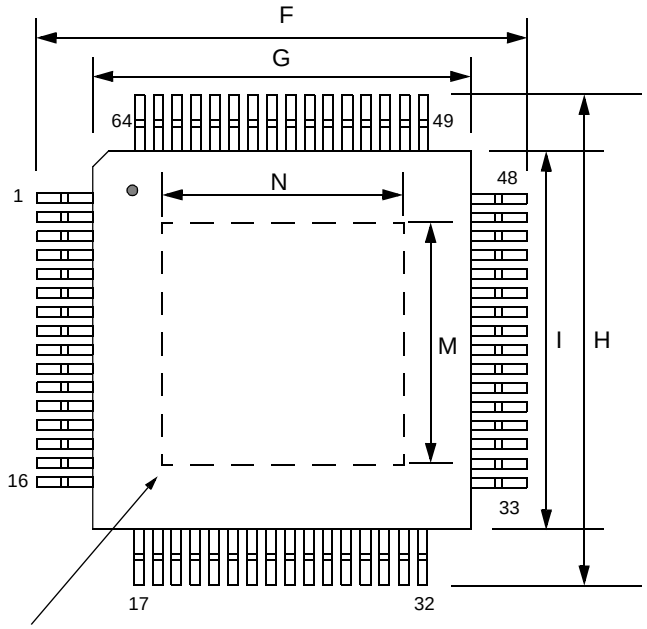
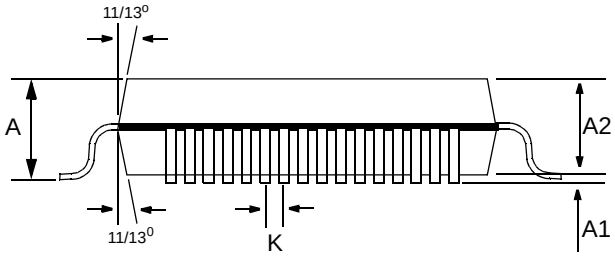
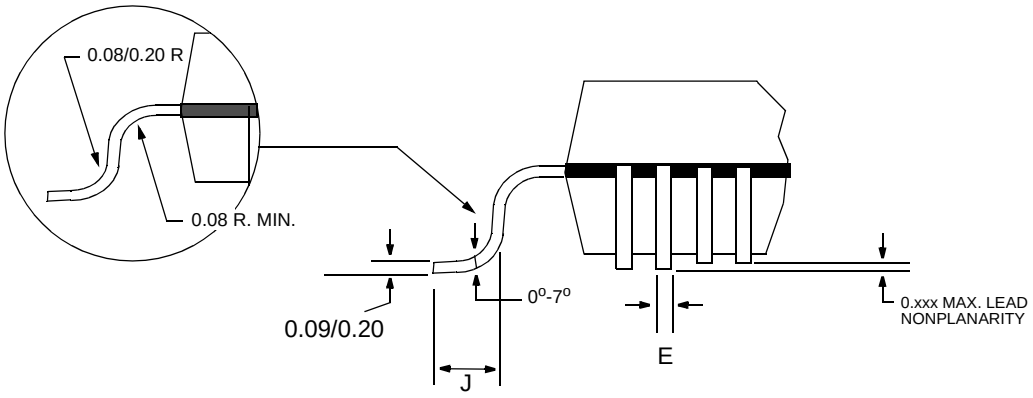
Package Information: 64-pin Exposed Pad TQFP



Item	*mm*	*Tolerance*
A	1.20	MAX
A1	0.10	±0.05
A2	1.00	±0.05
E	0.22	±0.05
F	12.00	±0.40
G	10.00	±0.10
H	12.00	±0.40
I	10.00	±0.10
J	0.60	±0.15
K	0.50	BSC
M	x.xx	±0.xx
N	x.xx	±0.xx





NOTES:
Drawing not to scale.
Exposed Pad Electrically Grounded
All dimensions in millimeters

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Ordering Information

The order number for this product is formed by a combination of the device number, and package type.

VSC6511 **RC**

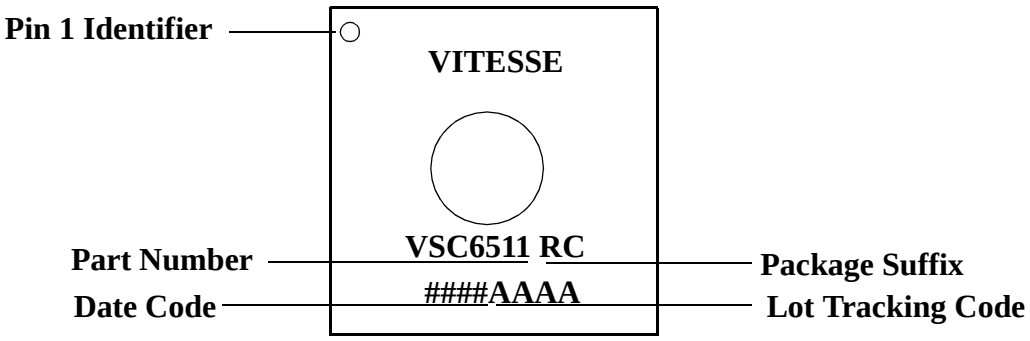
Device Type
VSC6511 - SMPTE-292M Multifunction Chip

Package Type
RC: 64-Pin, 10x10x1.0mm, Exposed Pad TQFP

Marking Information

The package is marked with three lines of text as shown below.

Figure 12: Package Marking Information



Notice

This document contains information about a product during its fabrication or early sampling phase of development. The information contained in this document is based on design targets, simulation results or early prototype test results. Characteristic data and other specifications are subject to change without notice. Therefore the reader is cautioned to confirm that this data sheet is current prior to design or order placement.

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Revision History

2.0 New Document.

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