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Data Sheet
VSC8114

ATM/SONET/SDH 622 Mb/s Transceiver Mux/Demux
with Integrated Clock Generation and Clock Recovery

Features

- Operates at STS-12/STM-4 (622.08Mb/s) Data Rate

- Compatible with Industry ATM UNI Devices

- On Chip Clock Generation of the 622.08MHz High Speed Clock (Mux)

- On Chip Clock Recovery of the 622.08MHz High Speed Clock (Demux)

- 8-Bit Parallel TTL Interface with Parity Error Detection and Generation

- SONET/SDH Frame Recovery

- Loss of Signal (LOS) Input & LOS Detection

- +3.3V/5V Programmable PECL Serial Interface

- Provides Equipment, Facilities and Split Loop-back Modes as well as Loop Timing Mode

- Provide PECL Reference Clock Inputs

- Meets Bellcore, ITU and ANSI Specifications for Jitter Performance

- Low Power - 0.9Watts Typical

- 100 PQFP Package

General Description

The VSC8114 is an ATM/SONET/SDH compatible transceiver integrating an on-chip Clock Multiplication Unit (PLL) for high speed clock generation as well as a Clock and data Recovery Unit (CRU) with 8-bit serial-to-parallel and parallel-to-serial data conversion. The PLL clock is used for serialization in the transmit direction (Mux). The recovered clock is used for deserialization in the receive direction (Demux). The demultiplexer contains SONET/SDH frame detection and recovery. In addition, the device provides both facility and equipment loopback modes and a loop time mode. The part is packaged in a 100PQFP with an integrated heat spreader for optimum thermal performance and reduced cost. The VSC8114 provides an integrated solution for ATM physical layers and SONET/SDH systems applications.

Functional Description

The VSC8114 is designed to provide a SONET/SDH compliant interface between the high speed optical networks and the lower speed User Network Interface devices such as the PM5355 S/UNI-622. The VSC8114 converts 8 bit parallel data at 77.76Mb/s to a serial bit stream at 622.08Mb/s. The device also provides a Facility Loopback function which loops the received high speed data and clock (optionally recovered on-chip) directly to the high speed transmit outputs. A Clock Multiplier Unit (CMU) is integrated into the transmit circuit to generate the high speed clock for the serial output data stream from input reference frequencies of 19.44 or 77.76 MHz. The CMU can be bypassed with the received/recovered clock in loop timing mode, thus synchronizing the entire part to a single clock. The block diagram on page 2 shows the major functional blocks associated with the VSC8114.

The receive section provides the serial-to-parallel conversion, converting 622Mb/s bit stream to an 8 bit parallel output at 77.76MHz. A Clock Recovery Unit (CRU) is integrated into the receive circuit to recover the high speed clock from the received serial data stream. The receive section provides an Equipment Loopback function which will loop the low speed transmit data and clock back through the receive section to the 8 bit parallel outputs. The VSC8114 also provides the option of selecting between either its internal CRU's clock and data signals, or optics containing a CRU clock and data signals. The receive section also contains a SONET/SDH frame

detector circuit which is used to provide frame pluses during the A1, A2 boundary in the serial to parallel converter. This only occurs when OOF is high. Both internal and external LOS functions are supported.

The VSC8114 provides the parity error detection and generation for the 8 bit data bus. On the receive side, the parity of the 8 bit data outputs is generated. On the transmit side, the parity of the 8 bit data input is calculated and compared with the received parity input.

VSC8114 Block Diagram
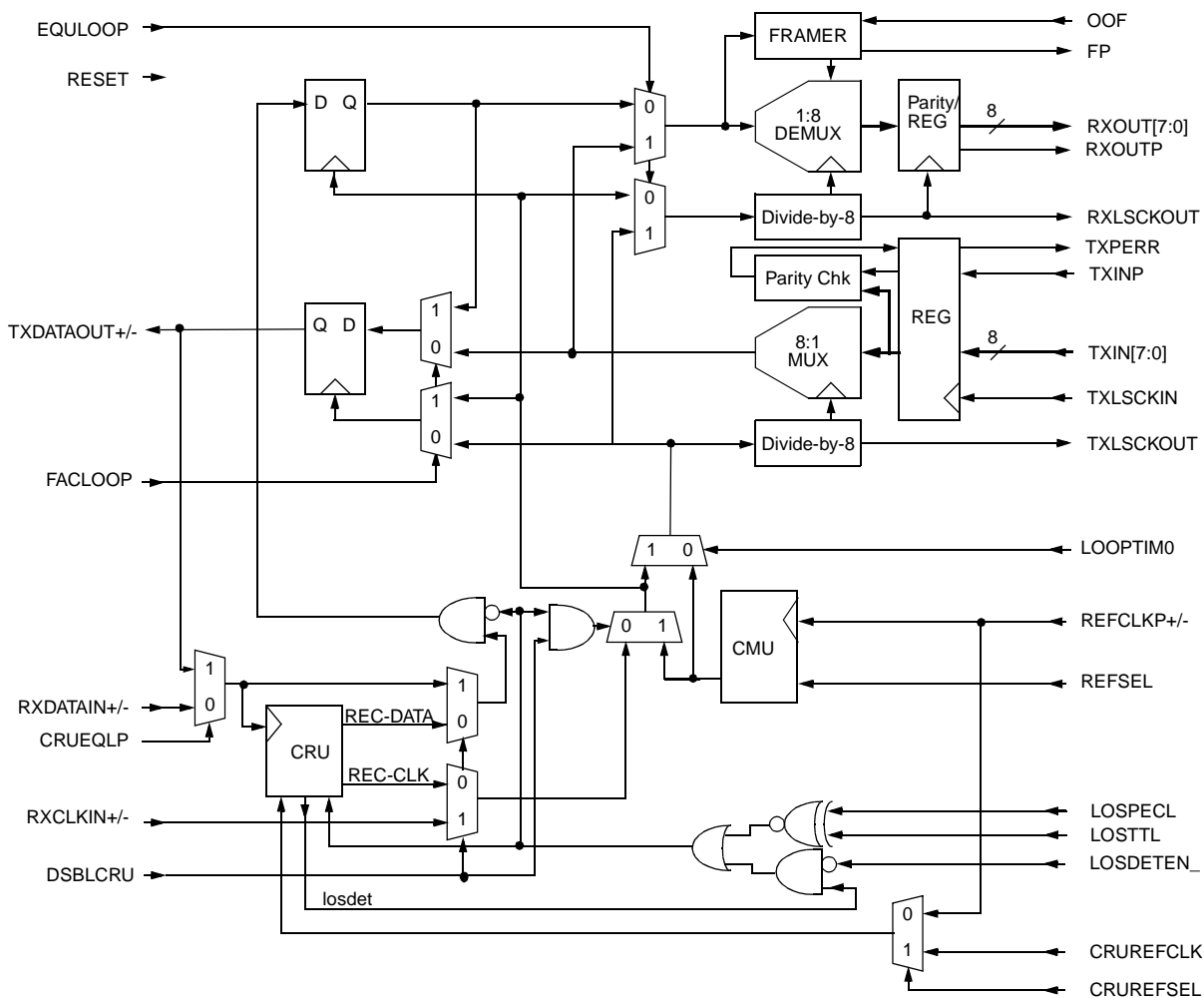

Transmit Section

Byte-wide data is presented to TXIN[7:0] and is clocked into the part on the rising edge of TXLSCKIN. See Figure 1. The data is then serialized (MSB leading) and presented to the TXDATAOUT+/- pins. The serial output stream is synchronized to the CMU generated clock which is a phase locked and frequency scaled ver-

sion of the input reference clock. External control input REFSEL selects the multiply ratio of the CMU (see table 11). A divide-by-8 version of the CMU clock (TXLSCKOUT) should be used to synchronize the transmit interface of the UNI device to the transmit input registers on the VSC8114 (see Application Notes, p. 20).

Figure 1: Data and Clock Transmit Block Diagram
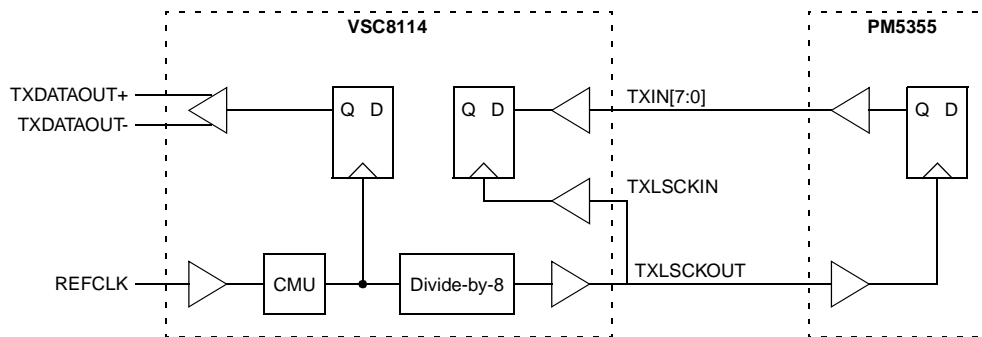
Receive Section

High speed Non-Return to Zero (NRZ) serial data at 622Mb/s are received by the RXDATAIN inputs. The CRU recovers the high speed clock from the serial data input. The serial data is converted to byte-wide parallel data and presented on RXOUT[7:0] pins. A divide-by-8 version of the high-speed clock (RXLSCKOUT) should be used to synchronize the byte-serial RXOUT[7:0] data with the receive portion of the UNI device. The on-chip CRU is by-passed by setting the DSBLCRU input high. In this mode, the serial input data and corresponding clock are received by the RXDATAIN and RXCLKIN inputs respectively. RXDATAIN is clocked in on the rising edge of RXCLKIN+. See Figure 2.

The receive section also includes frame detection and recovery circuitry which detects the SONET/SDH frame, aligns the received serial data on byte boundaries, and initiates a frame pulse on FP coincident with the byte aligned data. The frame recovery is initiated when OOF is held high which must occur at least 4 byte clock cycles before the A1A2 boundary. The OOF input control is a level-sensitive signal, and the VSC8114 will continually perform frame detection and recovery as long as this pin is held high even if 1 or more frames has been detected. Frame detection and recovery occurs when a series of three A1 bytes followed by three A2 bytes has been detected. The parallel output data on RXOUT[7:0] will be byte aligned starting on the third A2 byte. When a frame is detected, a single byte clock period long pulse is generated on FP which is synchronized with the byte-aligned third A2 byte on RXOUT[7:0]. The frame detector sends an FP pulse only if OOF is high.

Loss of Signal

The VSC8114 features Loss of Signal (LOS) detection. Loss of Signal is detected if the incoming serial data stream has no transition continuously for more than 128 bits. During an LOS condition, the VSC8114 forces the receive data low which is an indication for any downstream equipment that an optical interface failure has occurred. The receive section continues to be clocked by the CRU as it is now locked to the CRUREFCLK unless DSBLCRU is active, in which case it will be clocked by the CMU. This LOS condition will be removed when the part detects more than 16 transitions in a 128 bit time window. This LOS detection feature can be disabled by applying a high level to the LOSDETEN_ input. The VSC8114 also has a TTL input LOSTTL and a

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SEMICONDUCTOR CORPORATION

ATM/SONET/SDH 622 Mb/s Transceiver Mux/Demux
with Integrated Clock Generation and Clock Recovery

Data Sheet
VSC8114

PECL input LOSPECL to force the part into a Loss of Signal state. Most optics have a PECL output usually called "SD" or "FLAG" indicating the presence or lack of optical power. Depending on the optics manufacturer this signal is either active high or active low. The LOSTTL and LOSPECL inputs are XNOR'd to generate an internal LOS control signal. See Figure 2. The optics "SD" output should be connected to LOSPECL. The LOSTTL input should be tied to low if the optics "SD" is active high. If it's active low tie LOSTTL to a high. The inverse is true if the optics use "FLAG" for loss of signal

Figure 2: Data and Clock Receive Block Diagram
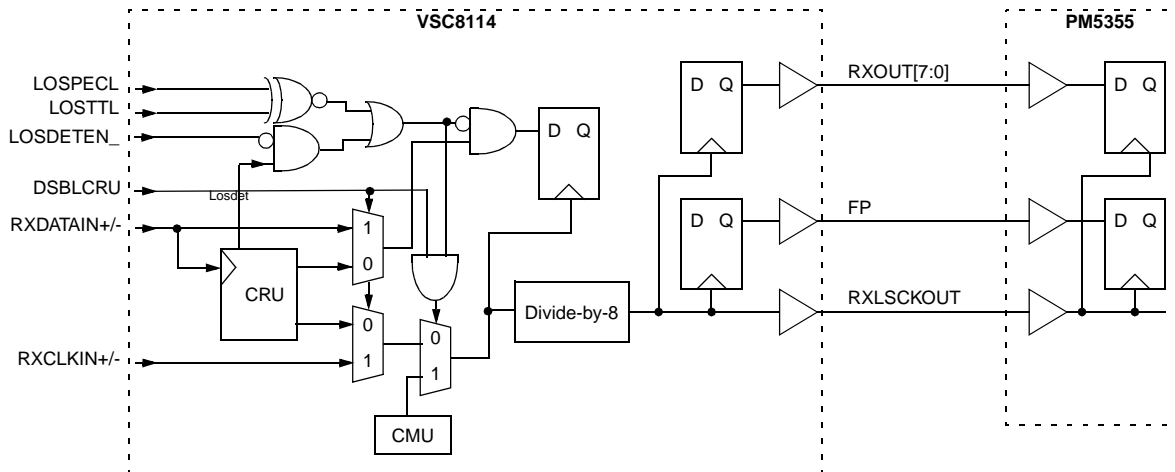
Facility Loopback

The Facility Loopback function is controlled by the FACLOOP signal. When the FACLOOP signal is set high, the Facility Loopback mode is activated and the high speed serial receive data (RXDATAIN) is presented to the high speed transmit output (TXDATAOUT). See Figure 3. In Facility Loopback mode the high speed receive data (RXDATAIN) is also converted to parallel data and presented to the low speed receive data output pins (RXOUT[7:0]). The receive clock (RXCLKIN) is also divided down and presented to the low speed clock output (RXLSCKOUT).

**Figure 3: Facility Loopback Data Path**
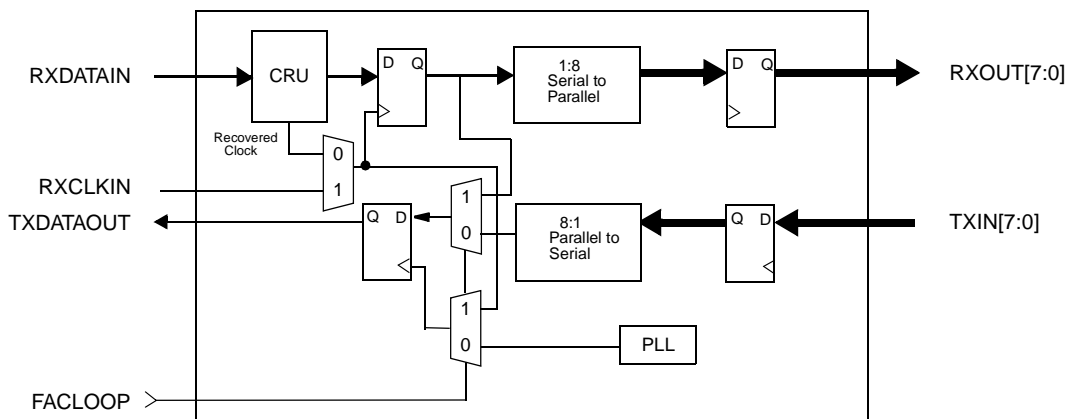
Equipment Loopback

The Equipment Loopback function is controlled by the EQULOOP signal. When the EQULOOP signal is set high, the Equipment Loopback mode is activated and the high speed transmit data generated from the parallel to serial conversion of the low speed data (TXIN[7:0]) is selected and converted back to parallel data in the receiver section and presented to the low speed parallel outputs (RXOUT[7:0]). See Figure 4. The internally generated 622MHz clock is used to generate the low speed receive clock output (RXLSCKOUT). In Equipment Loopback mode the transmit data (TXIN[7:0]) is serialized and presented to the high speed output (TXDATAOUT) using the clock generated by the on-chip clock multiplier unit.

CRU Equipment Loopback

Exactly the same as equipment loopback, the point where the transmit data is looped back is moved all the way back to the high speed I/O. When the CRUEQLP signal is set high, transmit data is looped back to the CRU, replacing RXDATAIN±

Figure 4: Equipment Loopback Data Path
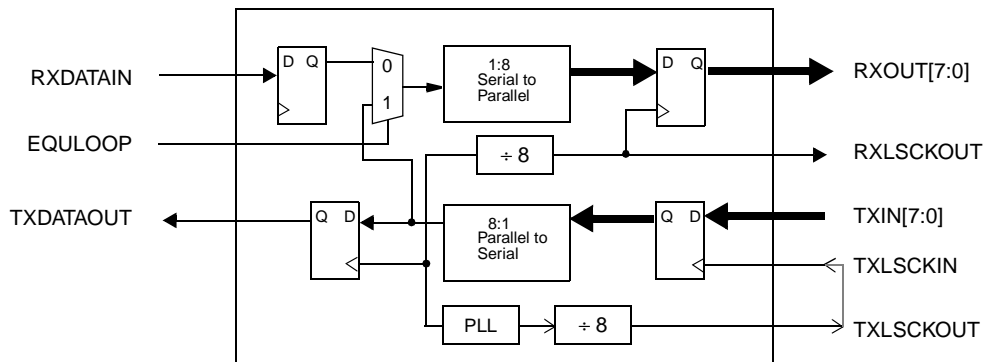
Split Loopback

Equipment and facility loopback modes can be enabled simultaneously. In this case, high-speed serial data received (RXDATAIN) is mux'd through to the high-speed serial outputs (TXDATAOUT). The low-speed transmit byte-wide bus (TXIN[7:0]) and (TXLSCKIN) is mux'd into the low-speed byte-wide receive output bus (RXOUT[7:0]) and (RXLSCKOUT). See Figure 5.

Figure 5: Split Loopback Datapath
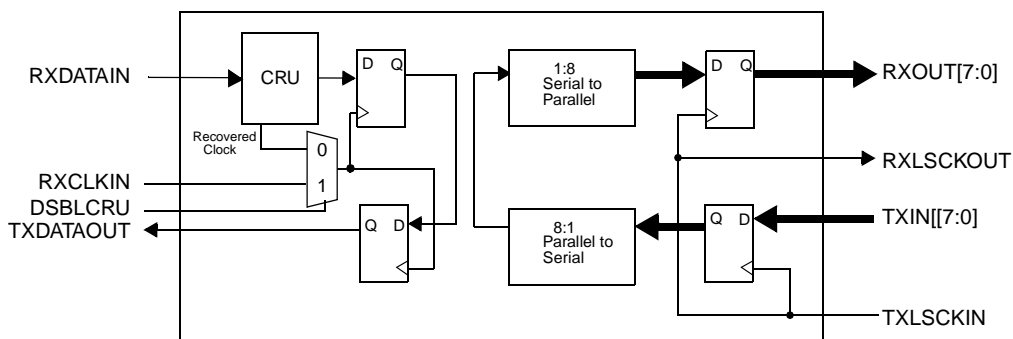
Loop Timing

LOOPTIM0 mode bypasses the CMU when the LOOPTIM0 input is asserted high. In this mode the CMU is bypassed by using the receive clock (RXCLKIN), and the entire part is synchronously clocked from a single external source.

Parity

An even parity input (TXINP) is provided for the byte-wide transmit data. This input, along with byte-wide data, is clocked into the VSC8114 on the rising edge of TXLSCKIN. Parity is calculated on the clocked in byte-wide data and compared to the clocked in parity input. A parity error is reported on the next TXLSCKIN rising edge on TXPERR. For no parity errors to result, TXINP must be logic 1 when on an odd number of bits in the TXIN[7:0] are logic 1; otherwise, it must be logic 0.

Even parity is calculated and clocked out along with byte-wide receive data (RXOUT[7:0]) on RXOUTP. RXOUTP is a logic 1 when an odd number of bits on RXOUT[7:0] are logic 1; ohterwise, it is logic 0.

Clock Synthesis

The VSC8114 uses an integrated phase-locked loop (PLL) for clock synthesis of the 622MHz high speed clock used for serialization in the transmitter section. The PLL is comprised of a phase-frequency detector (PFD), an integrating operation amplifier and a voltage controlled oscillator (VCO) configured in classic feedback system. The PFD compares the selected divided down version of the 622MHz VCO (select pin REFSEL selects divide-by ratios of 8 and 32, see Table 11) and the reference clock. The integrator provides a transfer function between input phase error and output voltage control. The VCO portion of the PLL is a voltage controlled ring-oscillator with a center frequency of 622MHz.

The reactive elements of the integrator are located off-chip and are connected to the feedback loop of the amplifier through the CP1, CP2, CN1 and CN2 pins. The configuration of these external surface mounted capacitors is shown in Figure 6. Table 1 shows the recommended external capacitor values for the configurable reference frequencies.

Good analog design practices should be applied to the board design for these external components. Tightly controlled analog ground and power planes should be provided for the PLL portion of the circuitry. The dedicated PLL power (VDDANA) and ground (VSSANA) pins should have quiet supply planes to minimize jitter generation within the clock synthesis unit. This is accomplished by either using a ferrite bead or a C-L-C choke (π filter) on the (VDDANA) power pins. Note: Vitesse recommends a (π filter) C-L-C choke over using a ferrite bead. All ground planes should be tied together using multiple vias.

Reference Clocks

Note that the CMU uses a differential PECL reference clock input to achieve optimum jitter performance.

The CRU has the option of either using the CMU's reference clock or its own independent reference clock CRUREFCLK. This is accomplished with the control signal CRUREFSEL. The CRUREFCLK should be used if the system is being operated in either a regeneration or loop timing mode. In either of these modes the quality of the CRUREFCLK is not a concern, thus it can be driven by a simple 77.76MHz crystal, the key is its independence from the CMU's reference clock.
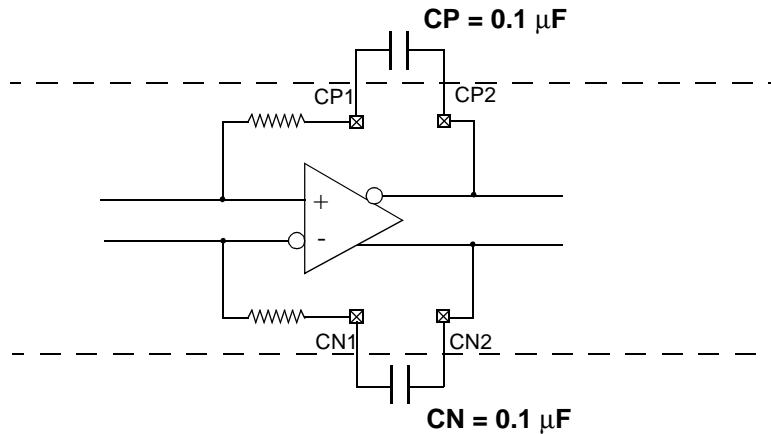
Figure 6: External Integrator Capacitor

CP = 0.1 μF

CP1   CP2

+

-

CN1   CN2

CN = 0.1 μF

Table 1: Recommended External Capacitor Values

Reference Frequency [MHz]	Divide Ratio	CP	CN	Type	Size	Tol.
19.44	32	0.1	0.1	X7R	0603/0803	+/-10%
77.76	8	0.1	0.1	X7R	0603/0803	+/-10%

Clock Recovery

The fully monolithic Clock Recovery Unit (CRU) consists of a Phase Detector, a Frequency Detector, a Loop Filter and a Voltage Controlled Oscillator (VCO). The phase detector compares the phase information of the incoming data with the recovered clock. The frequency detector compares the frequency component of the data input with the recovered clock to provide the pull in energy during lock acquisition. The Loop Filter integrates the phase information from the phase and frequency detectors and provides the control voltage to the VCO.

Jitter Tolerance

Jitter Tolerance is the ability of the Clock Recovery Unit to track timing variations in the received data stream. The Bellcore and ITU specifications allow the received optical data to contain jitter. The amount that must be tolerated is a function of the frequency of the jitter. The CRU is designed to tolerate jitter with margin over the specification limits, see Figure 7. The CRU obtains and maintains lock based on the data transition information. When there is no transition on the data stream, the recovered clock frequency can drift. The VSC8114 can maintain lock over 100 bits of no switching on the data stream.

Figure 7: Jitter Tolerance
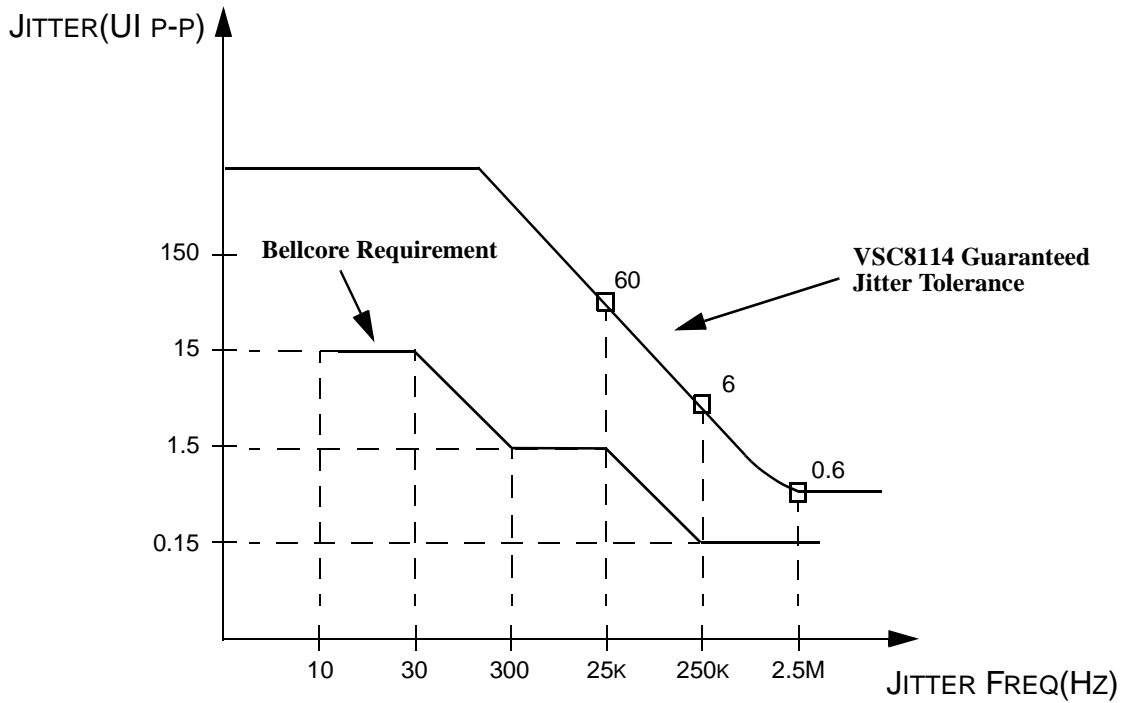
Data Latency

The VSC8114 contains several operating modes, each of which exercise different logic paths through the part. Table 2 bounds the data latency through each path with an associated clock signal.

Table 2: Data Latency

Circuit Mode	Description	Clock Reference	Range of Clock cycles
Receive	MSB at RXDATAIN to data on RXOUT [7:0]	RXCLKIN	25-35
Facilities Loopback	MSB at RXDATAIN to MSB at TXDATAOUT	RXCLKIN	2-4

AC Timing Characteristics

Figure 8: Receive High Speed Data Input Timing Diagram
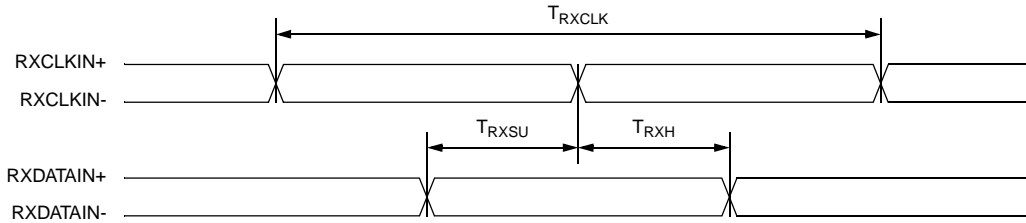
Table 3: Receive High Speed Data Input Timing Table

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{RXCLK}	Receive clock period	-	1.608	-	ns
T_{RXSU}	Serial data setup time with respect to RXCLKIN	250	-	-	ps
T_{RXH}	Serial data hold time with respect to RXCLKIN	250	-	-	ps

Figure 9: Receive Data Output Timing Diagram
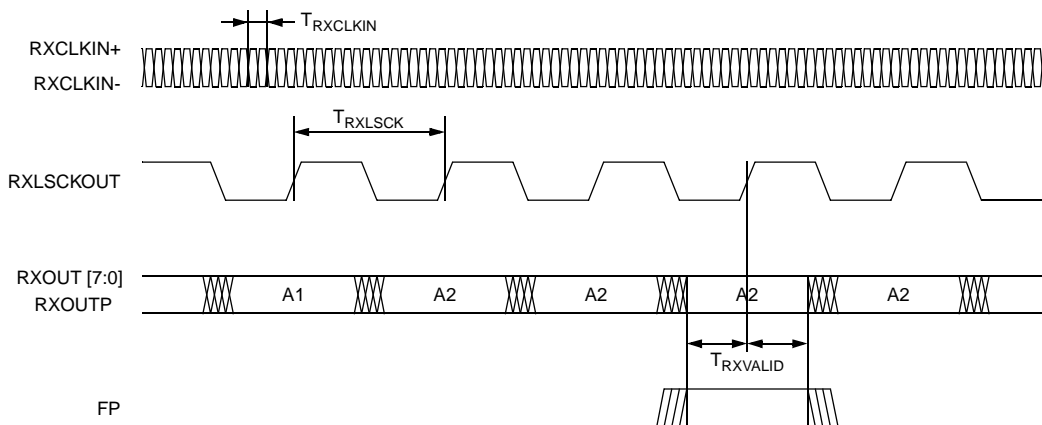
Table 4: Receive Data Output Timing Table

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{RXCLKIN}$	Receive clock period	-	1.608	-	ns
T_{RXLSCK}	Receive data output byte clock period	-	12.86	-	ns
$T_{RXVALID}$	Time data on RXOUT [7:0], FP, and RXOUTP is valid before and after the rising edge of RXLSCKOUT	4.0	-	-	ns
T_{PW}	Pulse width of frame detection pulse FP	-	12.86	-	ns

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Data Sheet

ATM/SONET/SDH 622 Mb/s Transceiver Mux/Demux
with Integrated Clock Generation and Clock Recovery
VSC8114

Figure 10: Transmit High Speed Data Timing Diagram
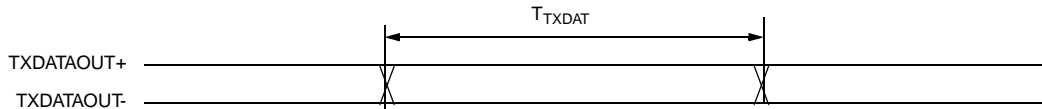
Table 5: Transmit High Speed Data Timing Table

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{TXDAT}	Transmit data width	-	1.608	-	ns

Figure 11: Transmit Data Timing Diagram
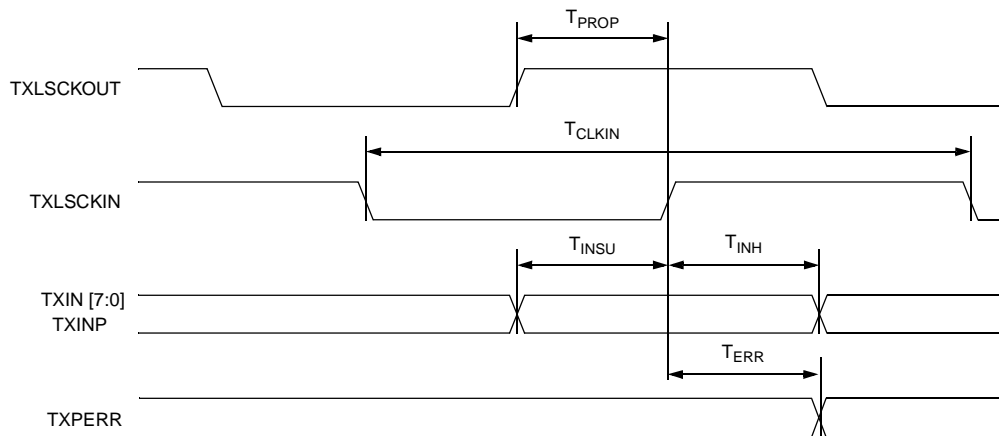
Table 6: Transmit Data Input Timing Table

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{CLKIN}	Transmit data input byte clock period	-	12.86	-	ns
T_{INSU}	Transmit data and parity setup time with respect to TXLSCKIN	1.0	-	-	ns
T_{INH}	Transmit data and parity hold time with respect to TXLSCKIN	1.0	-	-	ns
T_{PROP}	Maximum allowable propagation delay for connecting TXLSCKOUT to TXLSCKIN	-	-	3.5	ns
T_{ERR}	Propagation delay from TXLSCKIN to TXPERR	3.2	-	9.0	ns

Note: Duty cycle for TXLSCKOUT is 50% +/- 10% worst case

AC Characteristics

Table 7: PECL and TTL Outputs

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
$T_{R,TTL}$	TTL Output Rise Time	—	2	—	ns	10-90%
$T_{F,TTL}$	TTL Output Fall Time	—	1.5	—	ns	10-90%
$T_{R,PECL}$	PECL Output Rise Time	—	350	—	ps	20-80%
$T_{F,PECL}$	PECL Output Fall Time	—	350	—	ps	20-80%

DC Characteristics

Table 8: PECL and TTL Inputs and Outputs

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage (PECL)	—	—	$V_{DDP} - 0.9V$	V	—
V_{OL}	Output LOW voltage (PECL)	0.7	—	—	V	—
V_{OCM}	O/P Common Mode Range (PECL)	1.1	—	$V_{DDP} - 1.3V$	V	—
ΔV_{OUT75}	Differential Output Voltage (PECL)	600	—	1300	mV	75Ω to $V_{DDP} - 2.0V$
ΔV_{OUT50}	Differential Output Voltage (PECL)	600	—	1300	mV	50Ω to $V_{DDP} - 2.0V$
V_{IH}	Input HIGH voltage (PECL)	$V_{DDP} - 0.9V$	—	$V_{DDP} - 0.3V$	V	For single ended
V_{IL}	Input LOW voltage (PECL)	0	—	$V_{DDP} - 1.72V$	V	For single ended
ΔV_{IN}	Differential Input Voltage (PECL)	400	—	1600	mV	—
V_{ICM}	I/P Common Mode Range (PECL)	$1.5 - \Delta V_{IN}/2$	—	$V_{DDP} - 1.0 - \Delta V_{IN}/2$	V	—
V_{OH}	Output HIGH voltage (TTL)	2.4	—	—	V	$I_{OH} = -1.0$ mA
V_{OL}	Output LOW voltage (TTL)	—	—	0.5	V	$I_{OL} = +1.0$ mA
V_{IH}	Input HIGH voltage (TTL)	2.0	—	5.5	V	—

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IL}	Input LOW voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH current (TTL)	—	50	500	μA	$2.0V < V_{IN} < 5.5V$, Typical @ 2.4V
I_{IL}	Input LOW current (TTL)	—	—	-500	μA	$-0.5V < V_{IN} < 0.8V$

Power Dissipation

Table 9: Power Supply Currents

Parameter	Description	Max	Units
I_{DD}	Power supply current from V_{DD}	410	mA
I_{DDP}	Power supply current from PECL I/O Supply V_{DDP} (output unloaded)	30	mA
P_D	Power dissipation (Worst Case) $(I_{DD} + I_{DDP})$ x 3.45V = 1.51	1.51	W

Absolute Maximum Ratings[1]

Power Supply Voltage (V_{DD}) Potential to GND ....-0.5V to +4V

PECL I/O Supply Voltage (V_{DDP}) Potential to GND..-0.5V to +6V

DC Input Voltage (PECL inputs).. -0.5V to V_{DDP} +0.5V

DC Input Voltage (TTL inputs) ....-0.5V to 5.5V

DC Output Voltage (TTL Outputs).. -0.5V to V_{DD} + 0.5V

Output Current (TTL Outputs) .... +/-50mA

Output Current (PECL Outputs)..+/-50mA

Case Temperature Under Bias ....-55° to +125°C

Storage Temperature... -65°C to +150°C

Maximum Input ESD (Human Body Model) .... 1500 V

Note: Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltage (V_{DD}) ....+3.3V ±5 %

PECL I/O Supply Voltage (V_{DDP}).. +3.3V or +5.0V ±5 %

Commercial Operating Temperature Range .... 0° ambient to 70°C case

Extended Operating Temperature Range ....0° ambient to 115°C case

Industrial Operating Temperature Range .... -40° ambient to 85°C case

Clock Recovery Unit

Table 10: Reference Frequency for the CRU

CRUREFSEL	*REFSEL*	*CRUREFCLK Frequency [MHz]*	*Output Frequency [MHz]*
1	X	77.76 ± 500ppm	622.08
0	Uses CMU's Reference Clock (See Table 11 below)		

Clock Multiplier Unit

Table 11: Reference Frequency Selection and Output Frequency Control

REFSEL	*Reference Frequency [MHz]*	*Output Frequency [MHz]*
1	19.44	622.08
0	77.76	622.08

Table 12: Clock Multiplier Unit Performance

Name	*Description*	*Min*	*Typ*	*Max*	*Units*
RCd	Reference clock duty cycle	40		60	%
RCj	Reference clock jitter (RMS) @ 77.76 MHz ref [1]			13	ps
RCj	Reference clock jitter (RMS) @ 19.44 MHz ref [1]			5	ps
RC_f	Reference clock frequency tolerance [2]	-20		+20	ppm
OCj	TXDATAOUT+/- jitter (RMS) @ 77.76 MHz ref [3]			8	ps
OCj	TXDATAOUT+/- jitter (RMS) @ 19.44 MHz ref [3]			15	ps
OCf_{range}	Output frequency (alternating 10 pattern)	620		624	Mb/s

(1)   These Reference Clock Jitter limits are required for the outputs to meet SONET system level jitter requirements
*   (< 10 mUIrms)*
(2)   Needed to meet SONET output frequency stability requirements
(3)   Measured

Note: Jitter specification is defined utilizing a 12KHz - 5MHz LP-HP single pole filter.

Package Pin Description

Table 13: Pin Definitions

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
FACLOOP	1	I	TTL	Facility loopback, loops high-speed data
VDD	2		+3.3V	+3.3V Power Supply
CRUEQLP	3	I	TTL	CRU equipment loopback, loops TXDATAOUT to the CRU replacing RXDATAIN+/-
RESET	4	I	TTL	Resets frame detection, dividers, controls; active high
LOOPTIM0	5	I	TTL	Enable loop timing operation; active high
N/C	6			No connection
REFSEL	7	I	TTL	Reference clock select, refer to table 11
N/C	8			No connection
VDDP	9		+3.3/+5V	+3.3V or +5V Power Supply for PECL I/Os
TXDATAOUT+	10	O	PECL	Transmit output, high speed differential data +
TXDATAOUT-	11	O	PECL	Transmit output, high speed differential data -
VSS	12		GND	Ground
N/C	13			No connection
N/C	14			No connection
VDDP	15		+3.3/+5V	+3.3V or +5V Power Supply for PECL I/Os
N/C	16			No connection
LOSDETEN_	17	I	TTL	Enables internal LOS detection (active low).
VSS	18		GND	Ground
RXCLKIN+	19	I	PECL	Receive high speed differential clock input+
RXCLKIN-	20	I	PECL	Receive high speed differential clock input-
VDDP	21		+3.3/+5V	+3.3V or +5V Power Supply for PECL I/Os
OOF	22	I	TTL	Out Of Frame; Frame detection initiated with high level
DSBLCRU	23	I	TTL	Disable on-chip clock recovery unit; active high
RXDATAIN+	24	I	PECL	Receive high speed differential data input+
RXDATAIN-	25	I	PECL	Receive high speed differential data input-
NC	26			No connection
NC	27			No connection
VDD	28		+3.3V	+3.3V Power Supply
REFCLKP+	29	I	PECL	PECL reference clock input+
REFCLKP-	30	I	PECL	PECL reference clock input-
VDD	31		+3.3V	+3.3V Power Supply

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Data Sheet
VSC8114

ATM/SONET/SDH 622 Mb/s Transceiver Mux/Demux
with Integrated Clock Generation and Clock Recovery

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
N/C	32			No connection
RXOUTP	33	O	TTL	Receive output data even parity
VSS	34		GND	Ground
RXOUT0	35	O	TTL	Receive output data bit0
RXOUT1	36	O	TTL	Receive output data bit1
VSS	37		GND	Ground
RXOUT2	38	O	TTL	Receive output data bit2
RXOUT3	39	O	TTL	Receive output data bit3
VSS	40		GND	Ground
RXOUT4	41	O	TTL	Receive output data bit4
RXOUT5	42	O	TTL	Receive output data bit5
VSS	43		GND	Ground
RXOUT6	44	O	TTL	Receive output data bit6
RXOUT7	45	O	TTL	Receive output data bit7
VSS	46		GND	Ground
RXLSCKOUT	47	O	TTL	Receive byte clock output
FP	48	O	TTL	Frame detection pulse
VDD	49		+3.3V	+3.3V Power Supply
TXPERR	50	O	TTL	Transmit input data parity error
CRUREFCLK	51	I	TTL	Optional external CRU reference clock @ 77.76MHz
LOSTTL	52	I	TTL	Loss of Signal Control - TTL input
LOSPECL	53	I	PECL	Loss of Signal Control- Single ended PECL input
VDD	54		+3.3V	+3.3V Power Supply
VSS	55		GND	Ground
N/C	56			No connection
N/C	57			No connection
VDD	58		+3.3V	+3.3V Power Supply
VSSA	59		GND	Analog Ground (CMU)
VSSA	60		GND	Analog Ground (CMU)
N/C	61			No connection
VDDA	62		+3.3V	Analog Power Supply (CMU)
CP1	63		Analog	CMU external capacitor (see Figure 6, and Table 1)
CN1	64		Analog	CMU external capacitor (see Figure 6, and Table 1)
CN2	65		Analog	CMU external capacitor (see Figure 6, and Table 1)

ATM/SONET/SDH 622 Mb/s Transceiver Mux/Demux
with Integrated Clock Generation and Clock Recovery — *VSC8114*

Signal	*Pin*	*I/O*	*Level*	*Pin Description*
CP2	66		Analog	CMU external capacitor (see Figure 6, and Table 1)
VDDA	67		+3.3V	Analog Power Supply (CMU)
VDDA	68		+3.3V	Analog Power Supply (CRU)
VDDA	69		+3.3V	Analog Power Supply (CRU)
VSSA	70		GND	Analog Ground (CRU)
VSSA	71		GND	Analog Ground (CRU)
VSS	72		GND	Ground
N/C	73			No connection
N/C	74			No connection
VSS	75		GND	Ground
VDD	76		+3.3V	+3.3V Power Supply
N/C	77			No connection
N/C	78			No connection
N/C	79			No connection
N/C	80			No connection
VDD	81		+3.3V	+3.3V Power Supply
TXLSCKOUT	82	O	TTL	Transmit byte clock out
TXLSCKIN	83	I	TTL	Transmit byte clock in
VSS	84		GND	Ground
TXIN7	85	I	TTL	Transmit input data bit7
TXIN6	86	I	TTL	Transmit input data bit6
VSS	87		GND	Ground
TXIN5	88	I	TTL	Transmit input data bit5
TXIN4	89	I	TTL	Transmit input data bit4
N/C	90			No connection
TXIN3	91	I	TTL	Transmit input data bit3
TXIN2	92	I	TTL	Transmit input data bit2
VSS	93		GND	Ground
TXIN1	94	I	TTL	Transmit input data bit1
TXIN0	95	I	TTL	Transmit input data bit0
N/C	96			No connection
TXINP	97	I	TTL	Transmit input data even parity
CRUREFSEL	98	I	TTL	Selects between CMU's or CRU's reference clock
VDD	99		+3.3V	+3.3V Power Supply
EQULOOP	100	I	TTL	Equipment loopback, loops low-speed byte-wide data

Package Information

100 PQFP Package Drawings

TOP VIEW
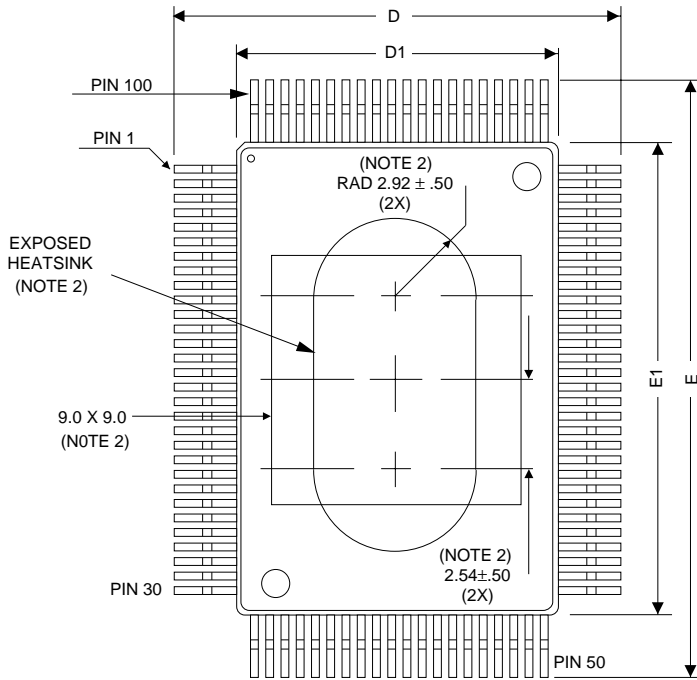
Key	mm	Tolerance
A	3.40	MAX
A1	0.25	MIN.
A2	2.7	±.10
D	17.20	±.20
D1	14.00	±.10
E	23.20	±.20
E1	20.00	±.10
L	0.80	±.2
e	0.65	NOM
b	0.30	±.10
θ	0°-7°	
R	.30	+0/-.1
R1	.2	NOM
θ2	15°	
θ3	15°	

PIN 100, PIN 1, PIN 30, PIN 50

EXPOSED HEATSINK (NOTE 2)

(NOTE 2) RAD 2.92 ± .50 (2X)

9.0 X 9.0 (NOTE 2)

(NOTE 2) 2.54±.50 (2X)
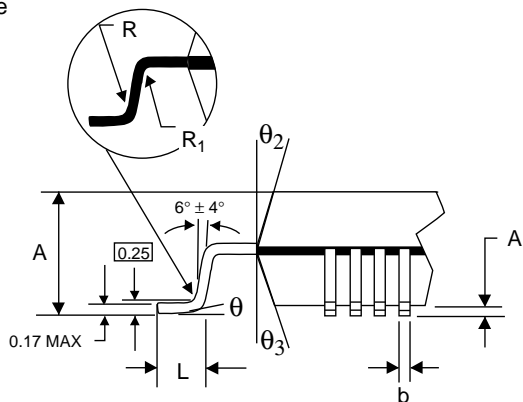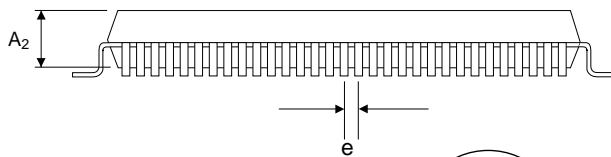
NOTES:
(1) Drawings not to scale.
(2) Two styles of exposed heat spreaders may be used; square or oval.
(3) All units in millimeters unless otherwise noted

6° ± 4°, 0.25, A, 0.17 MAX, L, b, A1

Package #: 101-202-4
Issue #: 1

The VSC8114 is manufactured in a 100PQFP package which is supplied by two different vendors. The critical dimensions in the drawing represent the superset of dimensions for both packages. The significant difference between the two packages is in the shape and size of the heatspreader which needs to be considered when attaching a heatsink.

Package Thermal Characteristics

The VSC8114 is packaged in a thermally enhanced 100PQFP with an embedded heat sink. The heat sink surface configurations are shown in the package drawings. With natural convection, the case to air thermal resistance is estimated to be 27.5^{o}C/W. The air flow versus thermal resistance relationship is shown in Table 14.

Junction to case thermal resistance is 1.2 ^{o}C/W

Table 14: Theta Case to Ambient versus Air Velocity

Air Velocity (LFPM)	Case to air thermal resistance ^{o}C/W
0	27.5
100	23.1
200	19.8
400	17.6
600	16

Ordering Information

The order number for this product are:

Part Number	Device Type
VSC8114QB:	622Mb/s Mux/Dmux with CMU and CRU in 100 Pin PQFP
	Commercial Temperature, 0°C ambient to 70°C case
VSC8114QB1	622Mb/s Mux/Dmux with CMU and CRU in 100 Pin PQFP
	Extended Temperature, 0°C to 85°C ambient (equivalent to 0°C ambient to 115°C case)
VSC8114QB2	622Mb/s Mux/Dmux with CMU and CRU in 100 Pin PQFP
	Industrial Temperature, -40°C ambient to 85°C case

Notice

This document contains preliminary information about a new product in the preproduction phase of development. The information in this document is based on initial product characterization. Vitesse reserves the right to alter specifications, features, capabilities, functions, manufacturing release dates, and even general availability of the product at any time. The reader is cautioned to confirm this datasheet is current prior to using it for design.

Warning

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Application Notes

Interconnecting the Byte Clocks (TXLSCKOUT and TXLSCKIN)

The byte clock (TXLSCKOUT and TXLSCKIN) on the VSC8114 has been brought off-chip to allow as much flexibility in system-level clocking schemes as possible. Since the byte clock (TXLSCKOUT) clocks both the VSC8114 and the UNI devices, it is important to pay close attention to the routing of this signal. The UNI device in general is a CMOS part which can have very wide spreads in timing (1-11ns clock in to parallel data out for the PM5355), which utilizes most of the 12.86ns period (at 78MHz), leaving little for the trace delays and set-up times required to interconnect the 2 devices.

The VSC8114 and the UNI device should be placed as close to each other as possible to provide maximum setup and hold time margin at the inputs of the VSC8114. Figure 12 suggests two different ways of routing the TXLSCKOUT-to-TXLSCKIN clock trace when used in a 622 MHz mode, which ever method is used the transmission line trace impedance should be no lower than 75 ohms.

Figure 12: Interconnecting the Byte Clocks
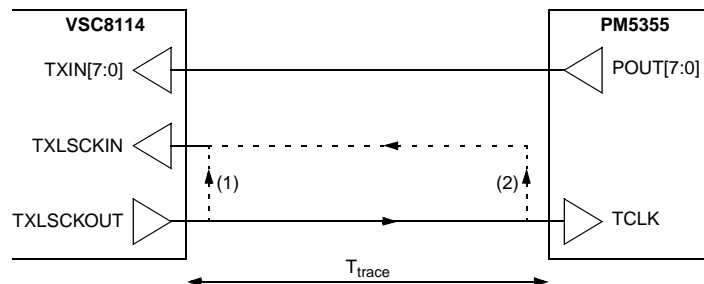
(1) TXLSCKOUT and TXLSCKIN are tied together at the pins of the VSC8114. This provides a setup and hold time margin for the TXIN input of

- $T_{su,margin} = T_{clk} - T_{TCLK-POUT,max}(PM5355) - T_{su,min}(VSC8114) - 2xT_{trace} = 0.86ns - 2xT_{trace}$

- $T_{hold,margin} = T_{TCLK-POUT,min}(PM5355) - T_{hold,min}(VSC8114) + 2xT_{trace} = 2xT_{trace}$

(2) TXLSCKOUT is daisy chained to the UNI device and then routed back to the VSC8114 along with the byte data. This interface provides a setup and hold time margin for the TXIN input of

- $T_{su,margin} = T_{clk} - T_{TCLK-POUT,max}(PM5355) - T_{su,min}(VSC8114) = 0.86ns$

- $T_{hold,margin} = T_{TCLK-POUT,min}(PM5355) - T_{hold,min}(VSC8114) = 0ns$

Option (2) does not provide any hold time margin, while option (1) requires the one-way trace delay (T_{trace}) to be less than 0.43ns (~3 inches).

The general recommendation is to apply option (1) and place the VSC8114 and PM5355 as close to each other as possible. If the one-way trace delay cannot be kept less than 0.43ns with a 50pf load, daisy-chaining (option 2) should be applied - close attention must be paid to signal routing in this case because of the lack of hold time margin.

Important note: The 11 ns max Tpd on the PM5355 assumes a 50pf load @ 60ps/pf, therefore 3 ns of the max delay is due to loading. The VSC8114 input (TXLSCKIN) plus package is about 6pf. Assuming about 1 pf/inch of 75 ohm trace on FR4 plus the VSC8114 6pf load, the user would in most cases choose option 1.

DC Coupling and Terminating High-speed PECL I/Os

The high speed signals on the VSC8114 (RXDATAIN, RXCLKIN, TXDATAOUT, REFCLKP, LOSPECL) use 3.3/5V programmable PECL I/Os which can be direct coupled to either +3.3V PECL or +5V PECL signals from the optics. These PECL levels are essentially ECL levels shifted positive by 3.3 volts or 5 volts. These PECL I/Os are referenced to the V_{DDP} supply (VDDP) and are terminated to ground. To program these I/Os for either 3.3V or 5V interface, the 3 V_{DDP} pins (pin 9, 15, 21) are required to connect to 3.3V or 5V supplies accordingly.

AC Coupling and Terminating High-speed PECL I/Os

If the optics modules provide ECL level interface, the high speed signals can be AC coupled to the VSC8114 as well. The PECL receiver inputs of the VSC8114 are internally biased at VDD/2. Therefore, AC-coupling to the VSC8114 inputs is accomplished by providing the pull-down resistor for the open-source PECL output and an AC-coupling capacitor used to eliminate the DC component of the output signal. This capacitor allows the PECL receivers of the VSC8114 to self-bias via its internal resistor divider network (see Figure 14).

The PECL output drivers are capable of sourcing current but not sinking it. To establish a LOW output level, a pull-down resistor, traditionally connected to VDD-2.0V, is needed when the output FET is turned off. Since VDD-2.0V is usually not present in the system, the resistor should be terminated to ground for convenience. The VSC8114 output drivers should be either AC-coupled to the 5.0V PECL inputs of the optics module, or translated (DC level shift). Appropriate biasing techniques for setting the DC-level of these inputs should be employed.

The dc biasing and 50 ohm termination requirements can easily be integrated together using a thevenin equivalent circuit as shown in Figure 14. The figure shows the appropriate termination values when interfacing 3.3V PECL to 5.0V PECL. This network provides the equivalent 50 ohm termination for the high speed I/Os and also provides the required dc biasing for the receivers of the optics module. Table 15 contains recommended values for each of the components.

TTL Input Structure

The TTL inputs of the VSC8114 are 3.3V TTL which can accept 5.0V TTL levels within a given set of tolerances (see Table 8). The input structure, shown in Figure 14, uses a current limiter to avoid overdriving the input FETs.

Initialization

The VSC8114 contains a "RESET" cap's pin which is only needed for VLSI production test requirements at Vitesse. The chip will initialize on its own as data is clocked through the device. The receive section will frame align on the A1, A2 boundary of the incoming SONET/SDH data stream. (See Receive section on page 3).

Layout of the High Speed Signals

The routing of the High Speed signals should be done using good high speed design practices. This would include using controlled impedance lines and keeping the distance between components to an absolute minimum. In addition, stubs should be kept at a minimum as well as any routing discontinuities. This will help minimize reflections and ringing on the high speed lines and insure the maximum eye opening. In addition the output pull down resistor should be placed as close to the VSC8114 pin as possible while the AC-coupling capacitor and the biasing resistors should be placed as close as possible to the optics input pin. The same is true on the receive circuit side. Using small outline components and minimum pad sizes also helps in reducing discontinuities.

Ground Planes

The ground plane for the components used in the High Speed interface should be continuous and not sectioned in an attempt to provide isolation to various components. Sectioning of the ground planes tends to interfere with the ground return currents on the signal lines. In addition, the smaller the ground planes the less effective they are in reducing ground bounce noise and the more difficult to decouple. Sectioning of the positive supplies can provide some isolation benefits.

Figure 13: AC Coupled High Speed I/O
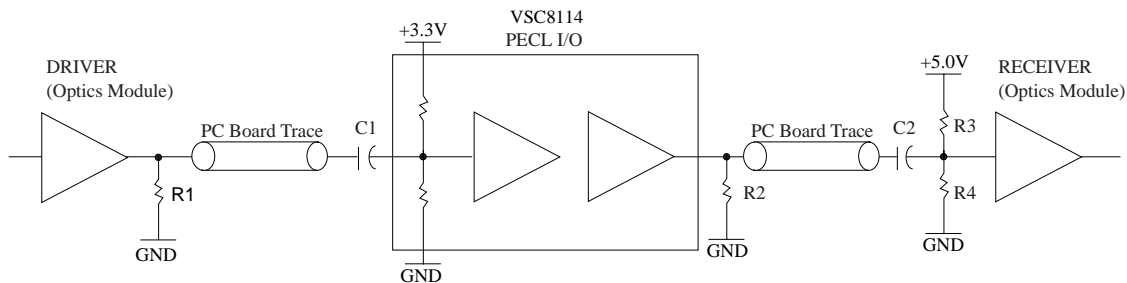
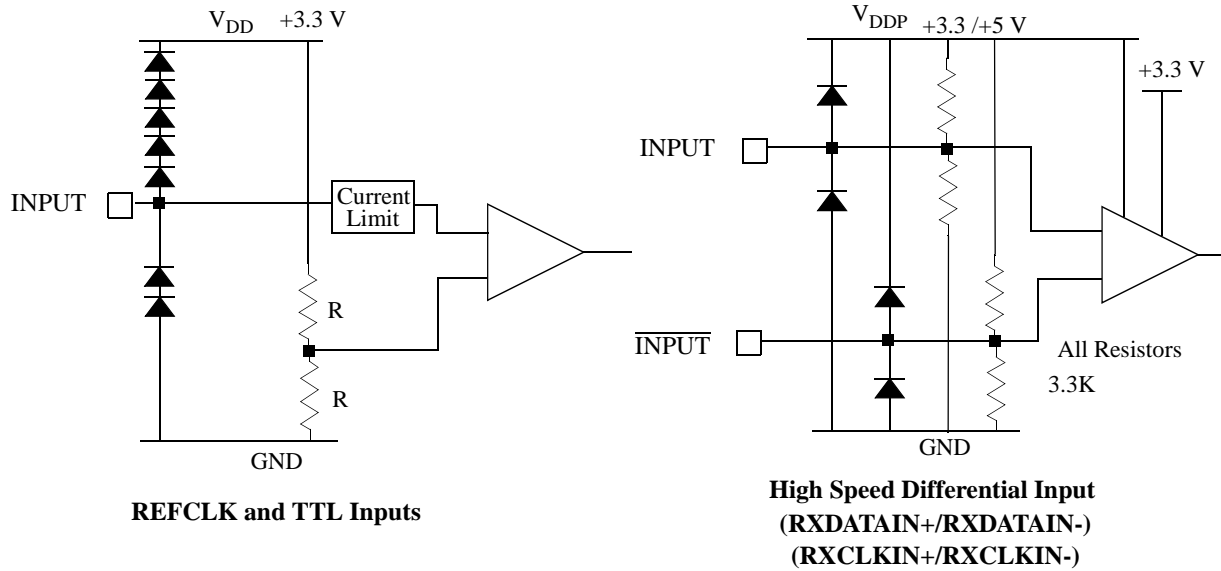Note: Only one side of a differential signal is shown.

Table 15: AC Coupling Component Values

Component	Value	Tolerance
R1	270 ohms	5%
R2	75 ohms	5%
R3	68 ohms	1%
R4	190 ohms	1%
C1, C2, C3, C4	.01uf High Frequency	

Figure 14: ¥Input Structures

REFCLK and TTL Inputs

High Speed Differential Input
(RXDATAIN+/RXDATAIN-)
(RXCLKIN+/RXCLKIN-)