Winbond Electronics Corp.

STEPLESS 200MHZ 3-DIMM CLOCK FOR SOLANO CHIPSET

1.0 GENERAL DESCRIPTION

The W83195BR-S is a Clock Synthesizer for Intel 815 Solano chipset. W83195BR-S provides all clocks required for high-speed RISC or CISC microprocessor and also provides 64 different frequencies of CPU, SDRAM, PCI, 3V66, IOAPIC clocks frequency setting. All clocks are externally selectable with smooth transitions.

The W83195BR-S provides I^2C serial bus interface to program the registers to enable or disable each clock outputs and provides 0.25% and 0.5% center type spread spectrum to reduce EMI. A watch dog timer is quipped and when time out, the RESET# pin will output 4ms pulse signal.

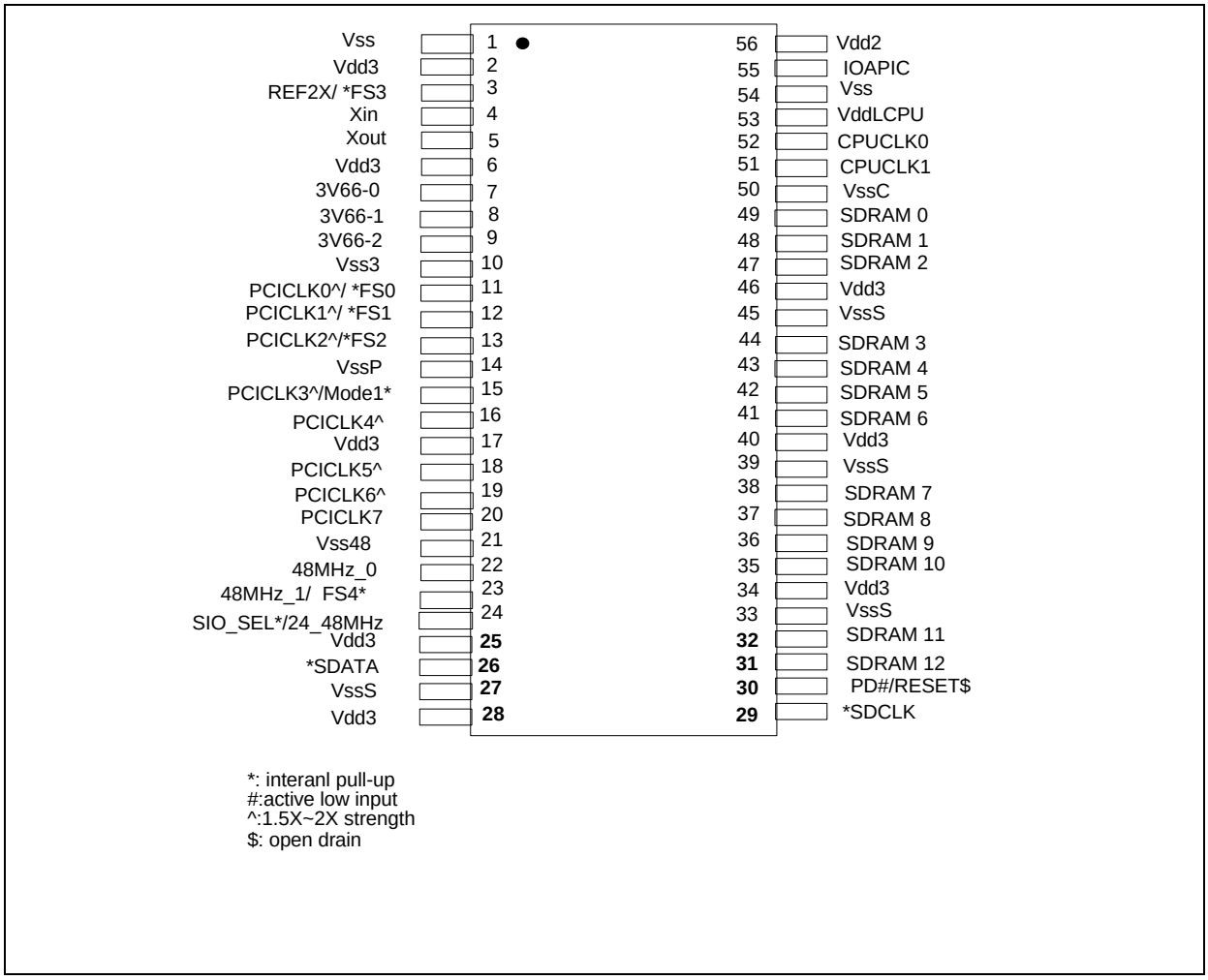
The W83195BR-S provides stepless frequency programming by controlling the VCO freq. and the clock output divisor ratio. Also the skew of CPU, SDRAM and 3V66 clock outputs are programmable.

The W83195BR-S accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. High drive PCI and SDRAM CLOCK outputs typically provide greater than 1 V /ns slew rate into 30 pF loads. CPU CLOCK outputs typically provide better than 1 V /ns slew rate into 20 pF loads as maintaining 50± 5% duty cycle. The fixed frequency outputs as REF, 24MHz, and 48 MHz provide better than 0.5V /ns slew rate.

2.0 PRODUCT FEATURES

- 2 CPU clocks
- 3 3V66 for chipset and AGP clocks
- 12 SDRAM clocks for 3 DIMMs
- 8 PCI synchronous clocks.
- Optional single or mixed supply:
  (VddR = VddP=VddS = Vdd48 = Vdd3 = 3.3V, VddLAPIC=VddLCPU=2.5V)
- Skew form CPU to PCI clock -1 to 4 ns, center 2.6 ns
- Smooth frequency switch with selections from 66.8 to 200 MHz
- I^2C 2-Wire serial interface and I^2C read back
- 0.25% and 0.5% center type spread spectrum
- Programmable registers to enable/stop each output and select modes
  (mode as Tri-state or Normal)
- Two 48 MHz pins for USB
- 24 MHz for super I/O
- 56-pin SSOP package

3.0 PIN CONFIGURATION



*: interanl pull-up
#:active low input
^:1.5X~2X strength
$: open drain

4.0 FREQUENCY SELECTION BY HARDWARE

FS4	FS3	FS2	FS1	FS0	CPU(MHz)	SDRAM (MHz)	3V66(MHz)	PCI(MHz)	IOAPIC (MHz)
0	0	0	0	0	75.30	112.95	75.30	37.65	18.83
0	0	0	0	1	95.00	95.00	63.33	31.67	15.83
0	0	0	1	0	129.00	129.00	86.00	43.00	21.50
0	0	0	1	1	150.00	113.00	75.33	37.67	18.83
0	0	1	0	0	150.00	150.00	75.00	37.50	18.75
0	0	1	0	1	110.00	110.00	73.33	36.67	18.33
0	0	1	1	0	140.00	140.00	70.00	35.00	17.50
0	0	1	1	1	144.00	108.00	72.00	36.00	18.00
0	1	0	0	0	68.30	102.45	68.30	34.15	17.08
0	1	0	0	1	105.00	105.00	70.00	35.00	17.50
0	1	0	1	0	138.00	138.00	69.00	34.50	17.25
0	1	0	1	1	140.00	105.00	70.00	35.00	17.50
0	1	1	0	0	66.80	100.20	66.80	33.40	16.70
0	1	1	0	1	100.20	100.20	66.80	33.40	16.70
0	1	1	1	0	133.60	133.60	66.80	33.40	16.70
0	1	1	1	1	133.60	100.20	66.80	33.40	16.70
1	0	0	0	0	157.30	118.00	78.67	39.33	19.67
1	0	0	0	1	160.00	120.00	80.00	40.00	20.00
1	0	0	1	0	146.00	110.00	73.33	36.67	18.33
1	0	0	1	1	122.00	91.50	61.00	30.50	15.25
1	0	1	0	0	127.00	127.00	84.67	42.33	21.17
1	0	1	0	1	122.00	122.00	81.33	40.67	20.33
1	0	1	1	0	117.00	117.00	78.00	39.00	19.50
1	0	1	1	1	114.00	114.00	76.00	38.00	19.00
1	1	0	0	0	80.00	120.00	80.00	40.00	20.00
1	1	0	0	1	78.00	117.00	78.00	39.00	19.50
1	1	0	1	0	166.00	166.00	83.00	41.50	20.75
1	1	0	1	1	160.00	160.00	80.00	40.00	20.00
1	1	1	0	0	66.60	100.00	66.67	33.33	16.67
1	1	1	0	1	100.00	100.00	66.67	33.33	16.67
1	1	1	1	0	133.30	133.30	66.65	33.33	16.66
1	1	1	1	1	133.30	100.00	66.67	33.33	16.67

5.0 SERIAL CONTROL 0REGISTERS

The Pin column lists the affected pin number and the @PowerUp column gives the state at true power up. Registers are set to the values shown only on true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the below described sequence (Register 0, Register 1, Register 2, ...) will be valid and acknowledged.

Frequency Table Setting by I2C (SEL5 ~ SEL0)

SSEL5	SSEL4	SSEL3	SSEL2	SSEL1	SSEL0	CPU (MHz)	SDRAM (MHz)	3V66 (MHz)	PCI(MHz)	IOAPIC (MHz)
0	0	0	0	0	0	75.30	112.95	75.30	37.65	18.83
0	0	0	0	0	1	95.00	95.00	63.33	31.67	15.83
0	0	0	0	1	0	129.00	129.00	86.00	43.00	21.50
0	0	0	0	1	1	150.00	113.00	75.33	37.67	18.83
0	0	0	1	0	0	150.00	150.00	75.00	37.50	18.75
0	0	0	1	0	1	110.00	110.00	73.33	36.67	18.33
0	0	0	1	1	0	140.00	140.00	70.00	35.00	17.50
0	0	0	1	1	1	144.00	108.00	72.00	36.00	18.00
0	0	1	0	0	0	68.30	102.45	68.30	34.15	17.08
0	0	1	0	0	1	105.00	105.00	70.00	35.00	17.50
0	0	1	0	1	0	138.00	138.00	69.00	34.50	17.25
0	0	1	0	1	1	140.00	105.00	70.00	35.00	17.50
0	0	1	1	0	0	66.80	100.20	66.80	33.40	16.70
0	0	1	1	0	1	100.20	100.20	66.80	33.40	16.70
0	0	1	1	1	0	133.60	133.60	66.80	33.40	16.70
0	0	1	1	1	1	133.60	100.20	66.80	33.40	16.70
0	1	0	0	0	0	157.30	118.00	78.67	39.33	19.67
0	1	0	0	0	1	160.00	120.00	80.00	40.00	20.00
0	1	0	0	1	0	146.00	110.00	73.33	36.67	18.33
0	1	0	0	1	1	122.00	91.50	61.00	30.50	15.25
0	1	0	1	0	0	127.00	127.00	84.67	42.33	21.17
0	1	0	1	0	1	122.00	122.00	81.33	40.67	20.33
0	1	0	1	1	0	117.00	117.00	78.00	39.00	19.50
0	1	0	1	1	1	114.00	114.00	76.00	38.00	19.00
0	1	1	0	0	0	80.00	120.00	80.00	40.00	20.00
0	1	1	0	0	1	78.00	117.00	78.00	39.00	19.50
0	1	1	0	1	0	166.00	166.00	83.00	41.50	20.75
0	1	1	0	1	1	160.00	160.00	80.00	40.00	20.00

0	1	1	1	0	0	66.60	100.00	66.67	33.33	16.67
0	1	1	1	0	1	100.00	100.00	66.67	33.33	16.67
0	1	1	1	1	0	133.30	133.30	66.65	33.33	16.66
0	1	1	1	1	1	133.30	100.00	66.67	33.33	16.67
SSEL5	**SSEL4**	**SSEL3**	**SSEL2**	**SSEL1**	**SSEL0**	**CPU (MHz)**	**SDRAM (MHz)**	**3V66 (MHz)**	**PCI(MHz)**	**IOAPIC (MHz)**
1	0	0	0	0	0	136.00	102.00	68.00	34.00	17.00
1	0	0	0	0	1	138.00	138.00	69.00	34.50	17.25
1	0	0	0	1	0	139.00	104.25	69.50	34.75	17.38
1	0	0	0	1	1	141.00	105.75	70.50	35.25	17.63
1	0	0	1	0	0	142.00	142.00	71.00	35.50	17.75
1	0	0	1	0	1	142.00	106.50	71.00	35.50	17.75
1	0	0	1	1	0	143.00	143.00	71.50	35.75	17.88
1	0	0	1	1	1	143.00	107.25	71.50	35.75	17.88
1	0	1	0	0	0	144.00	144.00	72.00	36.00	18.00
1	0	1	0	0	1	144.00	108.00	72.00	36.00	18.00
1	0	1	0	1	0	146.00	146.00	73.00	36.50	18.25
1	0	1	0	1	1	146.00	109.50	73.00	36.50	18.25
1	0	1	1	0	0	147.00	147.00	73.50	36.75	18.38
1	0	1	1	0	1	147.00	110.25	73.50	36.75	18.38
1	0	1	1	1	0	148.00	148.00	74.00	37.00	18.50
1	0	1	1	1	1	148.00	111.00	74.00	37.00	18.50
1	1	0	0	0	0	149.00	111.75	74.50	37.25	18.63
1	1	0	0	0	1	152.00	152.00	76.00	38.00	19.00
1	1	0	0	1	0	153.00	114.75	76.50	38.25	19.13
1	1	0	0	1	1	156.00	156.00	78.00	39.00	19.50
1	1	0	1	0	0	157.00	117.75	78.50	39.25	19.63
1	1	0	1	0	1	158.00	158.00	79.00	39.50	19.75
1	1	0	1	1	0	159.00	119.25	79.50	39.75	19.88
1	1	0	1	1	1	160.00	160.00	80.00	40.00	20.00
1	1	1	0	0	0	162.00	121.50	81.00	40.50	20.25
1	1	1	0	0	1	164.00	123.00	82.00	41.00	20.50
1	1	1	0	1	0	170.00	127.50	85.00	42.50	21.25
1	1	1	0	1	1	175.00	116.67	77.78	38.89	19.44
1	1	1	1	0	0	180.00	120.00	80.00	40.00	20.00
1	1	1	1	0	1	185.00	185.00	61.67	30.83	15.42
1	1	1	1	1	0	190.00	126.67	63.33	31.67	15.83
1	1	1	1	1	1	200.40	133.60	66.80	33.40	16.70

5.1 Register 0: Control Register

Bit	@PowerUp	Pin	Description
7	X	-	FS0#
6	X	-	FS1#
5	X	-	FS2#
4	X	-	FS3#
3	X	-	FS4#
2	1	-	If Reg0-bit7=1 0 = ± 0.5% Center type Spread Spectrum Modulation 1 = ± 0.25% Center type Spread Spectrum Modulation If Reg0-bit7=0 0 = 0 ~ - 1 % Down type Spread Spectrum Modulation 1 = 0 ~ - 0.5% Down type Spread Spectrum Modulation
1	0	-	0 = Normal 1 = Spread Spectrum enabled
0	1	-	1=CENTER SPREAD 0=DOWN SPREAD

5.2 Register 1 : SDRAM Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	38	SDRAM7 (Active / Inactive)
6	1	41	SDRAM6 (Active / Inactive)
5	1	42	SDRAM5 (Active / Inactive)
4	1	43	SDRAM4 (Active / Inactive)
3	1	44	SDRAM3 (Active / Inactive)
2	1	47	SDRAM2 (Active / Inactive)
1	1	48	SDRAM1 (Active / Inactive)
0	1	49	SDRAM0 (Active / Inactive)

5.3 Register 2: PCI Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	20	PCICLK7 (Active / Inactive)
6	1	19	PCICLK6 (Active / Inactive)
5	1	18	PCICLK5 (Active / Inactive)
4	1	16	PCICLK4 (Active / Inactive)
3	1	15	PCICLK3 (Active / Inactive)
2	1	13	PCICLK2 (Active / Inactive)
1	1	12	PCICLK1 (Active / Inactive)
0	1	11	PCICLK0 (Active / Inactive)

5.4 Register 3: Control Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	9	3V66_2(Active/Inactive)
6	1	8	3V66_1(Active / Inactive)
5	1	7	3V66_0(Active / Inactive)
4	1	31	SDRAM12 (Active / Inactive)
3	1	32	SDRAM11 (Active / Inactive)
2	1	35	SDRAM10 (Active / Inactive)
1	1	36	SDRAM9 (Active / Inactive)
0	1	37	SDRAM8 (Active / Inactive)

5.5 Register 4: Control Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	0	-	SSEL3 (Frequency table selection by software via I^2C)
6	0	-	SSEL2 (Frequency table selection by software via I^2C)
5	0	-	SSEL1 (Frequency table selection by software via I^2C)
4	0	-	SSEL0 (Frequency table selection by software via I^2C)
3	0	-	0 = Selection by hardware 1 = Selection by software I^2C - Bit (1,2, 4:6)
2	0	-	SSEL4 (Frequency table selection by software via I^2C)
1	0	-	SSEL5 (Frequency table selection by software via I^2C)
0	0	-	0 = Running 1 = Tristate all outputs

5.6 Register 5: Skew Register

Bit	@PowerUp	Pin	Description
7	**1**	**-**	**CSkew2 (CPU to SDRAM skew program bit)**
6	**0**	**-**	**CSkew1 (CPU to SDRAM skew program bit)**
5	**0**	**-**	**CSkew0 (CPU to SDRAM skew program bit)**
4	**1**	**-**	**CASkew2 (CPU to 3V66 skew program bit)**
3	**0**	**-**	**CASkew1 (CPU to 3V66 skew program bit)**
2	**0**	**-**	**CASkew0 (CPU to 3V66 skew program bit)**
1	1	51	CPUCLK1(Active/Inactive)
0	1	52	CPUCLK0(Active / Inactive)

5.7 Register 6~10: Step-less M/N control registers

5.12 Register 11: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	0	-	Winbond Chip ID
6	1	-	Winbond Chip ID
5	0	-	Winbond Chip ID
4	1	-	Winbond Chip ID
3	0	-	Winbond Chip ID
2	0	-	Winbond Chip ID
1	0	-	Winbond Chip ID
0	0	-	Winbond Chip ID

5.13 Register 12: Winbond Chip ID Register (Read Only)

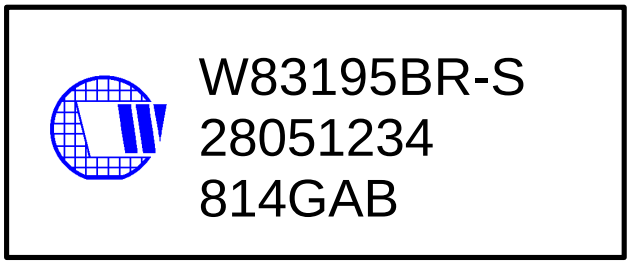
Bit	@PowerUp	Pin	Description
7	**0**	**-**	**Winbond Chip ID**
6	**0**	**-**	**Winbond Chip ID**
5	**1**	**-**	**Winbond Chip ID**
4	**0**	**-**	**Winbond Chip ID**
3	**0**	**-**	**Winbond Chip ID**
2	**0**	**-**	**Winbond Version ID**
1	**1**	**-**	**Winbond Version ID**
0	**0**	**-**	**Winbond Version ID**

Register10 Bit3-6				Ratio		
Bit6	Bit 5	Bit 4	Bit 3			
DS3	DS2	DS1	DS0	CPU	SDRAM	3V66
0	0	0	0	4	4	6
0	0	0	1	3	3	6
0	0	1	0	2	3	6
0	0	1	1	2	2	6
0	1	0	0	6	4	6
0	1	0	1	3	4	6
0	1	1	0	6	3	6
0	1	1	1	4	3	6
1	0	x	x	2	2	4
1	1	x	x	2	4	6

6.0 ORDERING INFORMATION

Part Number	Package Type	Production Flow
W83195BR-S	56 PIN SSOP	Commercial, 0°C to +70°C

7.0 HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83195BR-S

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 814 G B B

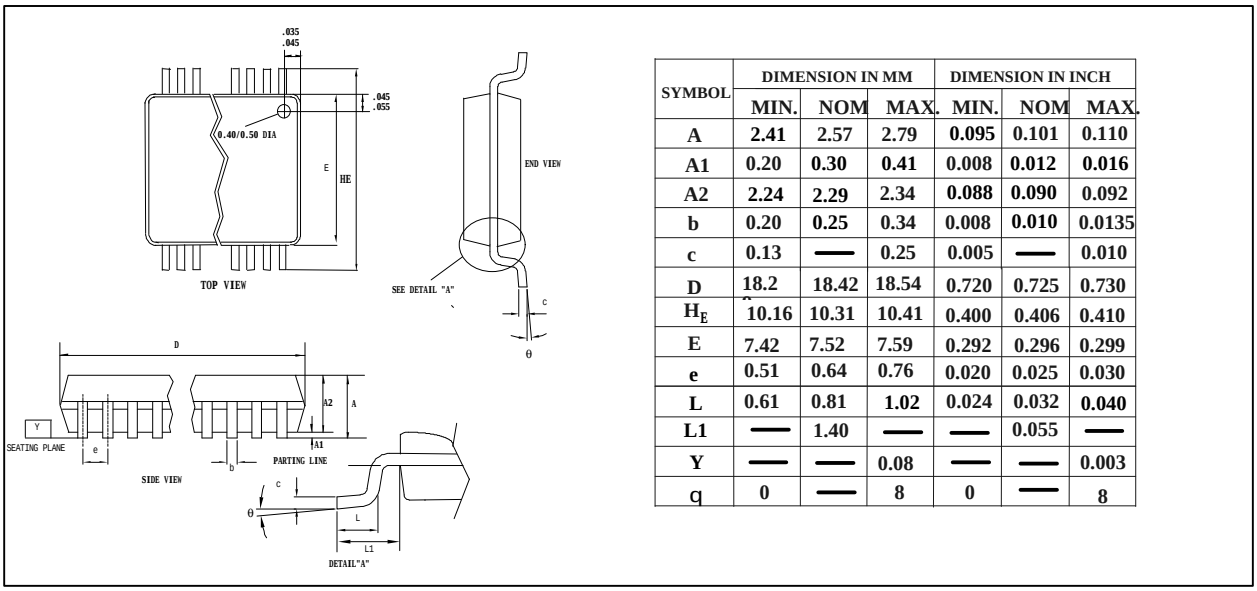
814: packages made in '98, week 14

G: assembly house ID; O means OSE, G means GR

A: Internal use code

B: IC revision

8.0 PACKAGE DRAWING AND DIMENSIONS



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	2.41	2.57	2.79	0.095	0.101	0.110
A1	0.20	0.30	0.41	0.008	0.012	0.016
A2	2.24	2.29	2.34	0.088	0.090	0.092
b	0.20	0.25	0.34	0.008	0.010	0.0135
c	0.13	—	0.25	0.005	—	0.010
D	18.2	18.42	18.54	0.720	0.725	0.730
H_E	10.16	10.31	10.41	0.400	0.406	0.410
E	7.42	7.52	7.59	0.292	0.296	0.299
e	0.51	0.64	0.76	0.020	0.025	0.030
L	0.61	0.81	1.02	0.024	0.032	0.040
L1	—	1.40	—	—	0.055	—
Y	—	—	0.08	—	—	0.003
q	0	—	8	0	—	8

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