W81181D/AD

USB HUB Controller

Publication Release Date: October 1999
Revision A1

W81181D Data Sheet Revision History

	Pages	Dates	Version	Version on Web	Main Contents
1	N.A.	10/01/98	0.50	N.A.	First published.
2		3/15/99	0.60		Add pin configuration and pin description
3		3/30/99	0.61		Modify pin configuration & pin description
4		5/4/99	0.62		Modify reference schematic
5		5/13/99	0.63		Modify pin 12 description
6		5/26/1999	0.64		Modify feature HUB spec Rev 1.1
7		7/09/1999	0.65		Add 48 MHz clock input pinout
8		7/12/1999	0.66		Modify 48 MHz (W81181AD) Schematic
9					
10					

LIFE SUPPORT APPLICATIONS

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1. GENERAL DESCRIPTION

W81181D, an high integrated 4 port USB hub controller which integrates a microcontroller, implements a medium speed (12 MHz) and slow speed (1.5 MHz) Universal Serial Bus (USB) hub control interface. It supports one upstream, four downstream ports and a serial interface. W81181D can be act as multifunction USB device. For example, the whole system can be designed as an USB HUB plus an USB mouse or an USB HUB plus an IR receiver, and no down stream port be occupied as well as no other component needed.

W81181D acts as an USB hub controller and a hub repeater at the direction of an internal microcontroller. W81181D controls the traffic among the host, four downstream ports, and the microprocessor. As a hub controller, it can enable/disable ports, send and receive resets, and detect devices of high or low speeds. The W81181D contains three function endpoints and two hub endpoints to allow both USB Control and Interrupt Transfers between the host and microcontroller.

W81181D is a compound USB device (hub with embedded function attached) with totally five downstream ports. W81181D can be used as a hub controller in a standalone hub with attached function or a microcontroller based USB device with hub function.

Ordering Information

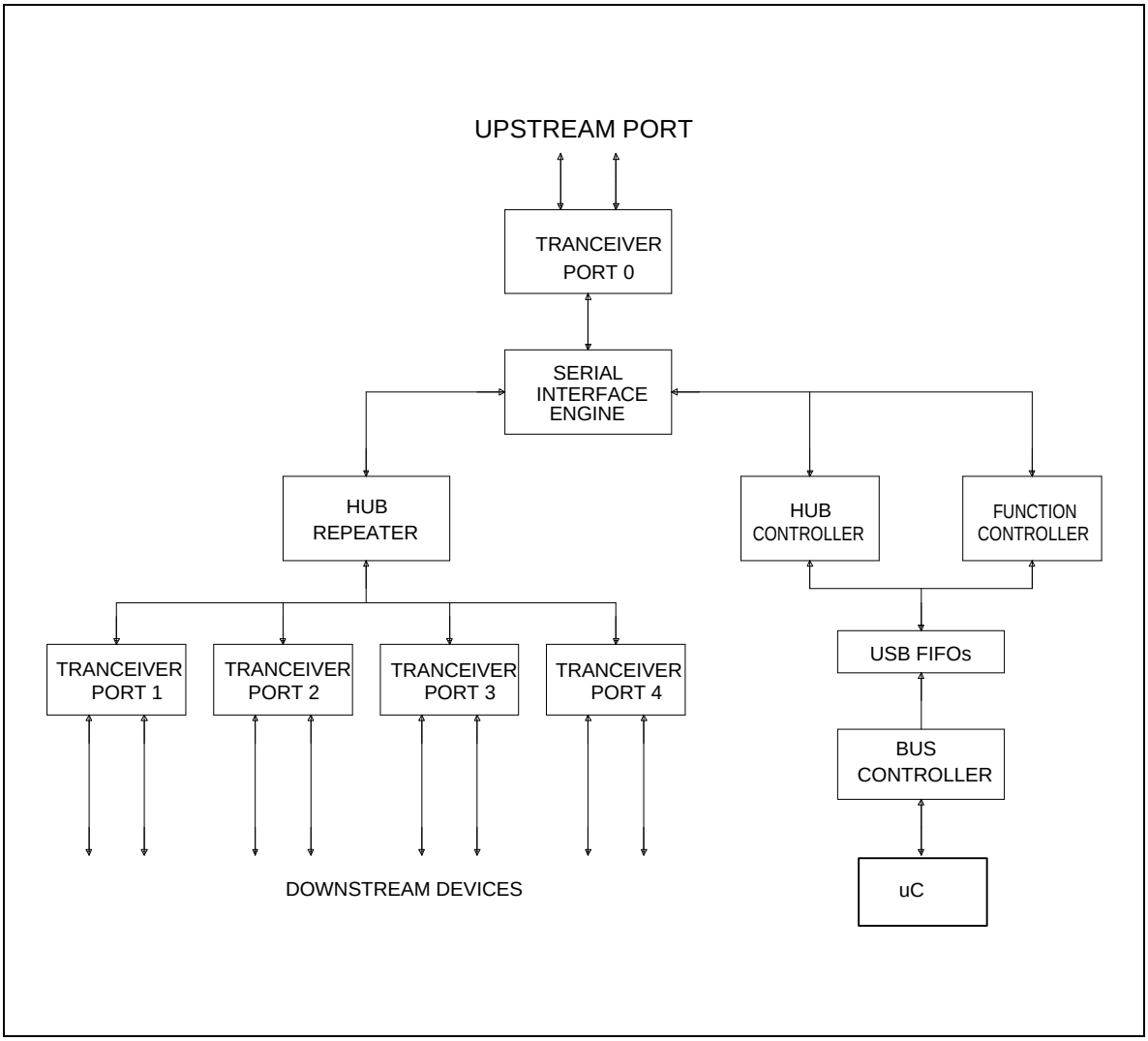
PART NO.	INPUT CLOCK Freq.	PACKAGE
W81181D	12 MHz	48-LQFP
W81181AD	48 MHz	48-LQFP

2. FEATURES

- Full compliance with USB spec Rev 1.1 and HID Class Definition Rev 1.0
- Compliance with USB Hub spec Rev 1.1
- Support multiple endpoints for standalone hub with attached function
- Embedded microprocessor--8052 (6K ROM + 256 Byte RAM)
- Support auto-detected two power source mode between bus power mode and self power mode.
- 12-MHz crystal/oscillator input to lower EMI (W81181D)
- 48-Mhz oscillator input for motherboard application (W81181AD)
- Support Suspend and Resume operation
- Four downstream ports with per port overcurrent protection
- Two endpoints for hub (Control and Interrupt)
- LED display supports bright/blinking alternative for port enable and OCP(over current protection) flags
- Single 5V supplied with embedded 5V-3.3V regulator
- Three endpoints for attached device (one Control and two Interrupt)
- Provides the external pull-up resistor control for the up-stream connection.
- Perport/Global downstream port power control optional
- Packaged in 48-pin LQFP
- 5V CMOS device

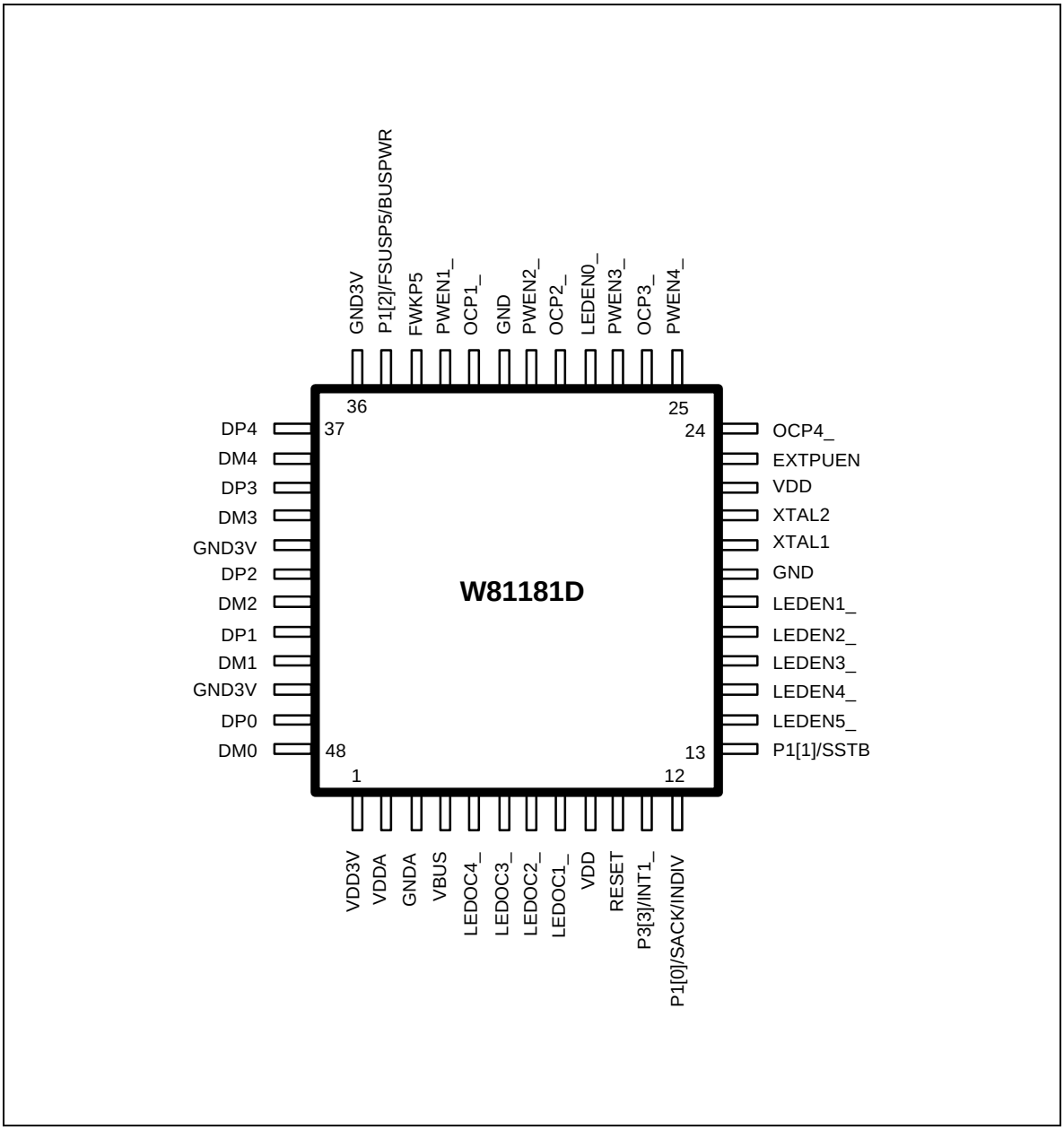
3. USB BLOCK DIAGRAM

The Serial Interface Engine (SIE) controls the USB data flow between the uCs and the USB bus. Port0 is a high speed (HS) transceiver for the upstream data path. The Hub Repeater is the traffic controller which directs the bus data to and from the correct paths. The hub Controller and Function Controller determines what data is to be written to or read from the various FIFOs. The Bus Controller directs the interface between the uC and Hub/Function Controller.

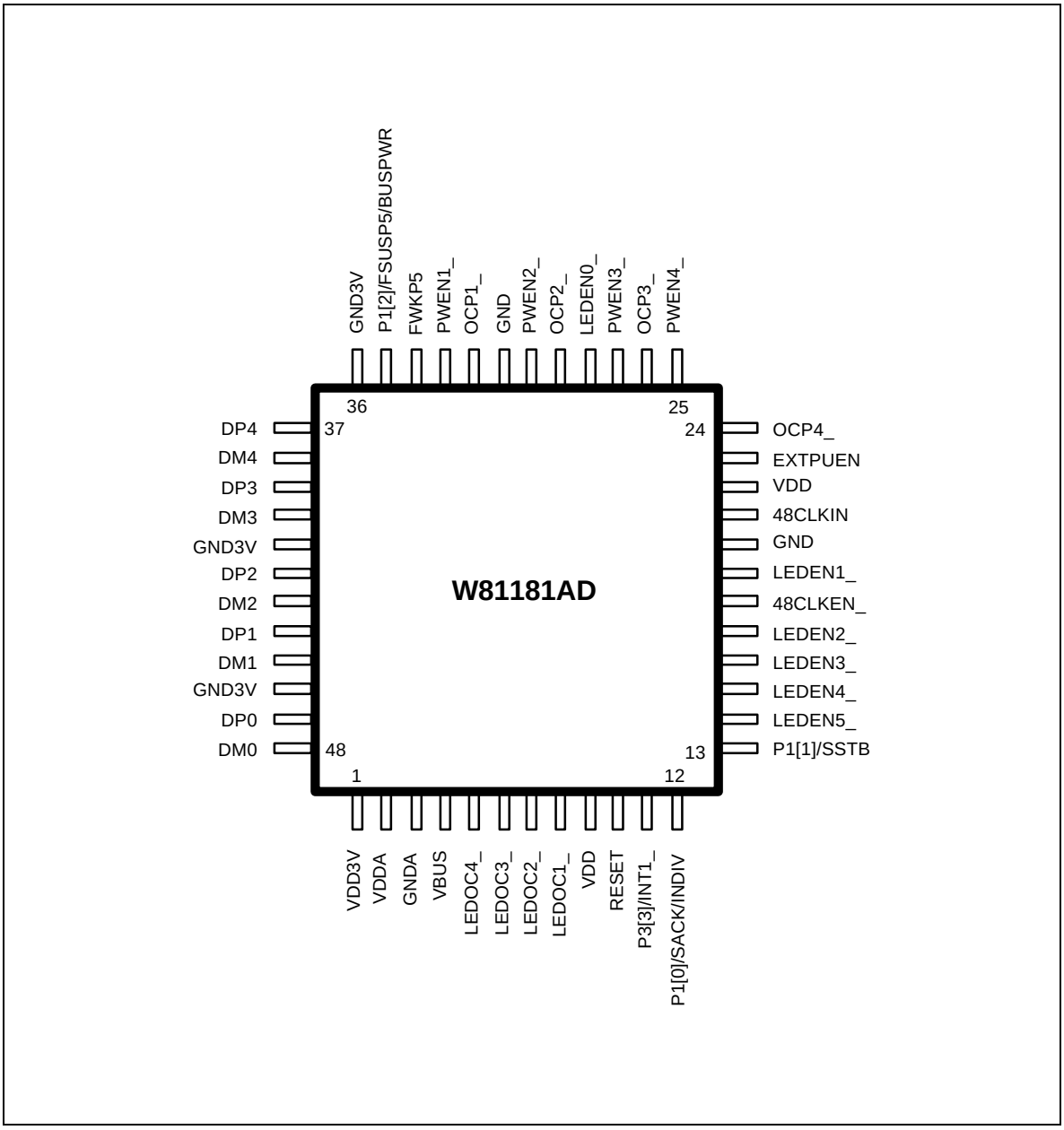


4. PIN CONFIGURATION

W81181D (12 MHz Clock Input)



W81181AD (48 MHz Clock Input)



5. PIN DESCRIPTION

W81181D

PIN NUMBER	PAD NAME	I/O TYPE	PIN FUNCTION	PULL UP/ DOWN
1	VDD3V	Power1	3.3V Regulator output. Supply voltage for all transceivers.	-
2	VDDA	Power1	Analog power.	-
3	GNDA	Power0	Analog ground.	-
4	VBUS	IUD2T	Input of upstream power status. On self-power mode, connection should be controlled by VBUS status.	-
5	LEDOC4_	IOU2P	Flag of port4 over-current. To drive LED directly	O
6	LEDOC3_	IOU2P	Flag of port3 over-current. To drive LED directly	O
7	LEDOC2_	IOU2P	Flag of port2 over-current. To drive LED directly	O
8	LEDOC1_	IOU2P	Flag of port1 over-current. To drive LED directly	O
9	VDD	Power1	Digital supply voltage.	-
10	RESET	IUD2T	Master reset input. Active high.	-
11	P3[3]/ INT1_	IOUD2	Normally, this pin is P33/INT1_ and used as bi-directional serial data (SDATA) for embedded function serial port.	U
12	P1[0]/ SACK/ INDIV	IOUD2	Normally, this pin is P10 and used as bi-directional serial data ACK (SACK) for embedded function serial port. If no embedded function this pin is INDIVIDUAL (default) or GANGED mode setting for downstream power control.	U
13	P1[1]/ SSTB	IOUD2	Normally, this pin is P11 and used as bi-directional serial data Strobe (SSTB) for embedded function serial port.	U
14	LEDEN5_	IOU2P	Downstream port5 LED. Active low to drive bright/blinking LED when port5 enable.	O
15	LEDEN4_	IOU2P	Downstream port4 LED. Active low to drive bright/blinking LED when port4 enable.	O
16	LEDEN3_	IOU2P	Downstream port3 LED. Active low to drive bright/blinking LED when port3 enable.	O
17	LEDEN2_	IOU2P	Downstream port2 LED. Active low to drive bright/blinking LED when port2 enable.	O
18	LEDEN1_	IOU2P	Downstream port1 LED. Active low to drive bright/blinking LED when port1 enable.	O
19	GND	Power0	Digital ground	-
20	XTAL1	OSCM	Crystal IN. For 12 MHz oscillation.	-

Pin Description (W81181D), continued

PIN NUMBER	PAD NAME	I/O TYPE	PIN FUNCTION	PULL UP/ DOWN
21	XTAL2	OSCM	Crystal OUT. For 12 MHz oscillation.	-
22	VDD	Power1	Digital supply voltage.	
23	EXTPUEN	O2	External pull-up connection control.	O
24	OCP4_	IUD2T	Downstream port4 over-current status. Active low.	-
25	PWEN4_	O2	Downstream port4 power control. Active low.	O
26	OCP3_	IUD2T	Downstream port3 over-current status. Active low.	-
27	PWEN3_	O2	Downstream port3 power control. Active low.	O
28	LEDEN0_	IOU2P	Upstream port0 LED. Active low to drive bright/blinking LED when upstream port0 enable.	O
29	OCP2_	IUD2T	Downstream port2 over-current status. Active low.	-
30	PWEN2_	O2	Downstream port2 power control. Active low.	O
31	GND	Power0	Digital ground.	
32	OCP1_	IUD2T	Downstream port1 over-current LED. Active low.	-
33	PWEN1_	O2	Downstream port1 power control. Active low.	O
34	FWKP5	IUD2	Embedded function wake-up input.	D
35	P1[2]/ FSUSP5/ PWRDET	IOUD2	Normally, this pin is a P12 and used as embedded function suspend control. If no embedded function this pin is self-powered (High) or bus-powered (Low) hub setting.	
36	GND3V	Power0	Ground of port3 and port4 transceivers.	-
37	DP4	AIO	USB D+ for downstream port4.	-
38	DM4	AIO	USB D- for downstream port4.	-
39	DP3	AIO	USB D+ for downstream port3.	-
40	DM3	AIO	USB D- for downstream port3.	-
41	GND3V	Power0	Ground of port1 and port2 transceivers.	-
42	DP2	AIO	USB D+ for downstream port2.	-
43	DM2	AIO	USB D- for downstream port2.	-
44	DP1	AIO	USB D+ for downstream port1.	-
45	DM1	AIO	USB D- for downstream port1.	-
46	GND3V	Power0	Ground of port0 transceivers.	-
47	DP0	AIO	USB D+ for upstream port0.	-
48	DM0	AIO	USB D- for upstream port0.	-

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W81181AD

PIN NUMBER	PAD NAME	I/O TYPE	PIN FUNCTION	PULL UP/ DOWN
1	VDD3V	Power1	3.3V Regulator output. Supply voltage for all transceivers.	-
2	VDDA	Power1	Analog power.	-
3	GNDA	Power0	Analog ground.	-
4	VBUS	IUD2T	Input of upstream power status. On self-power mode, connection should be controlled by VBUS status.	-
5	LEDOC4_	IOU2P	Flag of port4 over-current. To drive LED directly	O
6	LEDOC3_	IOU2P	Flag of port3 over-current. To drive LED directly	O
7	LEDOC2_	IOU2P	Flag of port2 over-current. To drive LED directly	O
8	LEDOC1_	IOU2P	Flag of port1 over-current. To drive LED directly	O
9	VDD	Power1	Digital supply voltage.	-
10	RESET	IUD2T	Master reset input. Active high.	-
11	P3[3]/ INT1_	IOUD2	Normally, this pin is P33/INT1_ and used as bi-directional serial data (SDATA) for embedded function serial port.	U
12	P1[0]/ SACK/ INDIV	IOUD2	Normally, this pin is P10 and used as bi-directional serial data ACK (SACK) for embedded function serial port. If no embedded function this pin is INDIVIDUAL (default) or GANGED mode setting for downstream power control.	U
13	P1[1]/ SSTB	IOUD2	Normally, this pin is P11 and used as bi-directional serial data Strobe (SSTB) for embedded function serial port.	U
14	LEDEN5_	IOU2P	Downstream port5 LED. Active low to drive bright/blinking LED when port5 enable.	O
15	LEDEN4_	IOU2P	Downstream port4 LED. Active low to drive bright/blinking LED when port4 enable.	O
16	LEDEN3_	IOU2P	Downstream port3 LED. Active low to drive bright/blinking LED when port3 enable.	O
17	LEDEN2_	IOU2P	Downstream port2 LED. Active low to drive bright/blinking LED when port2 enable.	O
18	48CLKEN_	IUD2	High enable embedded DPLL (12 MHz to 48 MHz). It should be kept to Low when using 48Mhz clock.	U
19	LEDEN1_	IOU2P	Downstream port1 LED. Active low to drive bright/blinking LED when port1 enable.	O
20	GND	Power0	Digital ground	-

Pin Description (W81181AD), continued

PIN NUMBER	PAD NAME	I/O TYPE	PIN FUNCTION	PULL UP/ DOWN
21	48CLKIN	OSCM	Clock input for 48 MHz oscillation.	-
22	VDD	Power1	Digital supply voltage.	
23	EXTPUEN	O2	External pull-up connection control.	O
24	OCP4_	IUD2T	Downstream port4 over-current status. Active low.	-
25	PWEN4_	O2	Downstream port4 power control. Active low.	O
26	OCP3_	IUD2T	Downstream port3 over-current status. Active low.	-
27	PWEN3_	O2	Downstream port3 power control. Active low.	O
28	LEDEN0_	IOU2P	Upstream port0 LED. Active low to drive bright/blinking LED when upstream port0 enable.	O
29	OCP2_	IUD2T	Downstream port2 over-current status. Active low.	-
30	PWEN2_	O2	Downstream port2 power control. Active low.	O
31	GND	Power0	Digital ground.	
32	OCP1_	IUD2T	Downstream port1 over-current LED. Active low.	-
33	PWEN1_	O2	Downstream port1 power control. Active low.	O
34	FWKP5	IUD2	Embedded function wake-up input.	D
35	P1[2]/ FSUSP5/ PWRDET	IOUD2	Normally, this pin is a P12 and used as embedded function suspend control. If no embedded function this pin is self-powered (High) or bus-powered (Low) hub setting.	
36	GND3V	Power0	Ground of port3 and port4 transceivers.	-
37	DP4	AIO	USB D+ for downstream port4.	-
38	DM4	AIO	USB D- for downstream port4.	-
39	DP3	AIO	USB D+ for downstream port3.	-
40	DM3	AIO	USB D- for downstream port3.	-
41	GND3V	Power0	Ground of port1 and port2 transceivers.	-
42	DP2	AIO	USB D+ for downstream port2.	-
43	DM2	AIO	USB D- for downstream port2.	-
44	DP1	AIO	USB D+ for downstream port1.	-
45	DM1	AIO	USB D- for downstream port1.	-
46	GND3V	Power0	Ground of port0 transceivers.	-
47	DP0	AIO	USB D+ for upstream port0.	-
48	DM0	AIO	USB D- for upstream port0.	-

IO TYPE

IO TYPE	DESCRIPTION
Power1	Power
Power0	Ground
OSCM	Middle-freq. Oscillating IO
IUD2	Input with pull-up/pull-down control
IUD2T	Schmitt Input with pull-up/pull-down control
IOU2P	Bi-directional high driving IO with programmable pull-up control and serial resistor
IOUD2	Bi-directional IO with pull-up/pull-down control
O2	Output
AIO	Analog Transceiver IO

Pull Up/Down Control

NOTE	DESCRIPTION
O	Output pin without pull-up/down
D	Input pin or I/O pin with pull-down
U	Input pin or I/O pin with pull-up
-	Input pin or I/O pin without pull-up/down

6. ABSOLUTE MAXIMUM RATINGS

PARAMETER	LIMIT
Supply Voltage (Vcc to Vss)	5.5V
Analog Input Voltage	Vss -0.5V to Vcc +0.5V
Digital Input Voltage	Vss -0.5V to Vcc +0.5V
Power Dissipation	TBD
Ambient Operating Temperature	0^{o}C to 70^{o}C
Lead Temperature (Soldering, 10 sec)	250^{o}C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

7. ELECTRICAL CHARACTERISTICS

Operating Conditions

V_{CC} = 5V +/-5%, T_A = 0° to 70° C

PARAMETER	SYM.	CONDITIONS	MIN.	MAX.	UNIT
V_{CC} Supply Current	I_{CC}			TBD	mA
Logic Output High	V_{OH}	Io ≥ 24 mA	2.5	V_{CC}	V
Logic Output Low	V_{OL}	Io ≥ 6 mA		0.4	V
Logic Input Leakage Current		T_A = 70 °C		10	uA
USB CHARACTERISTICS		Note 8			
Leakage Current:					
Hi-Z State Output Leakage	I_{LO}	V< V_{IN} < 3.3V	-10	+10	uA
Input Levels:					
Differential Input Sensitivity	V_{DI}	|(D+)-(D-)|	0.2		V
Single Ended Signal "0"	V_{SE0}		0.8	2.0	V
Differential Common Mode Range	V_{CM}	Includes VDI range	0.8	2.5	
Output Levels:					
Driver Output Low	V_{OLU}	R_L of 1.5 KΩ to 3.6V		0.3	V
Driver Output High	V_{OHU}	R_L of 15 KΩ to GND	2.8	3.6	V
Output Signal Crossover Voltage	V_{CRS}		1.3	2.0	V
Capacitance:					
Transceiver Capacitance	C_{IN}	Pin to GND		20	pF
Full Speed Timings:					
Output Rise/Fall Times	t_R/t_F	Notes 1, 4 (C_L = 50 pF)	4	20	nS
Source Differential Driver Jitter to Next Transition /to Paired Transition	t_{DJ1} /t_{DJ2}	Notes 2, 3	-3.5 /-4	3.5 /4	nS nS
Differential to EOP transition Skew	t_{DEOP}	Note 3	-2	5	nS
Hub Differential Data Delay(without cable)	t_{HDD2}	Notes 2, 3, 5		44	ns
Hub Differential Driver Jitter to Next Transition /to Paired Transition (including cable)	t_{HDJ1} /t_{HDJ2}	Notes 2, 3, 5	-3 /-1	3 /1	nS
Data bit width distortion after SOP	t_{SOP}	Notes 3, 5	-5	5	nS
Hub SE0 Delay Relative to t_{HDD}	t_{EOPD}	Notes 3, 5	0	15	nS
Hub EOP Output Width Skew	t_{HESK}	Notes 3, 5	-15	15	nS
Low Speed Timings:					
Output Rise/Fall Times	t_R/t_F	Notes 1, 4 (C_L = 50 pF)	75	300	nS

Electrical Characteristics, continued

PARAMETER	SYM.	CONDITIONS	MIN.	MAX.	UNIT
Source Differential Driver Jitter to Next Transition	t_{DJ1}	Notes 2, 3	-25	25	nS
/to Paired Transition	/t_{DJ2}		/-14	/14	nS
Differential to EOP transition Skew	t_{DEOP}	Notes 3	-40	100	nS
Hub Differential Data Delay(without cable)	t_{HDD2}	Notes 2, 3, 5		300	nS
Hub Differential Driver Jitter to Next Transition	t_{HDJ1}	Notes 2, 3, 5	-45	45	nS
/to Paired Transition (including cable)	/t_{HDJ2}		/-45	/-45	
Data bit width distortion after SOP	t_{SOP}	Notes 3, 5	-60	60	nS
Hub SE0 Delay Relative to t_{HDD}	t_{EOPD}	Notes 3, 5	0	200	nS
Hub EOP Output Width Skew	t_{HESK}	Notes 3, 5	-300	300	nS

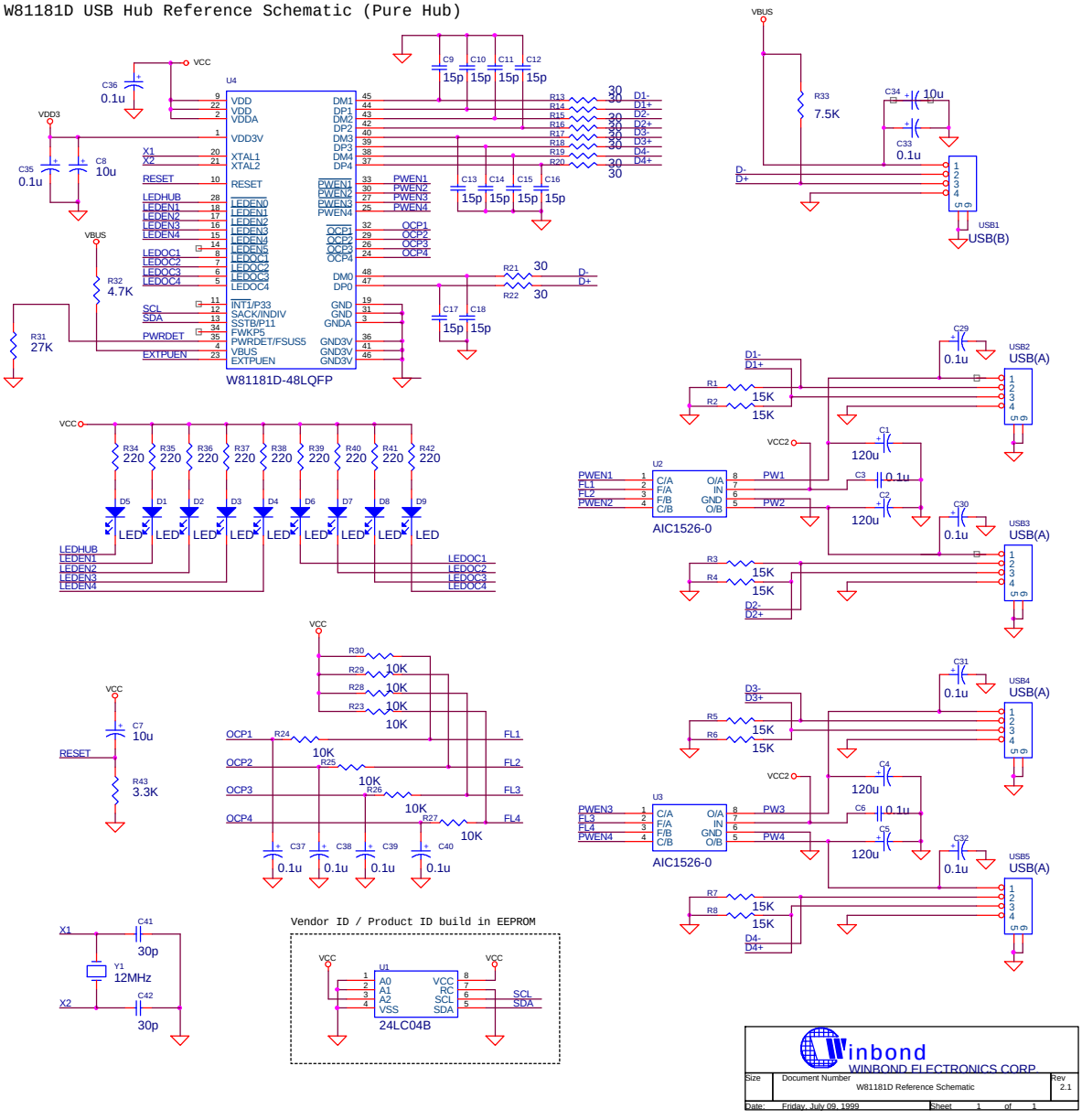
Notes:

1. Measured from 10% to 90% of the data signal.
2. Timing difference between the differential signals.
3. Measured at crossover point of differential data signals.
4. The rising and falling edges should be smoothly transiting(monotonic)
5. Full Speed timing have a 1.5 kΩ pull-up to 2.8 V on the D+ (DP) data line.
6. Low Speed timing have a 1.5 kΩ pull-up to 2.8 V on the D- (DM) data line.
7. The maximum load specification is the maximum effective capacitive load allowed that meets the target hub VBUS droop of 330 mV.
8. All other USB Electrical Characteristics refer to USB spec Rev 1.1 7.3.2 and 7.3.3.

8. TYPICAL APPLICATION

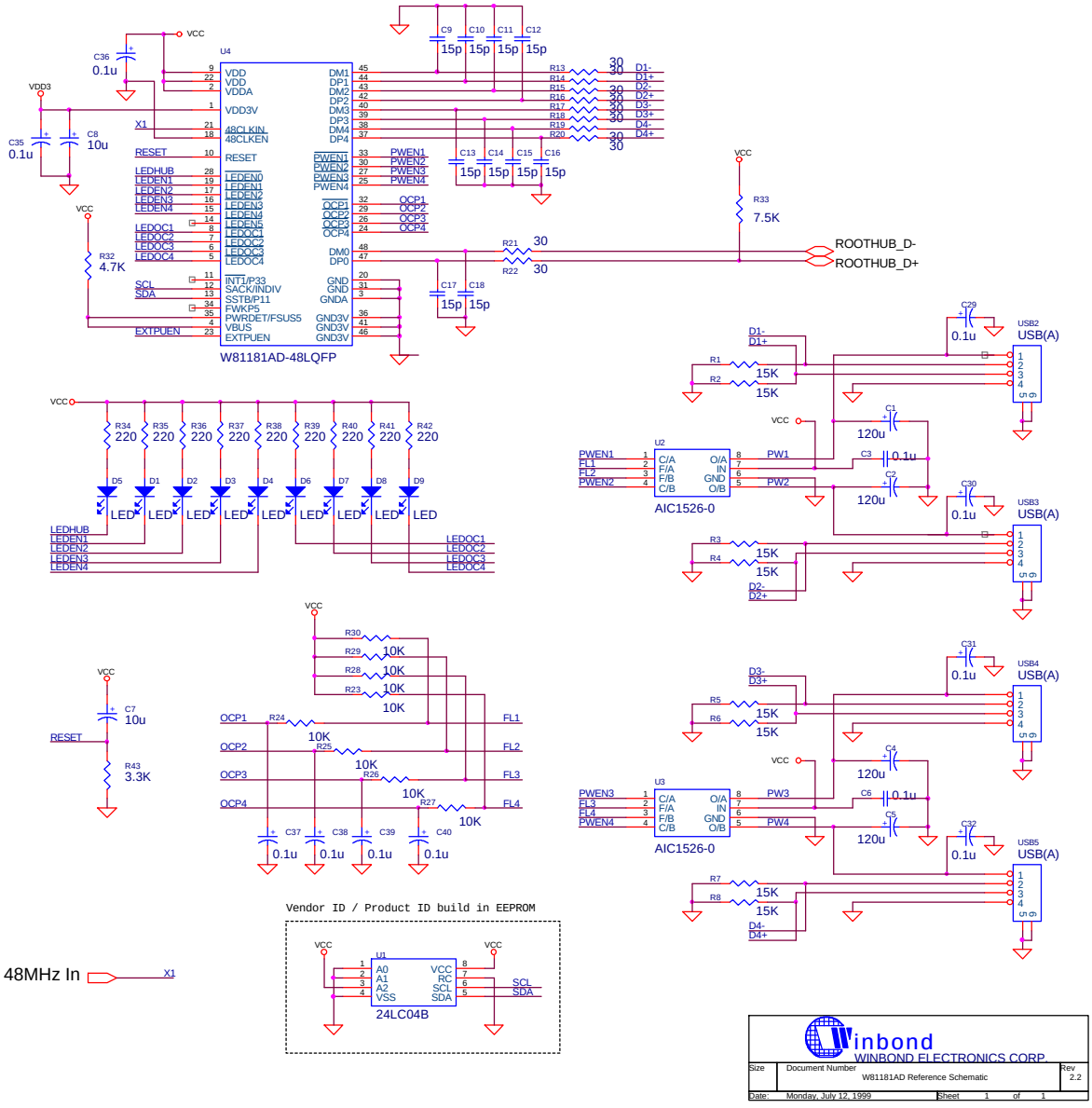
W81181D

W81181D USB Hub Reference Schematic (Pure Hub)



W81181AD

W81181AD USB Hub Reference Schematic (48MHz for Mother Board)



9. HOW TO READ THE TOP MARKING

The top marking of W81181D

Left: Winbond logo

1st line: Type number W8181, D means LQFP (Thickness = 1.4 mm)

2nd line: Tracking code

745 A A - 02A

745: packages made in '97, week 45

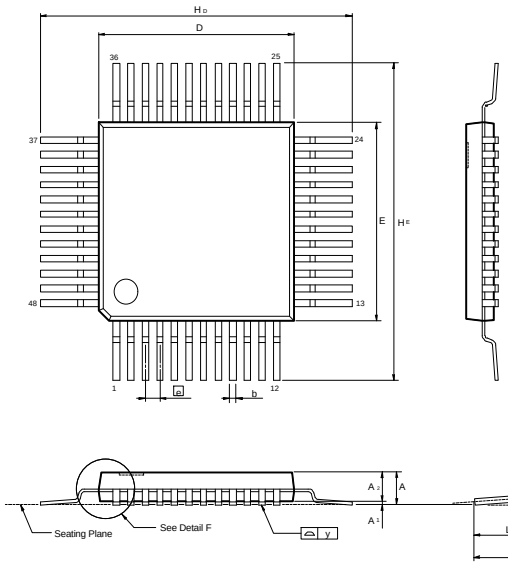
A: assembly house ID; A means ASE, O means OSE

A: IC revision; A means version A, B means version B

02A: for internal use

10. PACKAGE DIMENSIONS

48-pin QFP



Symbol	Dimension in Inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A				---	---	1.60
A_1				0.05	---	0.15
A_2				1.35	1.40	1.45
b				0.17	0.20	0.27
c				0.09	---	0.20
D					7.00	
E					7.00	
e					0.50	
H_D					9.00	
H_E					9.00	
L				0.45	0.60	0.75
L_1					1.00	
y				---	0.08	---
θ				0	3.5°	7

Notes:
1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

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