Winbond Electronics Corp.

200MHZ CLOCK FOR CAMINO CHIPSET

1.0 GENERAL DESCRIPTION

The W83194BR-C is a Clock Synthesizer for Intel Camino 820 chipset. W83194BR-C provides all clocks required for high-speed RISC or CISC microprocessor and also provides 64 different frequencies of CPU, PCI, 3V66, IOAPIC clocks frequency setting. All clocks are externally selectable with smooth transitions.

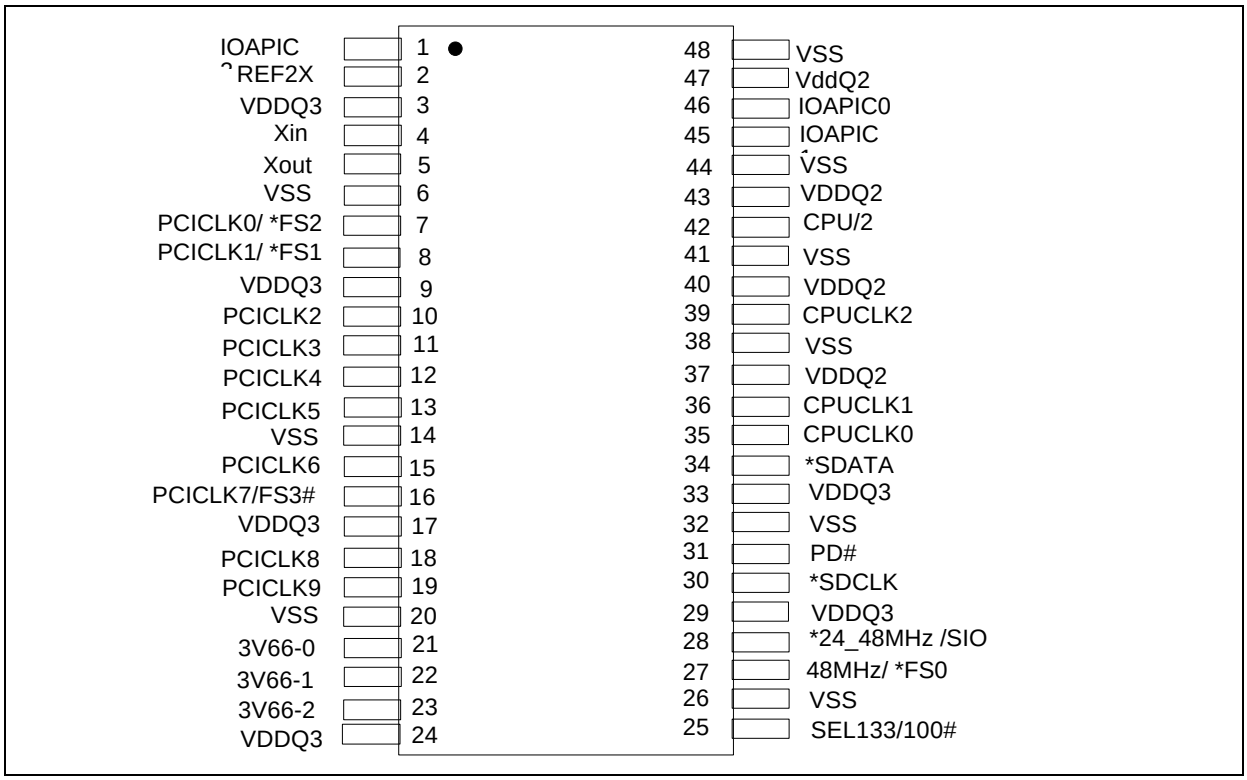
The W83194BR-C provides I^2C serial bus interface to program the registers to enable or disable each clock outputs and provides 0.5% and 0.75% center type spread spectrum to reduce EMI.

The W83194BR-C accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. High drive PCI CLOCK outputs typically provide greater than 1 V /ns slew rate into 30 pF loads. CPU CLOCK outputs typically provide better than 1 V /ns slew rate into 20 pF loads as maintaining 50± 5% duty cycle. The fixed frequency outputs as REF, 24MHz, and 48 MHz provide better than 0.5V /ns slew rate.

2.0 PRODUCT FEATURES

- 2 CPU clock outputs
- One CPU/2 output as reference input to DRCG
- 3 3V66 clock outputs
- 3 IOAPIC clock outputs
- 8 PCI synchronous clocks.
- Optional single or mixed supply:
  (VddQ2 = VddQ3 = 3.3V or VddQ3=3.3V, VddQ2=2.5V)
- CPU to 3V66 offset .0 to 1.5 ns
- 3V66 to PCI offset 1.5 to 4.0 ns
- Skew form CPU to PCI clock 1 to 4 ns, center 2.6 ns
- Smooth frequency switch with selections from 66.8 to 200MHz
- I^2C 2-Wire serial interface and I^2C read back
- 0.5% and 0.75% center type spread spectrum
- Programmable registers to enable/stop each output and select modes
  (mode as Tri-state or Normal)
- 48 MHz pins for USB
- 24 MHz for super I/O
- 48-pin SSOP package

3.0 PIN CONFIGURATION



4.0 PIN DESCRIPTION

IN - Input

OUT - Output

I/O - Bi-directional Pin

- Active Low

* - Internal 250kΩ pull-up

4.1 Crystal I/O

SYMBOL	PIN	I/O	FUNCTION
Xin	4	IN	Crystal input with internal loading capacitors and feedback resistors.
Xout	5	OUT	Crystal output at 14.318MHz nominally.

4.2 CPU, 3V66, PCI, IOAPIC Clock Outputs

SYMBOL	PIN	I/O	FUNCTION
CPUCLK [0:2]	45,44	OUT	Low skew (< 250ps) clock outputs for host frequencies such as CPU and Chipset.
CPU/2	42	O	As a reference signal for DRCG. The voltage is determined by VDDQ2.
PD#	31	IN	Power Down mode when driven low.
SEL133/100#	25	IN	Frequency selection input pin.
PCICLK0/ *FS2	7	I/O	3.3V PCI clock during normal operation. Latched input for FS2 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
PCICLK1/ *FS1	8	I/O	Low skew (< 250ps) PCI clock outputs. Latched input for FS1 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
PCICLK[2,8:9]	10,11,12,13,15 ,18,19	I/O	Low skew (< 250ps) PCI clock outputs.
PCICLK7/ *FS3	16	I/O	Low skew (< 250ps) PCI clock outputs. Latched input for FS3 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
3V66 [0:2]	21, 22, 23	OUT	3.3V output clocks for the chipset.
IOAPIC[0:2]	46, 45, 1	O	Synchronous with CPU clocks, 2.5V.

4.3 I^2C Control Interface

SYMBOL	PIN	I/O	FUNCTION
*SDATA	34	I/O	Serial data of I^2C 2-wire control interface with internal pull-up resistor.
*SDCLK	30	IN	Serial clock of I^2C 2-wire control interface with internal pull-up resistor.

4.4 Fixed Frequency Outputs

SYMBOL	PIN	I/O	FUNCTION
IOAPIC[0:2]	46, 45, 1	O	Synchronous with CPU clocks, 2.5V.
REFX2	2	I/O	14.318MHz reference clock.
24_48MHz/ *SIO	28	I/O	24MHz or 48MHz output clock. Latched input for SIO at initial power up for the output frequency of 24MHz(HIGH) and 48MHz(LOW) clocks.
48MHz/ FS0*	27	I/O	48MHz / Latched input for FS0 at initial power up for H/W selecting the output frequency.

4.5 Power Pins

SYMBOL	PIN	FUNCTION
VddQ2	37,40,43,47	Power supply for CPU & IOAPIC, 2.5V
VddQ3	3,9,17,24,29,33	Power supply for PCI,3V66,REF2X,48MHz output,3.3V.
Vss	6,14,20,26,32,38,41, 44,48	Circuit Ground.

5.0 Frequency Selection by Hardware

FS4	FS3	FS2	FS1	FS0	CPU(MHz)	CPU/2	3V66/CPU	3V66(MHz)	PCI(MHz)	IOAPIC (MHz)
0	0	0	0	0	133.90	66.95	0.50	66.95	33.48	16.74
0	0	0	0	1	128.50	64.25	0.50	64.25	32.13	16.06
0	0	0	1	0	124.00	62.00	0.67	82.67	41.34	20.67
0	0	0	1	1	66.80	33.40	1.00	66.80	33.40	16.70
0	0	1	0	0	120.00	60.00	0.67	80.00	40.00	20.00
0	0	1	0	1	114.00	57.00	0.67	76.00	38.00	19.00
0	0	1	1	0	105.00	52.50	0.67	70.00	35.00	17.50
0	0	1	1	1	100.20	50.10	0.67	66.80	33.40	16.70
0	1	0	0	0	160.00	80.00	0.50	80.00	40.00	20.00
0	1	0	0	1	155.00	77.50	0.50	77.50	38.75	19.38
0	1	0	1	0	152.50	76.25	0.50	76.25	38.13	19.06
0	1	0	1	1	150.00	75.00	0.50	75.00	37.50	18.75
0	1	1	0	0	148.00	74.00	0.50	74.00	37.00	18.50
0	1	1	0	1	143.00	71.50	0.50	71.50	35.75	17.88
0	1	1	1	0	138.00	69.00	0.50	69.00	34.50	17.25
0	**1**	**1**	**1**	**1**	**133.30**	**66.65**	0.50	**66.65**	**33.33**	**16.66**
1	0	0	0	0	100.90	50.45	0.50	50.45	25.23	12.61
1	0	0	0	1	109.00	54.50	0.67	72.67	36.34	18.17
1	0	0	1	0	116.00	58.00	0.67	77.34	38.67	19.33
1	0	0	1	1	122.00	61.00	0.50	61.00	30.50	15.25
1	0	1	0	0	126.00	63.00	0.50	63.00	31.50	15.75
1	0	1	0	1	130.00	65.00	0.50	65.00	32.50	16.25
1	0	1	1	0	135.00	67.50	0.50	67.50	33.75	16.88
1	0	1	1	1	140.00	70.00	0.50	70.00	35.00	17.50
1	1	0	0	0	145.00	72.50	0.50	72.50	36.25	18.13
1	1	0	0	1	159.00	79.50	0.50	79.50	39.75	19.88
1	1	0	1	0	162.00	81.00	0.50	81.00	40.50	20.25
1	1	0	1	1	165.00	82.50	0.50	82.50	41.25	20.63
1	1	1	0	0	168.00	84.00	0.50	84.00	42.00	21.00
1	1	1	0	1	171.00	85.50	0.50	85.50	42.75	21.38
1	1	1	1	0	174.00	87.00	0.50	87.00	43.50	21.75
1	1	1	1	1	180.00	90.00	0.50	90.00	45.00	22.50

6.0 SERIAL CONTROL REGISTERS

The Pin column lists the affected pin number and the @PowerUp column gives the state at true power up. Registers are set to the values shown only on true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the below described sequence (Register 0, Register 1, Register 2, ...) will be valid and acknowledged.

Frequency Selection BY I2C

SSEL5	SSEL4	SSEL3	SSEL2	SSEL1	SSEL0	CPU (MHz)	CPU/2	3V66 (MHz)	PCI (MHz)	IOAPIC (MHz)
0	0	0	0	0	0	133.90	66.95	66.95	33.48	16.74
0	0	0	0	0	1	128.50	64.25	64.25	32.13	16.06
0	0	0	0	1	0	124.00	62.00	82.67	41.34	20.67
0	0	0	0	1	1	66.80	33.40	66.80	33.40	16.70
0	0	0	1	0	0	120.00	60.00	80.00	40.00	20.00
0	0	0	1	0	1	114.00	57.00	76.00	38.00	19.00
0	0	0	1	1	0	105.00	52.50	70.00	35.00	17.50
0	0	0	1	1	1	100.20	50.10	66.80	33.40	16.70
0	0	1	0	0	0	160.00	80.00	80.00	40.00	20.00
0	0	1	0	0	1	155.00	77.50	77.50	38.75	19.38
0	0	1	0	1	0	152.50	76.25	76.25	38.13	19.06
0	0	1	0	1	1	150.00	75.00	75.00	37.50	18.75
0	0	1	1	0	0	148.00	74.00	74.00	37.00	18.50
0	0	1	1	0	1	143.00	71.50	71.50	35.75	17.88
0	0	1	1	1	0	138.00	69.00	69.00	34.50	17.25
0	**0**	**1**	**1**	**1**	**1**	**133.30**	**66.65**	**66.65**	**33.33**	**16.66**
0	1	0	0	0	0	100.90	50.45	50.45	25.23	12.61
0	1	0	0	0	1	109.00	54.50	72.67	36.34	18.17
0	1	0	0	1	0	116.00	58.00	77.34	38.67	19.33
0	1	0	0	1	1	122.00	61.00	61.00	30.50	15.25
0	1	0	1	0	0	126.00	63.00	63.00	31.50	15.75
0	1	0	1	0	1	130.00	65.00	65.00	32.50	16.25
0	1	0	1	1	0	135.00	67.50	67.50	33.75	16.88
0	1	0	1	1	1	140.00	70.00	70.00	35.00	17.50
0	1	1	0	0	0	145.00	72.50	72.50	36.25	18.13
0	1	1	0	0	1	159.00	79.50	79.50	39.75	19.88
0	1	1	0	1	0	162.00	81.00	81.00	40.50	20.25
0	1	1	0	1	1	165.00	82.50	82.50	41.25	20.63
0	1	1	1	0	0	168.00	84.00	84.00	42.00	21.00
0	1	1	1	0	1	171.00	85.50	85.50	42.75	21.38
0	1	1	1	1	0	174.00	87.00	87.00	43.50	21.75
0	1	1	1	1	1	180.00	90.00	90.00	45.00	22.50

SSEL5	SSEL4	SSEL3	SSEL2	SSEL1	SSEL0	CPU (MHz)	CPU/2	3V66 (MHz)	PCI (MHz)	IOAPIC (MHz)
1	0	0	0	0	0	134.00	67.00	67.00	33.50	16.75
1	0	0	0	0	1	135.00	67.50	67.50	33.75	16.88
1	0	0	0	1	0	136.00	68.00	68.00	34.00	17.00
1	0	0	0	1	1	137.00	68.50	68.50	34.25	17.13
1	0	0	1	0	0	139.00	69.50	69.50	34.75	17.38
1	0	0	1	0	1	141.00	70.50	70.50	35.25	17.63
1	0	0	1	1	0	142.00	71.00	71.00	35.50	17.75
1	0	0	1	1	1	144.00	72.00	72.00	36.00	18.00
1	0	1	0	0	0	146.00	73.00	73.00	36.50	18.25
1	0	1	0	0	1	147.00	73.50	73.50	36.75	18.38
1	0	1	0	1	0	149.00	74.50	74.50	37.25	18.63
1	0	1	0	1	1	151.00	75.50	75.50	37.75	18.88
1	0	1	1	0	0	152.00	76.00	76.00	38.00	19.00
1	0	1	1	0	1	153.00	76.50	76.50	38.25	19.13
1	0	1	1	1	0	154.00	77.00	77.00	38.50	19.25
1	0	1	1	1	1	157.00	78.50	78.50	39.25	19.63
1	1	0	0	0	0	158.00	79.00	79.00	39.50	19.75
1	1	0	0	0	1	161.00	80.50	80.50	40.25	20.13
1	1	0	0	1	0	163.00	81.50	81.50	40.75	20.38
1	1	0	0	1	1	164.00	82.00	82.00	41.00	20.50
1	1	0	1	0	0	166.00	83.00	83.00	41.50	20.75
1	1	0	1	0	1	167.00	83.50	83.50	41.75	20.88
1	1	0	1	1	0	169.00	84.50	84.50	42.25	21.13
1	1	0	1	1	1	170.00	85.00	85.00	42.50	21.25
1	1	1	0	0	0	172.00	86.00	86.00	43.00	21.50
1	1	1	0	0	1	173.00	86.50	86.50	43.25	21.63
1	1	1	0	1	0	175.00	87.50	87.50	43.75	21.88
1	1	1	0	1	1	181.00	90.50	90.50	45.25	22.63
1	1	1	1	0	0	183.00	91.50	91.50	45.75	22.88
1	1	1	1	0	1	185.00	92.50	92.50	46.25	23.13
1	1	1	1	1	0	190.00	95.00	95.00	47.50	23.75
1	1	1	1	1	1	200.00	100.00	100.00	50.00	25.00

6.1 Register 0: CPU Frequency Select Register

Bit	@PowerUp	Pin	Description
7	0	-	SSEL3 (Frequency table selection by software via I^2C)
6	0	-	SSEL2 (Frequency table selection by software via I^2C)
5	0	-	SSEL1 (Frequency table selection by software via I^2C)
4	0	-	SSEL0 (Frequency table selection by software via I^2C)
3	0	-	0 = Selection by hardware 1 = Selection by software I^2C - Bit (1,2, 6:4)
2	0	-	SSEL4 (Frequency table selection by software via I^2C)
1	0	-	SSEL5 (Frequency table selection by software via I^2C)
0	0	-	0 = Normal 1 = Spread Spectrum enabled

6.2 Register 1 : CPU Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	27	48MHz(Active / Inactive)
6	1	28	24_48MHz(Active / Inactive)
5	0	-	0 = ±0.25% Center type Spread Spectrum Modulation 1 =±0.5% Center type Spread Spectrum Modulation
4	1	42	CPU/2(Active / Inactive)
3	0	-	0 = Running 1 = Tristate all outputs
2	1	39	CPUCLK2(Active / Inactive)
1	1	36	CPUCLK1(Active / Inactive)
0	1	35	CPUCLK0(Active / Inactive)

6.3 Register 2: PCI Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	1	16	PCICLK7 (Active / Inactive)
6	1	15	PCICLK6 (Active / Inactive)
5	1	13	PCICLK5 (Active / Inactive)
4	1	12	PCICLK4 (Active / Inactive)
3	1	11	PCICLK3 (Active / Inactive)
2	1	10	PCICLK2 (Active / Inactive)
1	1	8	PCICLK1 (Active / Inactive)
0	1	7	PCICLK0 (Active / Inactive)

6.4 Register 3: 3V66 Clock Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	0	-	Reserve
6	1	23	3V66_2(Active / Inactive)
5	1	22	3V66_1(Active / Inactive)
4	1	21	3V66_0(Active / Inactive)
3	0	-	Reserve
2	0	-	Reserve
1	1	19	PCICLK9 (Active / Inactive)
0	1	18	PCICLK8 (Active / Inactive)

6.5 Register 4: PCI Clock Additional Register (1 = Active, 0 = Inactive)

Bit	@PowerUp	Pin	Description
7	0	-	0 = Center type Spread Spectrum Modulation 1 =0~0.5% Down type Spread Spectrum (Override register bit5)
6	1	1	IOAPIC2 (Active / Inactive)
5	1	45	IOAPIC1 (Active / Inactive)
4	1	46	IOAPIC0 (Active / Inactive)
3	0	-	Reserve
2	0	-	Reserve
1	0	-	Reserve
0	1	2	REF2X (Active / Inactive)

6.6 Register 5: Skew Register

Bit	@PowerUp	Pin	Description
7	**1**	**-**	**Skew2 (CPU to 3V66 skew program bit)**
6	**0**	**-**	**Skew1 (CPU to 3V66 skew program bit)**
5	**0**	**-**	**Skew0 (CPU to 3V66 skew program bit)**
4	**X**	**-**	**FS3#**
3	**X**	**-**	**SEL133/100#**
2	**X**	**-**	**FS2#**
1	**X**	**-**	**FS1#**
0	**X**	**-**	**FS0#**

6.7 Register 6: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	1	-	Winbond Chip ID
6	0	-	Winbond Chip ID
5	0	-	Winbond Chip ID
4	1	-	Winbond Chip ID
3	0	-	Winbond Chip ID
2	0	-	Winbond Chip ID
1	0	-	Winbond Chip ID
0	0	-	Winbond Chip ID

5.8 Register 7: Winbond Chip ID Register (Read Only)

Bit	@PowerUp	Pin	Description
7	0	-	Winbond Chip ID
6	0	-	Winbond Chip ID
5	0	-	Winbond Chip ID
4	1	-	Winbond Chip ID
3	**0**	-	Winbond Version ID
2	**0**	-	Winbond Version ID
1	**0**	-	Winbond Version ID
0	**1**	-	Winbond Version ID

6.9 Register 8: Watchdog Timer Register

Bit	@PowerUp	Pin	Description
7	0	-	Enable Count 1 = start timer 0 = stop timer
6	0	-	Second timeout status (READ ONLY)
5	0	-	Second count 5
4	0	-	Second count 4
3	0	-	Second count 3
2	0	-	Second count 2
1	0	-	Second count 1
0	0	-	Second count 0

6.10 Register 9: M/N Program Register and 3V66 Divisor

Bit	@PowerUp	Pin	Description
7	0	-	N value bit 8
6	0	-	3V66 divisor 00: CPU/2 ; 01: CPU/1.5
5	0	-	3V66 divisor 10: CPU/1 ; 11: CPU/3
4	0	-	M value bit 4
3	0	-	M value bit 3
2	0	-	M value bit 2
1	0	-	M value bit 1
0	0	-	M value bit 0

6.11 Register 10: M/N Program Register

Bit	@PowerUp	Pin	Description
7	0	-	N value bit 7
6	0	-	N value bit 6
5	0	-	N value bit 5
4	0	-	N value bit 4
3	0	-	N value bit 3
2	0	-	N value bit 2
1	0	-	N value bit 1
0	0	-	N value bit 0

6.12 Register 11: Divisor Register

Bit	@PowerUp	Pin	Description
7	1	-	Spread spectrum up count[0:3]
6	1	-	Spread spectrum up count[0:3]
5	1	-	Spread spectrum up count[0:3]
4	1	-	Spread spectrum up count[0:3]
3	1	-	Spread spectrum down count[0:3]
2	1	-	Spread spectrum down count[0:3]
1	1	-	Spread spectrum down count[0:3]
0	1	-	Spread spectrum down count[0:3]

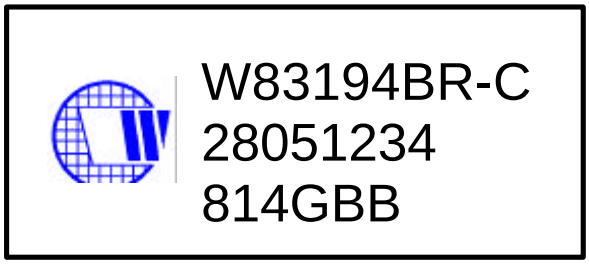
6.12 Register 12 Divisor Register

Bit	@PowerUp	Pin	Description
7	0	-	0: use frequency table 1: use M/N register 9~12 to program frequency **Freq. = 14.318MHz * (N+4)/ 2*M**
6	1	-	Reserve
5	1	-	Reserve
4	1	-	Reserve
3	1	-	Reserve
2	1	-	Reserve
1	1	-	Reserve
0	1	-	Reserve

7.0 ORDERING INFORMATION

Part Number	Package Type	Production Flow
W83194BR-C	48 PIN SSOP	Commercial, 0°C to +70°C

8.0 HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83194BR-C

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 814 G B B

814: packages made in '98, week 14

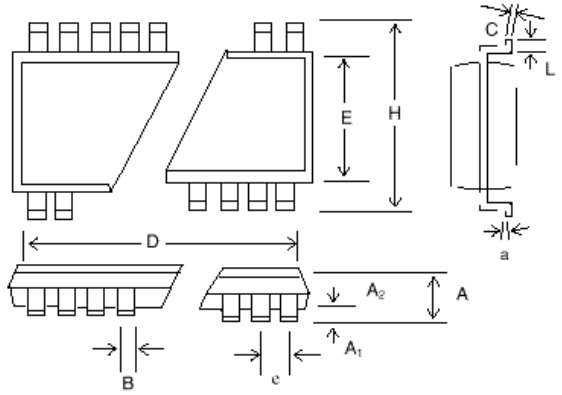
G: assembly house ID; A means ASE, S means SPIL, G means GR

B: Winbond internal use code

B: IC revision

All the trade marks of products and companies mentioned in this data sheet belong to their respective owners.

9.0 PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0°	5°	8°	0°	5°	8°

Winbond Electronics Corp.

Headquarters
No. 4, Creation Rd. III
Science-Based Industrial Park
Hsinchu, Taiwan
TEL: 886-35-770066
FAX: 886-35-789467
www: http://www.winbond.com.tw/

Taipei Office
11F, No. 115, Sec. 3, Min-Sheng East Rd.
Taipei, Taiwan
TEL: 886-2-7190505
FAX: 886-2-7197502
TLX: 16485 WINTPE

Winbond Electronics (H.K.) Ltd.
Rm. 803, World Trade Square, Tower II
123 Hoi Bun Rd., Kwun Tong
Kowloon, Hong Kong
TEL: 852-27516023-7
FAX: 852-27552064

Winbond Electronics (North America) Corp.
2730 Orchard Parkway
San Jose, CA 95134 U.S.A.
TEL: 1-408-9436666
FAX: 1-408-9436668

Please note that all data and specifications are subject to change without notice. All the trade marks of products and companies mentioned in this data sheet belong to their respective owners.

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sale.