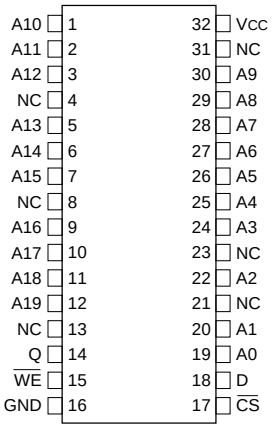
1Mx1 SRAM MONOLITHIC *ADVANCED**

PIN CONFIGURATION
TOP VIEW



PIN DESCRIPTION

A_{0-19}	Address Inputs
D,Q	Data Input, Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

FEATURES

- Access Times 20, 25, 35ns
- MIL-STD-883 Compliant Devices Available
- Packaging
  - 32 lead, Ceramic SOJ (Package 101)
- Commercial, Industrial and Military Temperature Ranges
- Organized as 1M x 1
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- 2V Data Retention Devices also Available for Battery Back-Up Operation

* *This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.*

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	Vcc+0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	I/O Pin	Cycle	Current
H	X	Not Selected	High-Z	—	I_{SB1}, I_{SB2}
L	H	Read	D_{OUT}	Read	I_{CCA}
L	L	Write	High-Z	Write	I_{CCA}

H = High, L = Low, X = Don't Care

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C_{IN}	V_{IN} = 0V, f = 1.0MHz	15	pF
Output capicitance	C_{OUT}	V_{OUT} = 0V, f = 1.0MHz	15	pF

This parameter is guaranteed by design but not tested.

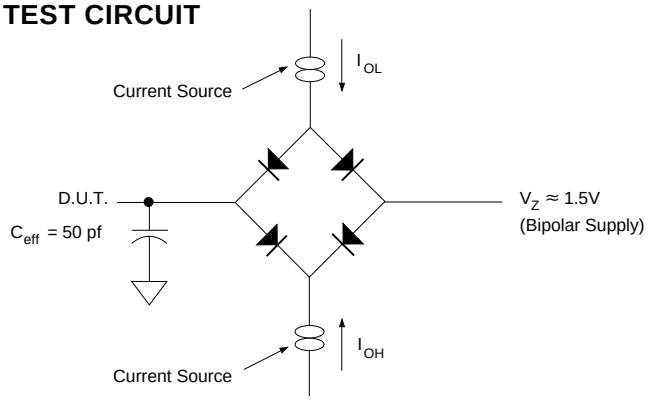
DC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		105	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz		30	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA, V_{CC} = 4.5		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, V_{CC} = 4.5	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

AC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

Parameter Read Cycle	Symbol	-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	20		25		35		ns
Address Access Time	t_{AA}		20		25		35	ns
Output Hold from Address Change	t_{OH}	0		5		5		ns
Chip Select Access Time	t_{ACS}		20		25		35	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	5		5		5		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		9		10		12	ns

1. This parameter is guaranteed by design but not tested.

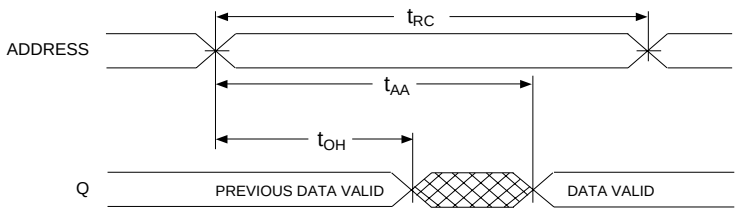
AC CHARACTERISTICS

(V_{CC} = 5.0V, GND = 0V, T_A = -55°C to +125°C)

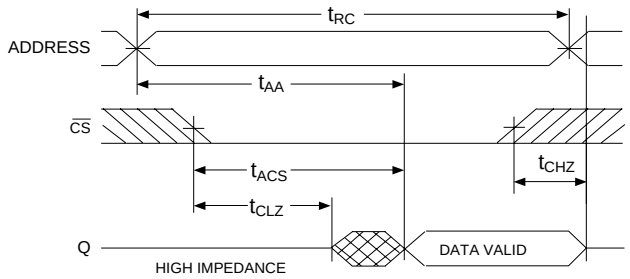
Parameter Write Cycle	Symbol	-20		-25		-35		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	20		25		35		ns
Chip Select to End of Write	t_{CW}	15		20		25		ns
Address Valid to End of Write	t_{AW}	15		20		25		ns
Data Valid to End of Write	t_{DW}	12		15		20		ns
Write Pulse Width	t_{WP}	15		20		25		ns
Address Setup Time	t_{AS}	2		2		2		ns
Address Hold Time	t_{AH}	0		0		0		ns
Output Active from End of Write	t_{OW}[1]	5		5		5		ns
Write Enable to Output in High Z	t_{WHZ}[1]	0	9	0	10	0	12	ns
Data Hold Time	t_{DH}	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM - READ CYCLE

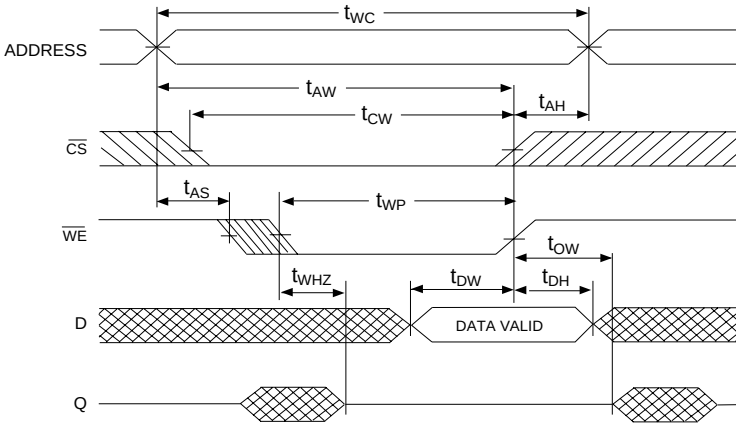


READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



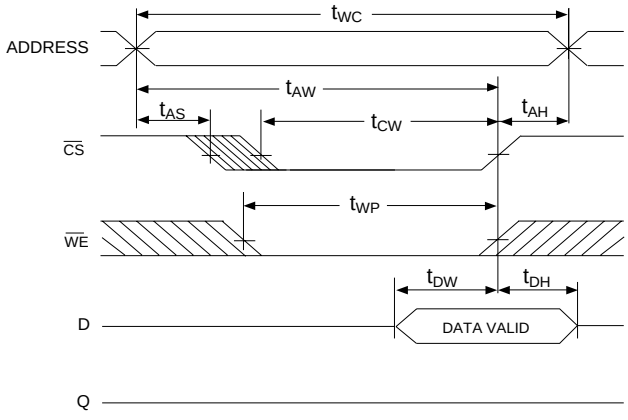
READ CYCLE 2 ($\overline{WE}$ = V_{IH})

WRITE CYCLE - $\overline{WE}$ CONTROLLED



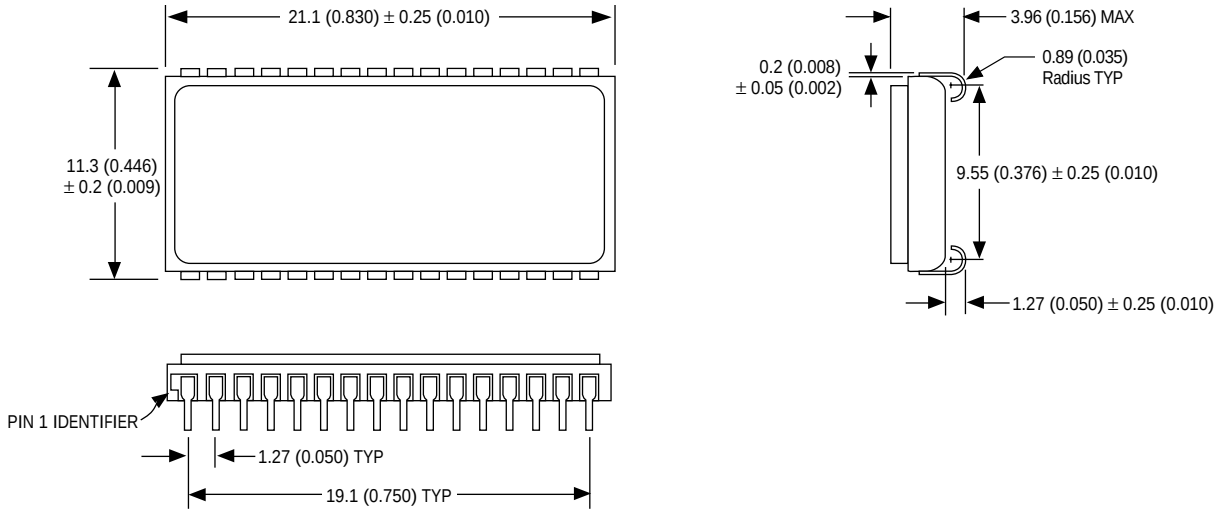
WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

WRITE CYCLE - $\overline{CS}$ CONTROLLED



WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

PACKAGE 101: 32 LEAD, CERAMIC SOJ



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W M S 1M 1 - XXX DE X X

LEAD FINISH:
- Blank = Gold plated leads
- A = Solder dip leads

DEVICE GRADE:

M = Military Screened	-55°C to +125°C
I = Industrial	-40°C to +85°C
C = Commercial	0°C to +70°C

PACKAGE:
- DE = 32 Lead Ceramic SOJ (Package 101)

ACCESS TIME (ns)

ORGANIZATION, 1M x 1

SRAM

MONOLITHIC

WHITE MICROELECTRONICS