512Kx32 SRAM 3.3V MODULE *ADVANCED**

FEATURES

- Access Times of 70, 85, 100, 120ns
- Packaging
  - 66-pin, PGA Type, 1.185 inch square, Hermetic Ceramic HIP (Package 401)
  - 68 lead, Hermetic CQFP (G2T), 22.4mm (0.880 inch) square 4.57mm (0.180 inch) high (Package 509). Designed to fit JEDEC 68 lead 0.990" CQFJ footprint.
- Organized as 512Kx32, User Configurable as 1024Kx16 or 2Mx8
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- Low Voltage
  - 3.3V ±10% Power Supply
- Low Power CMOS
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
  WS512K32V-XG2TX - 8 grams typical
  WS512K32V-XHX - 13 grams typical

* *This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.*

FIG. 1 PIN CONFIGURATION FOR WS512K32V-XHX

TOP VIEW

1	12	23	34	45	56
I/O8	$\overline{WE_2}$	I/O15	I/O24	VCC	I/O31
I/O9	$\overline{CS_2}$	I/O14	I/O25	$\overline{CS_4}$	I/O30
I/O10	GND	I/O13	I/O26	$\overline{WE_4}$	I/O29
A13	I/O11	I/O12	A6	I/O27	I/O28
A14	A10	$\overline{OE}$	A7	A3	A0
A15	A11	A18	NC	A4	A1
A16	A12	$\overline{WE_1}$	A8	A5	A2
A17	VCC	I/O7	A9	$\overline{WE_3}$	I/O23
I/O0	$\overline{CS_1}$	I/O6	I/O16	$\overline{CS_3}$	I/O22
I/O1	NC	I/O5	I/O17	GND	I/O21
I/O2	I/O3	I/O4	I/O18	I/O19	I/O20
11	22	33	44	55	66

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
~~Vcc~~	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

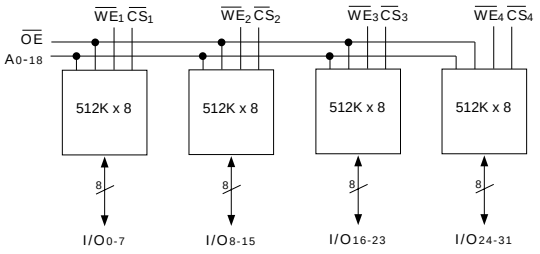
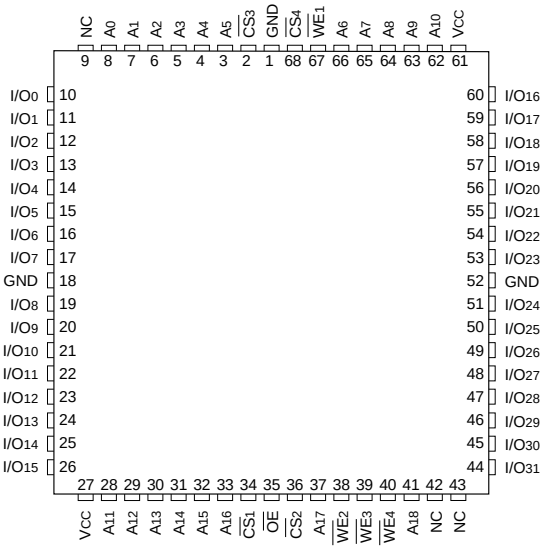
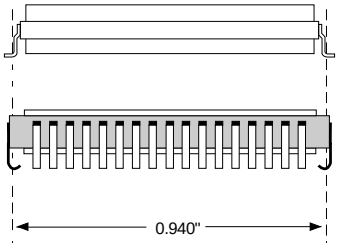


FIG. 2 PIN CONFIGURATION FOR WS512K32V-XG2TX

TOP VIEW



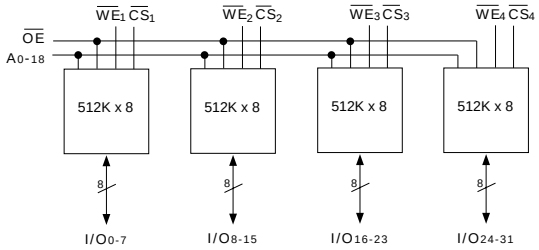


The WEDC 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
WE1-4	Write Enables
CS1-4	Chip Selects
OE	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	Vcc+0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	4.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp (Mil)	T_A	-55	+125	°C

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Out Disable	High Z	Active
L	X	L	Write	Data In	Active

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ Capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}$ Capacitance HIP (PGA)	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
$\overline{WE}$ Capacitance CQFP G2T	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	15	pF
$\overline{CS}$ Capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O Capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	20	pF
Address Input Capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 3.3V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = 3.6, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current x 32 Mode	$I_{CC \times 32}$	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 3.6		100	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 3.6		2.0	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA, V_{CC} = 3.0		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA, V_{CC} = 3.0	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

AC CHARACTERISTICS

(V_{CC} = 3.3V, V_{SS} =0V, T_A = -55°C to +125°C)

Parameter Read Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	70		85		100		120		ns
Address Access Time	t_{AA}		70		85		100		120	ns
Output Hold from Address Change	t_{OH}	5		5		5		5		ns
Chip Select Access Time	t_{ACS}		70		85		100		120	ns
Output Enable to Output Valid	t_{OE}		35		40		50		60	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	10		10		10		10		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	5		5		5		5		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		25		25		35		35	ns
Output Disable to Output in High Z	t_{OHZ}[1]		25		25		35		35	ns

1. This parameter is guaranteed by design but not tested.

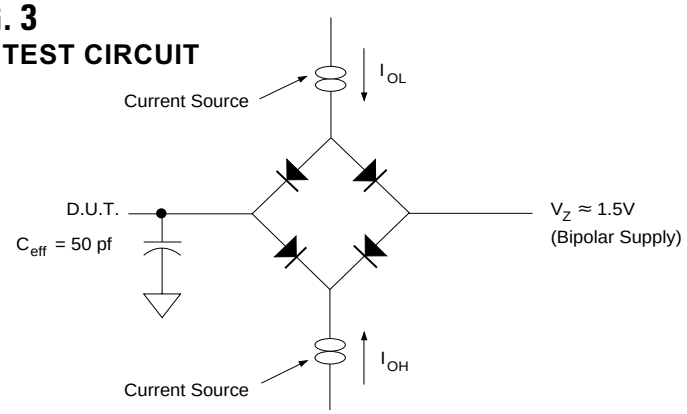
AC CHARACTERISTICS

(V_{CC} = 3.3V, V_{SS} =0V, T_A = -55°C to +125°C)

Parameter Write Cycle	Symbol	-70		-85		-100		-120		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	70		85		100		120		ns
Chip Select to End of Write	t_{CW}	60		75		80		100		ns
Address Valid to End of Write	t_{AW}	60		75		80		100		ns
Data Valid to End of Write	t_{DW}	30		30		40		40		ns
Write Pulse Width	t_{WP}	50		50		60		60		ns
Address Setup Time	t_{AS}	0		0		0		0		ns
Address Hold Time	t_{AH}	5		5		5		5		ns
Output Active from End of Write	t_{OW}[1]	5		5		5		5		ns
Write Enable to Output in High Z	t_{WHZ}[1]		25		25		35		35	ns
Data Hold from Write Time	t_{DH}	0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

FIG. 3
AC TEST CIRCUIT

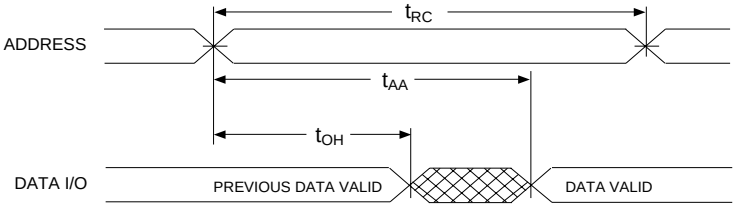


AC TEST CONDITIONS

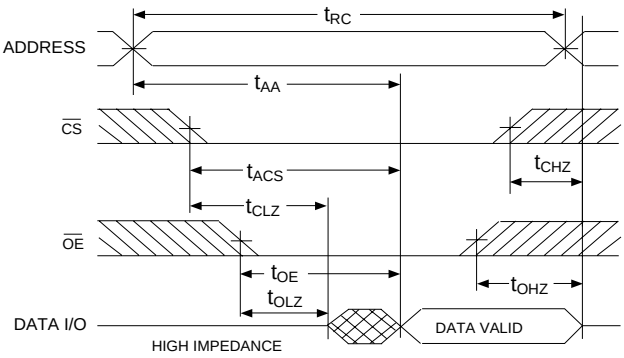
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

FIG. 4
TIMING WAVEFORM - READ CYCLE

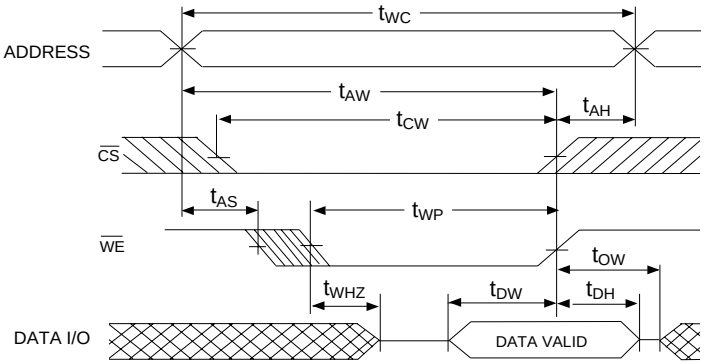


READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



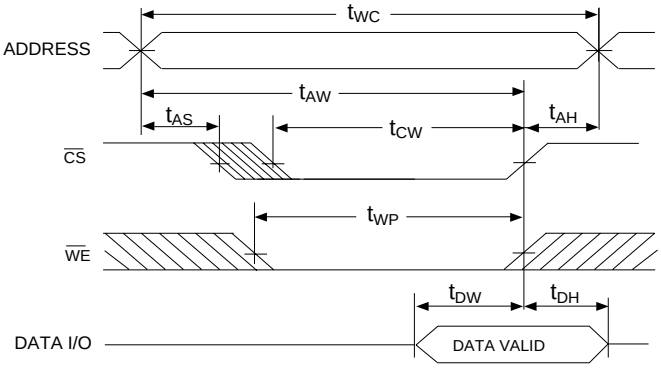
READ CYCLE 2 ($\overline{WE}$ = V_{IH})

FIG. 5
WRITE CYCLE - $\overline{WE}$ CONTROLLED



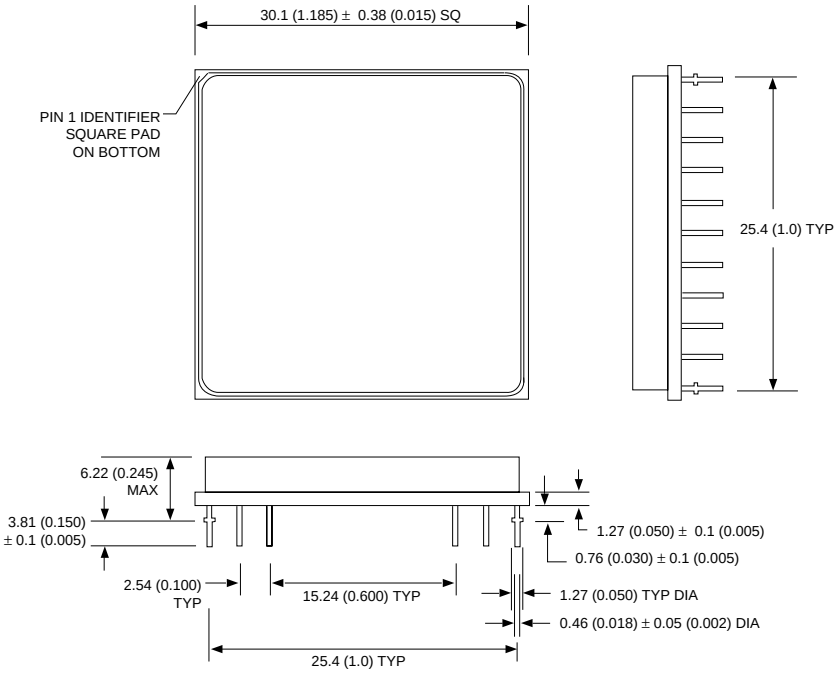
WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

FIG. 6
WRITE CYCLE - $\overline{CS}$ CONTROLLED



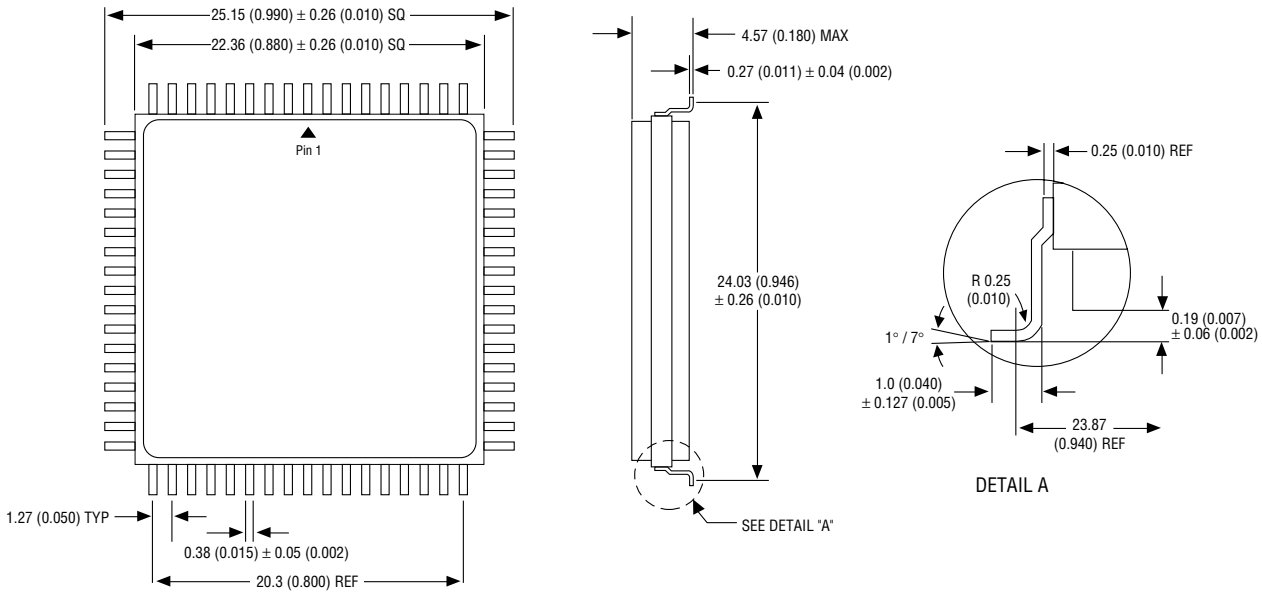
WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

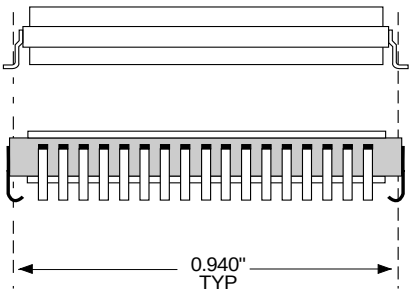
PACKAGE 401: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 509: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2T)





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ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W S 512K 32 X V - XXX X X X

LEAD FINISH:
Blank = Gold plated leads
A = Solder dip leads

DEVICE GRADE:
Q = MIL-STD-883 Compliant
M = Military Screened -55°C to +125°C
I = Industrial -40°C to 85°C
C = Commercial 0°C to +70°C

PACKAGE TYPE:
H = Ceramic Hex-In-line Package, HIP (Package 401)
G2T = 22.4mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 509)

ACCESS TIME (ns)

Low Voltage Supply 3.3V ± 10%

IMPROVEMENT MARK:
N = No Connect at pin 21 and 39 in HIP for Upgrades

ORGANIZATION, 512Kx32
User configurable as 1Mx16 or 2Mx8

SRAM

WHITE ELECTRONIC DESIGNS CORP.