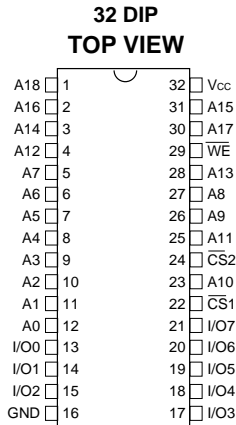




# 2x512Kx8 DUALITHIC™ SRAM PRELIMINARY\*

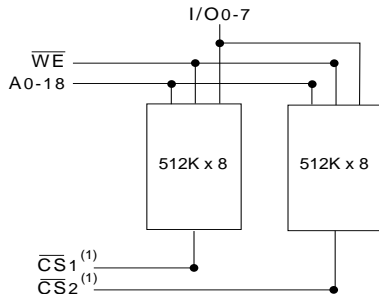
## PIN CONFIGURATION FOR WS1M8-XCX



## PIN DESCRIPTION

A0-18	Address Inputs
I/O0-7	Data Input/Output
$\overline{CS}1-2$	Chip Selects
$\overline{WE}$	Write Enable
Vcc	+5.0V Power
GND	Ground

## BLOCK DIAGRAM



### NOTE:

1.  $\overline{CS}1$  and  $\overline{CS}2$  are used to select the lower and upper 512Kx8 of the device.  $\overline{CS}1$  and  $\overline{CS}2$  must not be enabled at the same time.

## FEATURES

- Access Times 70, 85, 100ns
- Evolutionary, Corner Power/Ground Pinout
- Packaging:
  - 32 pin, Hermetic Ceramic DIP (Package 300)
- Organized as two banks of 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Output Enable Internally tied to GND.

\* This data sheet describes a product under development, not fully characterized, and is subject to change without notice.

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T <sub>A</sub>	-55	+125	°C
Storage Temperature	T <sub>STG</sub>	-65	+150	°C
Signal Voltage Relative to GND	V <sub>G</sub>	-0.5	V <sub>CC</sub> +0.5	V
Junction Temperature	T <sub>J</sub>		150	°C
Supply Voltage	V <sub>CC</sub>	-0.5	7.0	V

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.5	V
Input High Voltage	V <sub>IH</sub>	2.2	V <sub>CC</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.3	+0.8	V
Operating Temp. (Mil.)	T <sub>A</sub>	-55	+125	°C

**TRUTH TABLE**

$\overline{CS}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	Standby	High Z	Standby
L	H	Read	Data Out	Active
L	L	Write	Data In	Active

NOTE:  $\overline{OE}$  is internally tied to GND.**CAPACITANCE**(T<sub>A</sub> = +25°C)

Parameter	Symbol	Condition	Max	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V, f = 1.0MHz	28	pF
Output capacitance	C <sub>OUT</sub>	V <sub>OUT</sub> = 0V, f = 1.0MHz	28	pF

This parameter is guaranteed by design but not tested.

**DC CHARACTERISTICS**(V<sub>CC</sub> = 5.0V, GND = 0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Sym	Conditions	Units		
			Min	Max	
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>		10	μA
Output Leakage Current	I <sub>LO</sub> <sup>1</sup>	$\overline{CS}$ = V <sub>IH</sub> , V <sub>OUT</sub> = GND to V <sub>CC</sub>		10	μA
Operating Supply Current	I <sub>CC</sub> <sup>1</sup>	$\overline{CS}$ = V <sub>IL</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		55	mA
Standby Current	I <sub>SB</sub> <sup>1</sup>	$\overline{CS}$ = V <sub>IH</sub> , f = 5MHz, V <sub>CC</sub> = 5.5		2	mA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.1mA		0.4	V
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0mA	2.4		V

NOTE: DC test conditions: V<sub>IH</sub> = V<sub>CC</sub> - 0.3V, V<sub>IL</sub> = 0.3V1.  $\overline{OE}$  is internally tied to GND.**DATA RETENTION CHARACTERISTICS**(T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol	Conditions	Units			
			Min	Typ	Max	
Data Retention Supply Voltage	V <sub>DR</sub>	$\overline{CS} \geq V_{CC} - 0.2V$	2.0		5.5	V
Data Retention Current	I <sub>CCDR1</sub>	V <sub>CC</sub> = 3V		150	800*	μA

\* Also available in Low Power version. Please call factory for information.



### AC CHARACTERISTICS

(V<sub>CC</sub> = 5.0V, GND = 0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol	-70		-85		-100		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle								
Read Cycle Time	t <sub>RC</sub>	70		85		100		ns
Address Access Time	t <sub>AA</sub>		70		85		100	ns
Output Hold from Address Change	t <sub>OH</sub>	5		5		5		ns
Chip Select Access Time	t <sub>ACS</sub>		70		85		100	ns
Chip Select to Output in Low Z	t <sub>CLZ</sub> <sup>1</sup>	5		5		5		ns
Chip Disable to Output in High Z	t <sub>CHZ</sub> <sup>1</sup>		25		25		25	ns

1. This parameter is guaranteed by design but not tested.

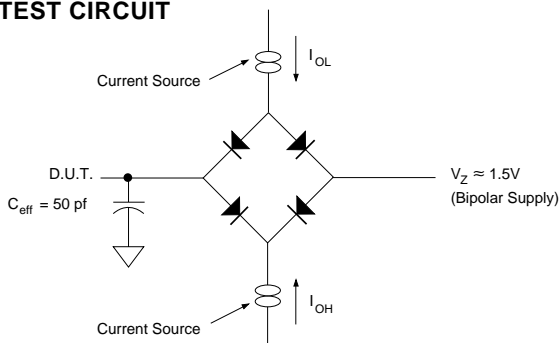
### AC CHARACTERISTICS

(V<sub>CC</sub> = 5.0V, GND = 0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol	-70		-85		-100		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle								
Write Cycle Time	t <sub>WC</sub>	70		85		100		ns
Chip Select to End of Write	t <sub>CW</sub>	60		75		80		ns
Address Valid to End of Write	t <sub>AW</sub>	60		75		80		ns
Data Valid to End of Write	t <sub>DW</sub>	30		30		40		ns
Write Pulse Width	t <sub>WP</sub>	50		50		60		ns
Address Setup Time	t <sub>AS</sub>	0		0		0		ns
Address Hold Time	t <sub>AH</sub>	5		5		5		ns
Output Active from End of Write	t <sub>OW</sub> <sup>1</sup>	5		5		5		ns
Write Enable to Output in High Z	t <sub>WHZ</sub> <sup>1</sup>		25		25		35	ns
Data Hold Time	t <sub>DH</sub>	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

### AC TEST CIRCUIT



### AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V <sub>IL</sub> = 0, V <sub>IH</sub> = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

#### NOTES:

V<sub>Z</sub> is programmable from -2V to +7V.

I<sub>OL</sub> & I<sub>OH</sub> programmable from 0 to 16mA.

Tester Impedance Z<sub>0</sub> = 75 Ω.

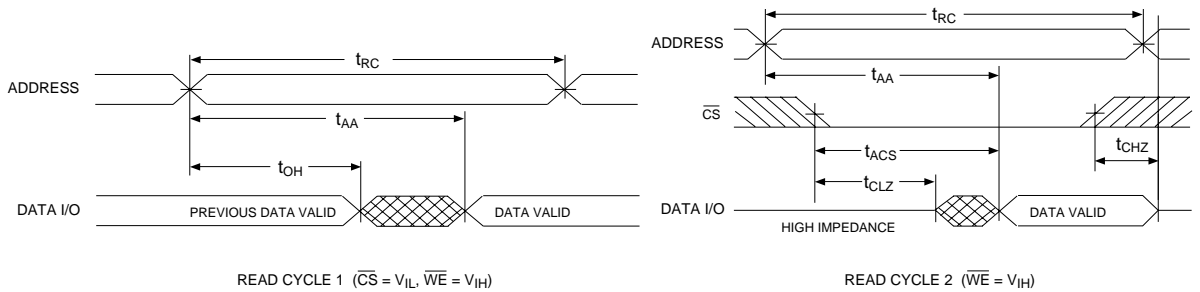
V<sub>Z</sub> is typically the midpoint of V<sub>OH</sub> and V<sub>OL</sub>.

I<sub>OL</sub> & I<sub>OH</sub> are adjusted to simulate a typical resistive load circuit.

ATE tester includes jig capacitance.

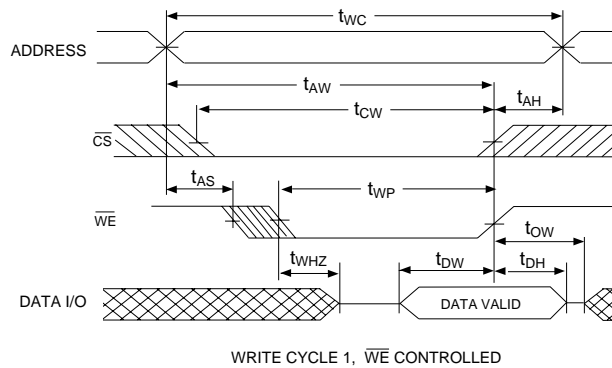


**TIMING WAVEFORM - READ CYCLE**

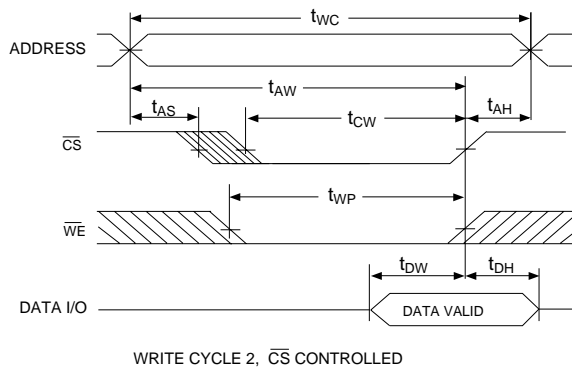


NOTE:  $\overline{OE}$  is internally tied to GND.

**WRITE CYCLE -  $\overline{WE}$  CONTROLLED**

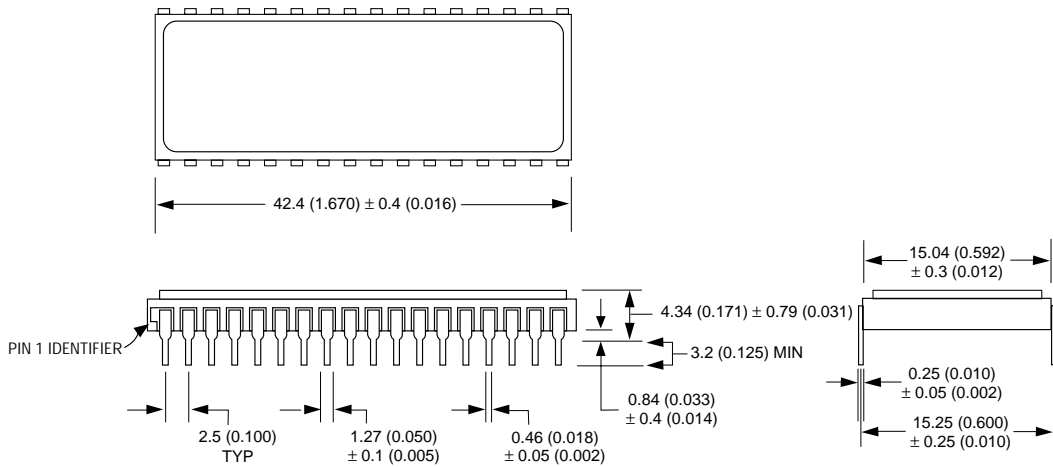


**WRITE CYCLE -  $\overline{CS}$  CONTROLLED**





PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

WS 1M8 - XXX C X X

LEAD FINISH:

- Blank = Gold plated leads
- A = Solder dip leads

DEVICE GRADE:

- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

PACKAGE:

- C = Ceramic 0.600" DIP (Package 300)

ACCESS TIME (ns)

ORGANIZATION, two banks of 512K x 8

SRAM

WHITE MICROELECTRONICS