



2Mx8 MONOLITHIC FLASH, SMD 5962-97609 PRELIMINARY*

FEATURES

- Access Times of 90, 120, 150ns
- Packaging:
 - 56 lead, Hermetic Ceramic, 0.520" CSOP (Package 207). Fits standard 56 SSOP footprint.
 - 44 pin Ceramic LCC**
 - 44 pin Ceramic SOJ (Package 102)**
 - 44 lead Ceramic Flatpack (Package 225)**
- Sector Architecture
 - 32 equal size sectors of 64KBytes each
 - Any combination of sectors can be erased. Also supports full chip erase.
- 100,000 Write/Erase Cycles Minimum
- Organized as 2Mx8
- Commercial, Industrial, and Military Temperature Ranges

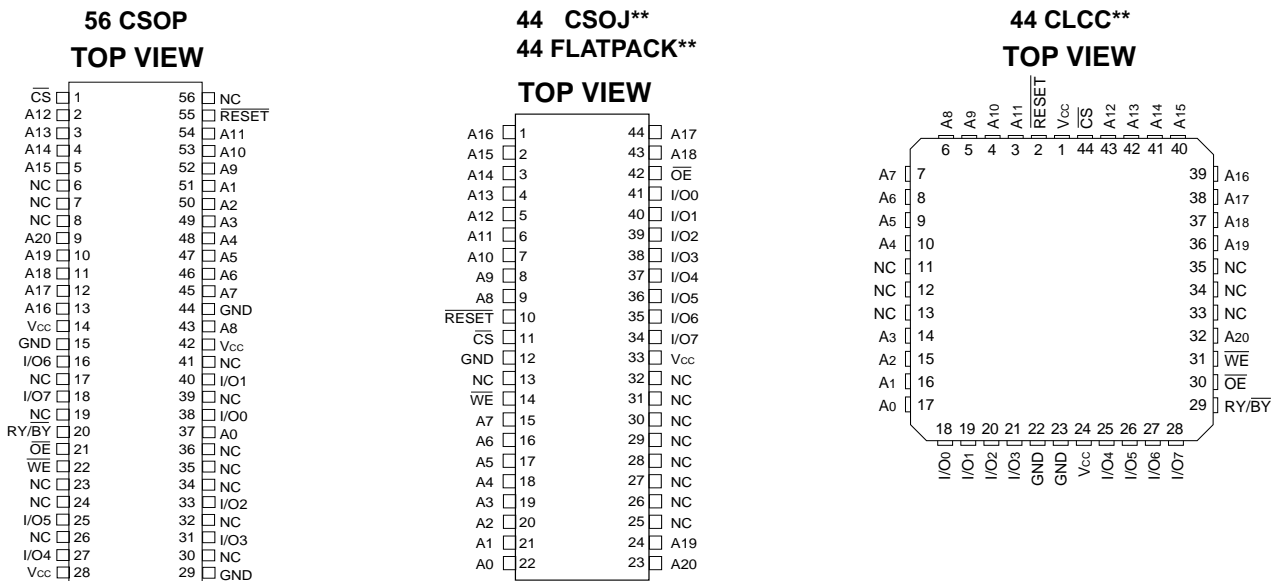
- 5 Volt Read and Write. 5V ±10% Supply.
- Low Power CMOS
- Data Polling and Toggle Bit feature for detection of program or erase cycle completion.
- Supports reading or programming data to a sector not being erased.
- RESET pin resets internal state machine to the read mode.
- Multiple Ground Pins for Low Noise Operation

* This data sheet describes a product under development, not fully characterized, and is subject to change without notice.

** Package to be developed.

Note: For programming information refer to Flash Programming 16M5 Application Note.

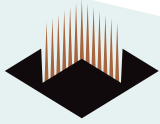
FIG. 1 PIN CONFIGURATION FOR WMF2M8-XXX5



PIN DESCRIPTION

I/O0-7	Data Inputs/Outputs
A0-20	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
Vcc	Power Supply
GND	Ground
RY/BY	Ready/Busy
RESET	Reset

** Package to be developed.



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to V _{SS}	V _T	-2.0 to +7.0	V
Power Dissipation	P _T	8	W
Storage Temperature	T _{stg}	-65 to +125	°C
Short Circuit Output Current	I _{OS}	100	mA
Endurance - Write/Erase Cycles (Mil Temp)		100,000 min	cycles
Data Retention (Mil Temp)		20	years

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
Address Input capacitance	C _{AD}	V _{I/O} = 0 V, f = 1.0 MHz	12	pF
Output Enable capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	12	pF
Write Enable capacitance	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	12	pF
Chip Select capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	12	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	12	pF

This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} + 0.5	V
Input Low Voltage	V _{IL}	-0.5	-	+0.8	V
Operating Temperature (Mil.)	T _A	-55	-	+125	°C
Operating Temperature (Ind.)	T _A	-40	-	+85	°C

DC CHARACTERISTICS - CMOS COMPATIBLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I _{LI}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	V _{CC} = 5.5, V _{IN} = GND to V _{CC}		10	μA
V _{CC} Active Current for Read (1)	I _{CC1}	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH}, f = 5\text{MHz}$		40	mA
V _{CC} Active Current for Program or Erase (2)	I _{CC2}	$\overline{CS} = V_{IL}, \overline{OE} = V_{IH}$		60	mA
V _{CC} Standby Current	I _{CC3}	V _{CC} = 5.5, $\overline{CS} = V_{IH}, f = 5\text{MHz}, \overline{RESET} = V_{CC} \pm 0.3\text{V}$		2.0	mA
Output Low Voltage	V _{OL}	I _{OL} = 12.0 mA, V _{CC} = 4.5		0.45	V
Output High Voltage	V _{OH}	I _{OH} = -2.5 mA, V _{CC} = 4.5	0.85xV _{CC}		V
Low V _{CC} Lock-Out Voltage	V _{LKO}		3.2	4.2	V

NOTES:

- The I_{CC} current listed includes both the DC operating current and the frequency dependent component (@ 5MHz). The frequency component typically is less than 2mA/MHz, with \overline{OE} at V_{IH}.
- I_{CC} active while Embedded Algorithm (program or erase) is in progress.
- DC test conditions V_{IL} = 0.3V, V_{IH} = V_{CC} - 0.3V



AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS - WE CONTROLLED
 (V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter	Symbol		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{wc}	90		120		150		ns
Chip Select Setup Time	t _{ELWL}	t _{cs}	0		0		0		ns
Write Enable Pulse Width	t _{WLWH}	t _{wP}	45		50		50		ns
Address Setup Time	t _{AVWL}	t _{as}	0		0		0		ns
Data Setup Time	t _{DVWH}	t _{ds}	45		50		50		ns
Data Hold Time	t _{WHDX}	t _{dh}	0		0		0		ns
Address Hold Time	t _{WLAX}	t _{ah}	45		50		50		ns
Write Enable Pulse Width High	t _{WHWL}	t _{wPH}	20		20		20		ns
Duration of Byte Programming Operation (1)	t _{WHWH1}			300		300		300	μs
Sector Erase (2)	t _{WHWH2}			15		15		15	sec
Read Recovery Time before Write	t _{GHWL}		0		0		0		μs
V _{CC} Setup Time	t _{vcs}		50		50		50		μs
Chip Programming Time				44		44		44	sec
Chip Erase Time (3)				256		256		256	sec
Output Enable Hold Time (4)		t _{oEH}	10		10		10		ns
RESET Pulse Width		t _{rP}	500		500		500		ns

NOTES:

1. Typical value for t_{WHWH1} is 7μs.
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

AC CHARACTERISTICS – READ-ONLY OPERATIONS
 (V_{CC} = 5.0V, T_A = -55°C to +125°C)

Parameter	Symbol		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{rc}	90		120		150		ns
Address Access Time	t _{AVQV}	t _{acc}		90		120		150	ns
Chip Select Access Time	t _{ELQV}	t _{ce}		90		120		150	ns
Output Enable to Output Valid	t _{GLOV}	t _{oe}		40		50		55	ns
Chip Select High to Output High Z (1)	t _{EHQZ}	t _{df}		20		30		35	ns
Output Enable High to Output High Z (1)	t _{GHQZ}	t _{df}		20		30		35	ns
Output Hold from Addresses, CS or OE Change, whichever is First	t _{AXQX}	t _{oh}	0		0		0		ns
RESET Low to Read Mode (1)		t _{Ready}		20		20		20	μs

1. Guaranteed by design, not tested.



AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, \overline{CS} CONTROLLED

($V_{CC} = 5.0V$, $V_{SS} = 0V$, $T_A = -55^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	90		120		150		ns
Write Enable Setup Time	t_{WLLEL}	t_{WS}	0		0		0		ns
Chip Select Pulse Width	t_{ELEH}	t_{CP}	45		50		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	45		50		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	45		50		50		ns
Chip Select Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300	μs
Sector Erase Time (2)	t_{WHWH2}			15		15		15	sec
Read Recovery Time	t_{GHLEL}		0		0		0		μs
Chip Programming Time				44		44		44	sec
Chip Erase Time (3)				256		256		256	sec
Output Enable Hold Time (4)		t_{OEHL}	10		10		10		ns

NOTES:

1. Typical value for t_{WHWH1} is 7 μs .
2. Typical value for t_{WHWH2} is 1sec.
3. Typical value for Chip Erase Time is 32sec.
4. For Toggle and Data Polling.

FIG. 2
AC TEST CIRCUIT

The diagram shows a bridge circuit with four diodes. A D.U.T. (Device Under Test) is connected to the left node, with an effective capacitance $C_{eff} = 50$ pf. Two current sources are connected to the top and bottom nodes, with currents I_{OL} and I_{OH} respectively. The bridge is powered by a bipolar supply $V_Z \approx 1.5V$.

AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0, V_{IH} = 3.0$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
 V_Z is programmable from -2V to +7V.
 I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance $Z_0 = 75 \Omega$.
 V_Z is typically the midpoint of V_{OH} and V_{OL} .
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

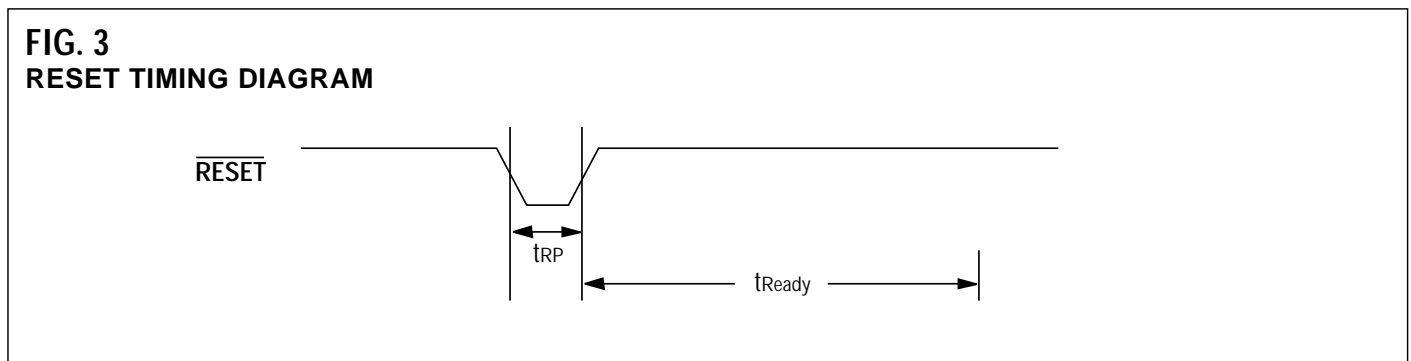




FIG. 4
AC WAVEFORMS FOR READ OPERATIONS

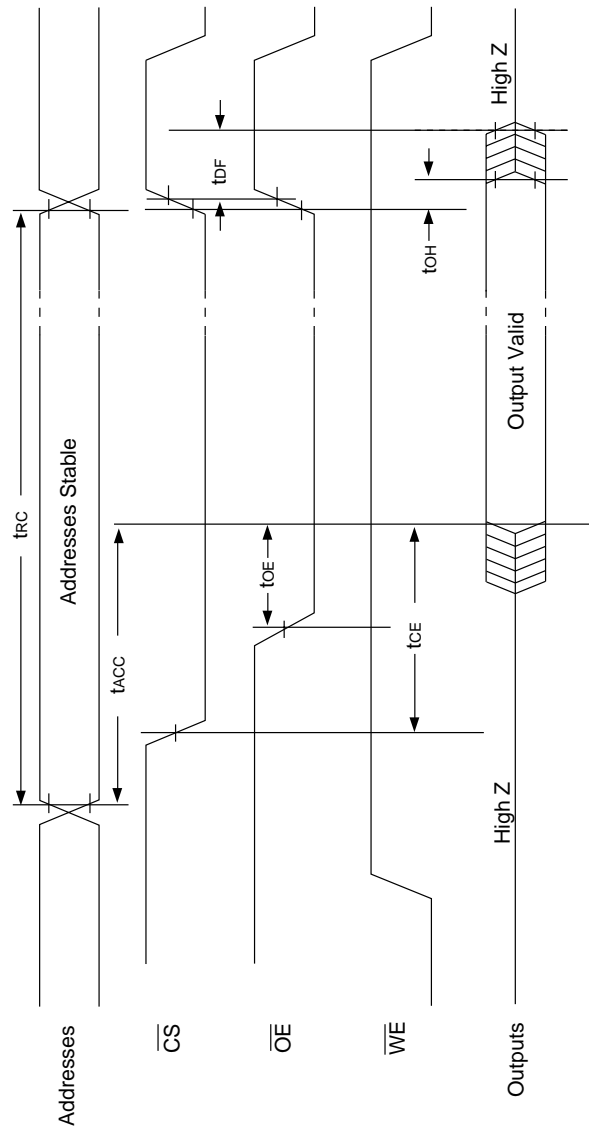
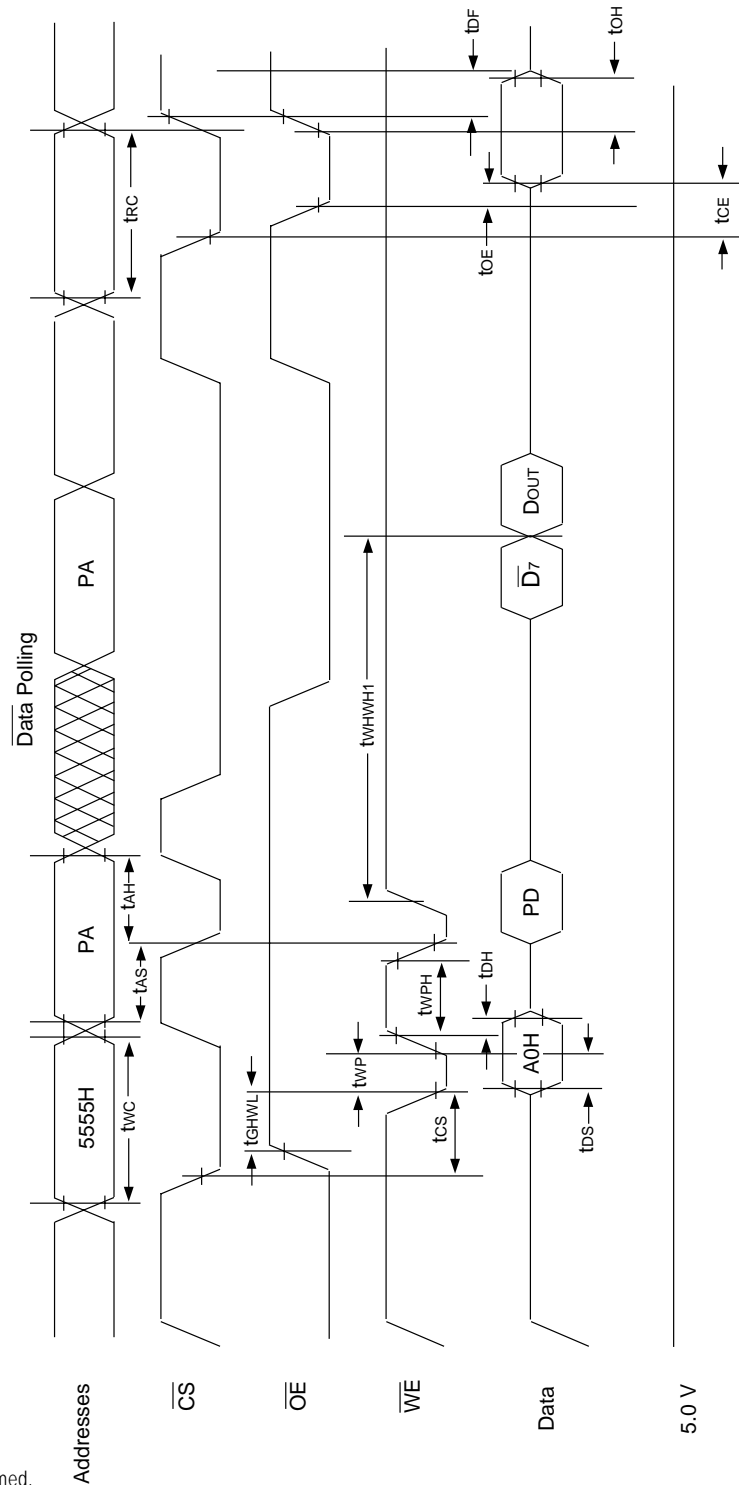




FIG. 5
WRITE/ERASE/PROGRAM
OPERATION, WE CONTROLLED

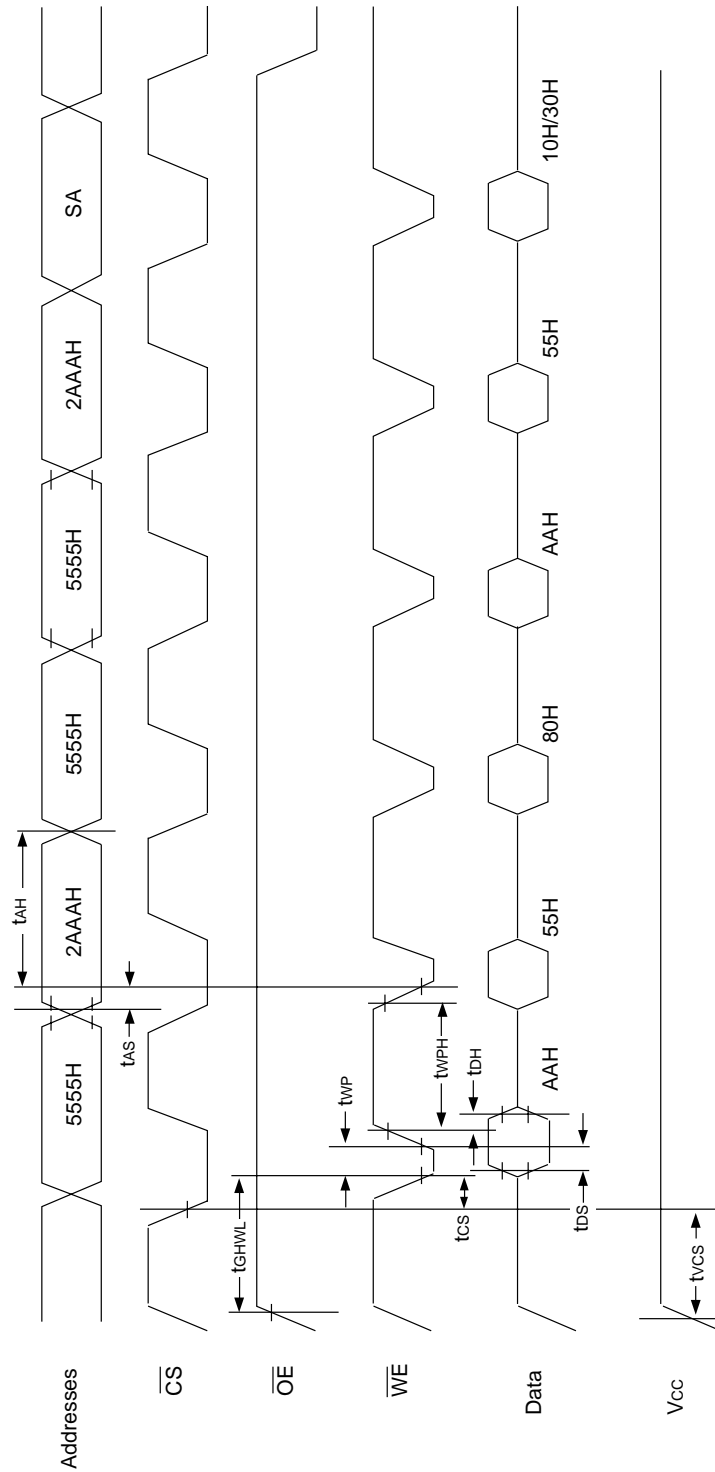


NOTES:

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. $\overline{D7}$ is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.



FIG. 6
AC WAVEFORMS CHIP/SECTOR
ERASE OPERATIONS



NOTE:
1. SA is the sector address for Sector Erase.



FIG. 7
AC WAVEFORMS FOR $\overline{\text{DATA}}$ POLLING
DURING EMBEDDED ALGORITHM OPERATIONS

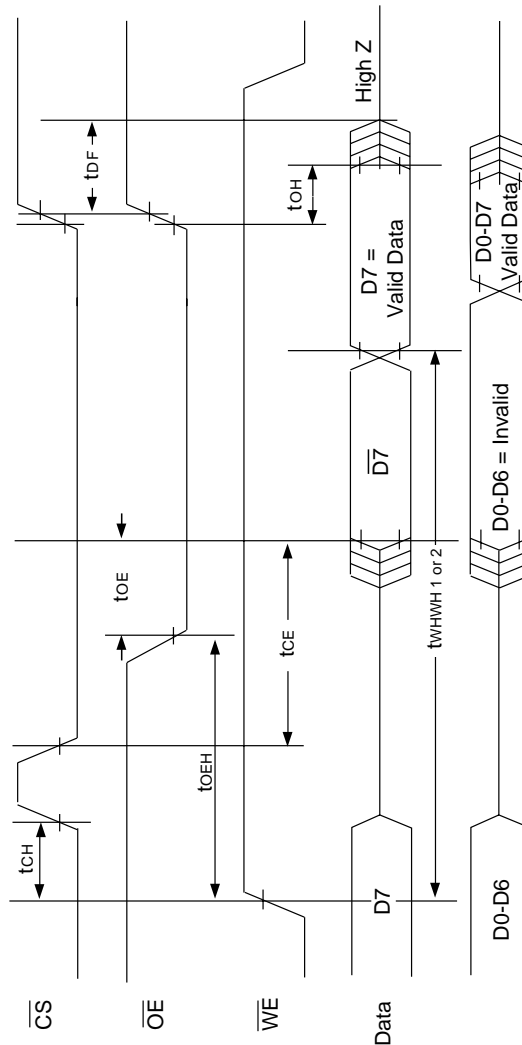
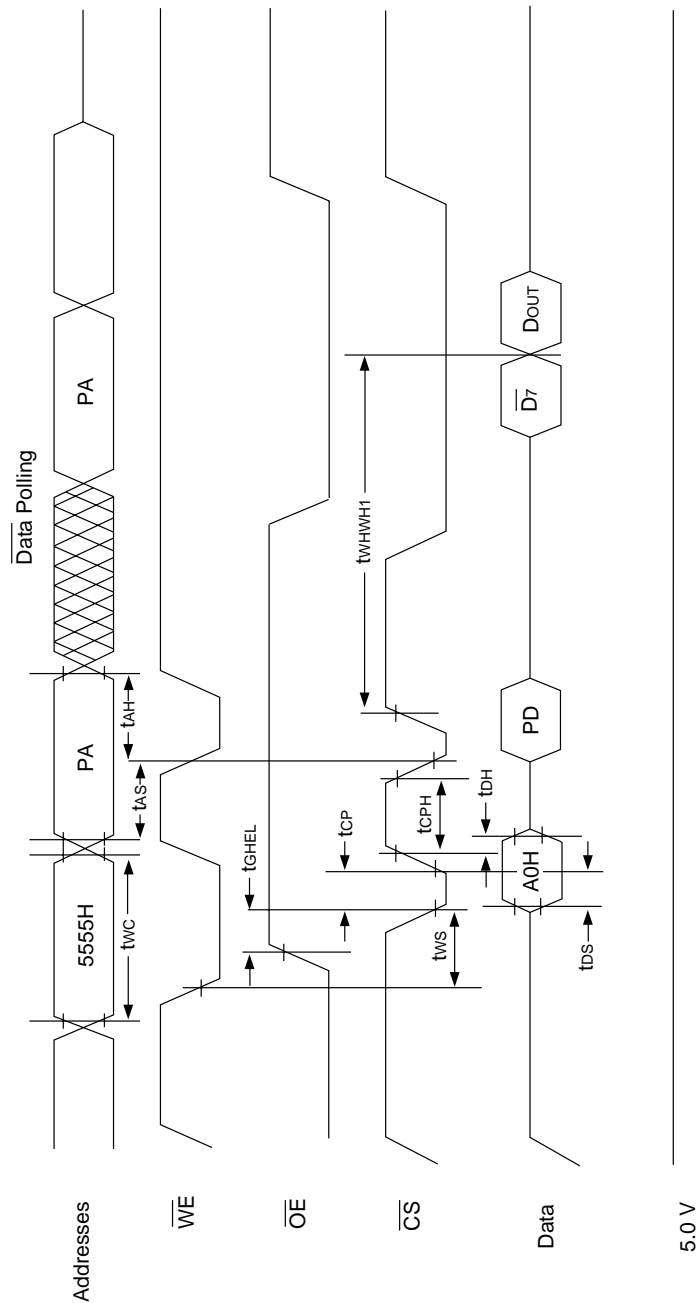


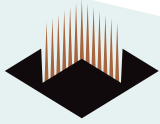


FIG. 8
ALTERNATE \overline{CS} CONTROLLED
PROGRAMMING OPERATION TIMINGS

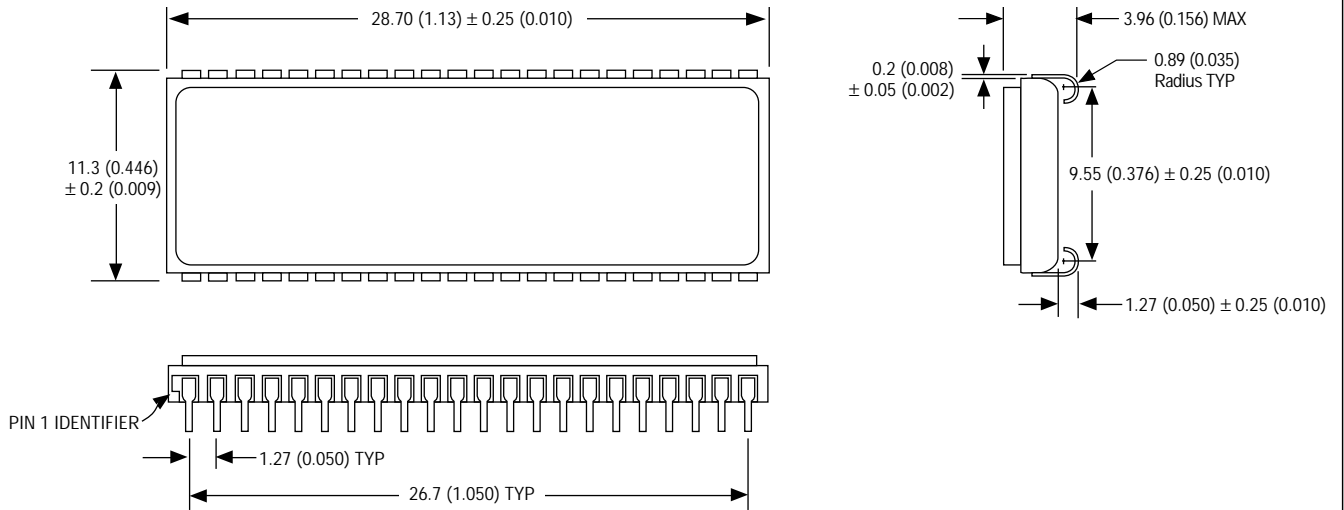


NOTES:

- 1. PA represents the address of the memory location to be programmed.
- 2. PD represents the data to be programmed at byte address.
- 3. $\overline{D7}$ is the output of the complement of the data written to the device.
- 4. Dout is the output of the data written to the device.
- 5. Figure indicates the last two bus cycles of a four bus cycle sequence.



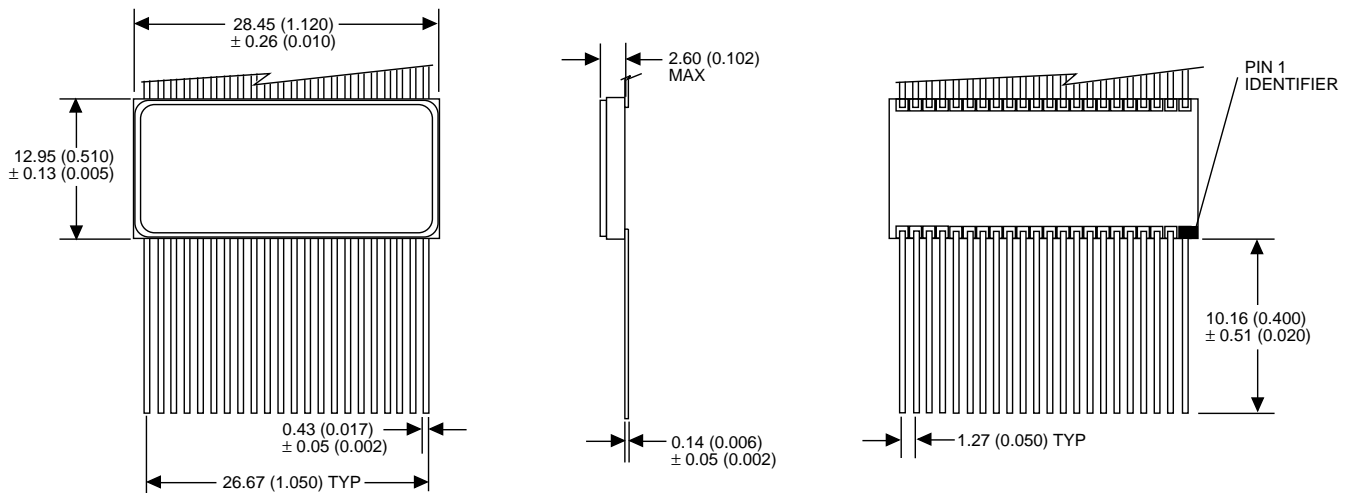
PACKAGE 102: 44 LEAD, CERAMIC SOJ**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

** Package to be developed.

PACKAGE 225: 44 LEAD, CERAMIC FLATPACK**

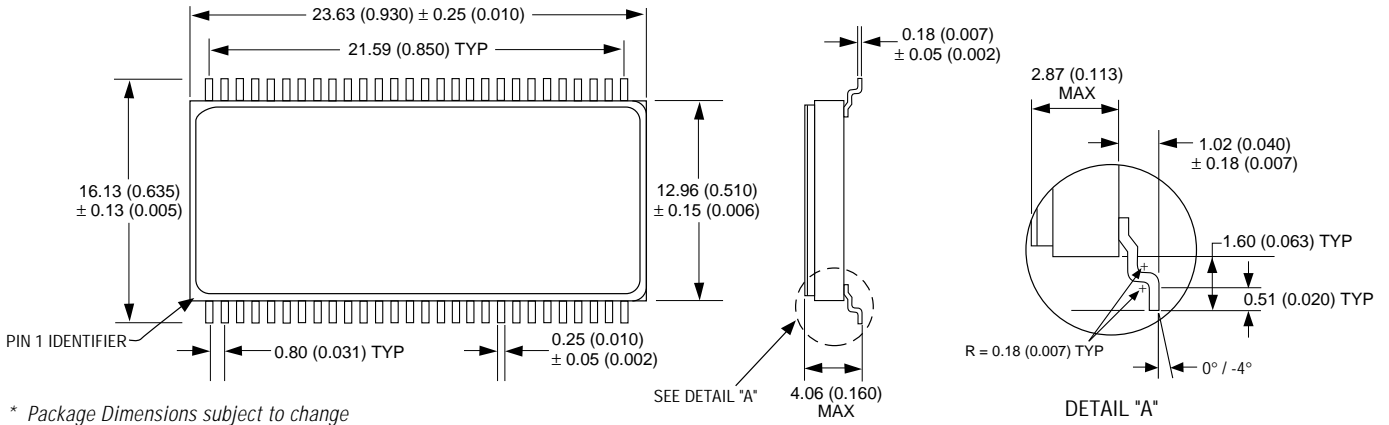


ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

** Package to be developed.



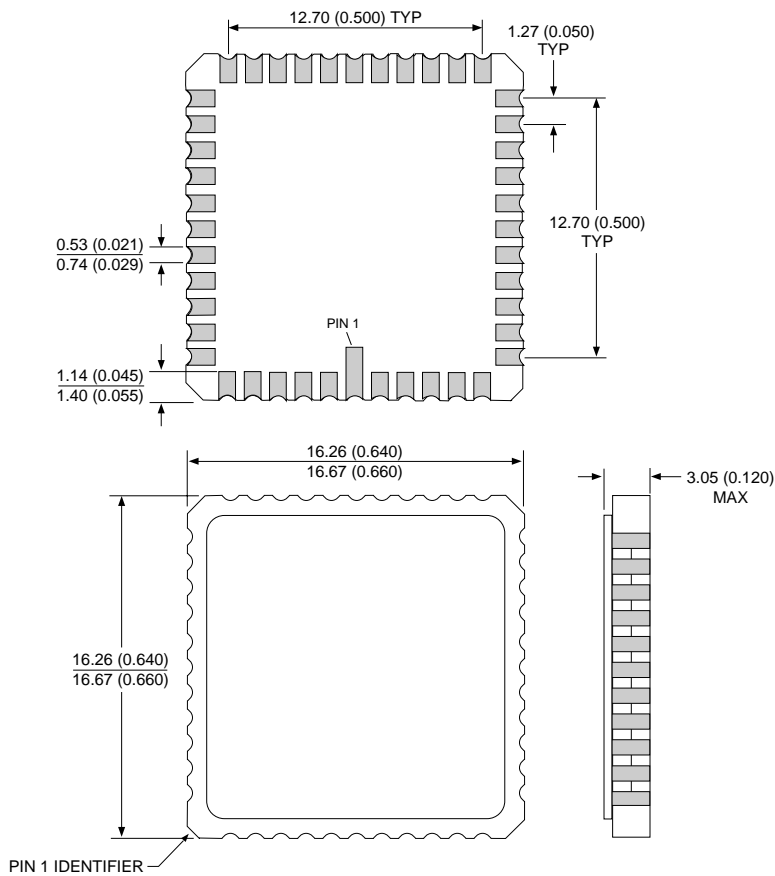
PACKAGE 207: 56 LEAD, CERAMIC SOP**



* Package Dimensions subject to change

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE DIMENSION: 44 LEAD, CERAMIC LCC**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

** Package to be developed.



ORDERING INFORMATION

W M F 2M 8 - XXX X X 5 X

LEAD FINISH:

Blank = Gold plated leads
 A = Solder dip leads

V_{PP} PROGRAMMING VOLTAGE

5 = 5V

DEVICE GRADE:

M = Military, 883 Screened -55°C to +125°C
 I = Industrial -40°C to +85°C
 C = Commercial 0°C to +70°C

PACKAGE TYPE:

DA = 56 Lead CSOP (Package 207)
 fits standard 56 SSOP footprint
 DL = 44 Lead Ceramic SOJ (Package 102)*
 FL = 44 Lead Ceramic Flatpack (Package 225)*
 L = 44 Lead Ceramic LCC*

ACCESS TIME (ns)

ORGANIZATION, 2M x 8

Flash

MONOLITHIC

WHITE ELECTRONIC DESIGNS CORP.

* Package to be developed.

DEVICE TYPE	SECTOR SIZE	SPEED	PACKAGE	SMD NO.
2M x 8 Flash Monolithic	64KByte	150ns	56 lead CSOP (DA)	5962-97609 01HXX
2M x 8 Flash Monolithic	64KByte	120ns	56 lead CSOP (DA)	5962-97609 02HXX
2M x 8 Flash Monolithic	64KByte	90ns	56 lead CSOP (DA)	5962-97609 03HXX