128Kx32 5V FLASH MODULE, SMD 5962-94716

FEATURES

- Access Times of 50*, 60, 70, 90, 120, 150ns
- Packaging:
  - 66 pin, PGA Type, 1.075 inch square, Hermetic Ceramic HIP (Package 400)
  - 68 lead, Hermetic CQFP (G2U)[1], 22.4mm (0.880 inch) square, 3.56mm (0.140 inch) high (Package 510)
  - 68 lead, Hermetic CQFP (G1U), 23.9mm (0.940 inch) square, 3.56mm (0.140 inch) high (Package 519)
  - 68 lead, Hermetic CQFP (G1T), 23.9mm (0.940 inch) square, 4.06mm (0.160 inch) high (Package 524)
- Sector Architecture
  - 8 equal size sectors of 16KBytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- 100,000 Erase/Program Cycles Typical, 0°C to +70°C
- Organized as 128Kx32
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Programming. 5V ± 10% Supply
- Low Power CMOS, 1mA Standby Typical
- Embedded Erase and Program Algorithms
- TTL Compatible Inputs and CMOS Outputs
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Page Program Operation and Internal Program Control Time
- Weight

  WF128K32-XG1UX5 - 5 grams typical

  WF128K32-XG1TX5 - 5 grams typical

  WF128K32-XG2UX5[1] - 8 grams typical

  WF128K32-XH1X5 - 13 grams typical

Note 1: Package Not Recommended For New Design
Note: For programming information refer to Flash Programming 1M5 Application Note.
** The access time of 50ns is available in Industrial and Commercial temperature ranges only.*

FIG. 1 PIN CONFIGURATION FOR WF128K32N-XH1X5

TOP VIEW

1	12	23	34	45	56
I/O8	$\overline{WE}_2$	I/O15	I/O24	VCC	I/O31
I/O9	$\overline{CS}_2$	I/O14	I/O25	$\overline{CS}_4$	I/O30
I/O10	GND	I/O13	I/O26	$\overline{WE}_4$	I/O29
A13	I/O11	I/O12	A6	I/O27	I/O28
A14	A10	$\overline{OE}$	A7	A3	A0
A15	A11	NC	NC	A4	A1
A16	A12	$\overline{WE}_1$	A8	A5	A2
NC	VCC	I/O7	A9	$\overline{WE}_3$	I/O23
I/O0	$\overline{CS}_1$	I/O6	I/O16	$\overline{CS}_3$	I/O22
I/O1	NC	I/O5	I/O17	GND	I/O21
I/O2	I/O3	I/O4	I/O18	I/O19	I/O20
11	22	33	44	55	66

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

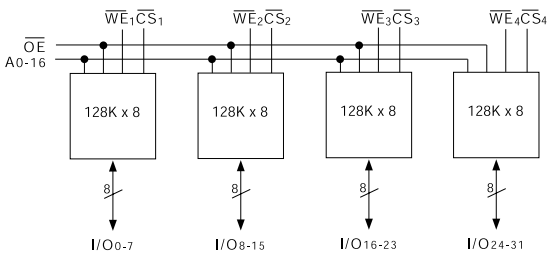
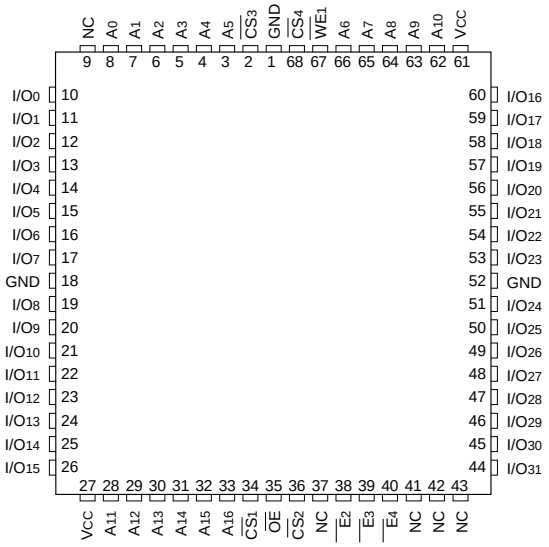


FIG. 3 PIN CONFIGURATION FOR WF128K32-XG1UX5, WF128K32-XG1TX5 AND WF128K32-XG2UX5[1]

TOP VIEW



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
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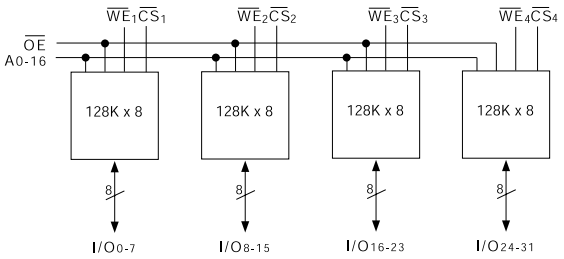
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



Note 1: Package Not Recommended For New Design

ABSOLUTE MAXIMUM RATINGS (1)

Parameter		Unit
Operating Temperature	-55 to +125	°C
Supply Voltage Range (V_{CC})	-2.0 to +7.0	V
Signal voltage range (any pin except A9) (2)	-2.0 to +7.0	V
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering, 10 seconds)	+300	°C
Data Retention Mil Temp	10 years	
Endurance (write/erase cycles) Mil Temp	10,000 cycles min.	
A_9 Voltage for sector protect (V_{ID}) (3)	-2.0 to +14.0	V

NOTES:
1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2. Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may overshoot Vss to -2.0 V for periods of up to 20ns. Maximum DC voltage on output and I/O pins is Vcc + 0.5V. During voltage transitions, outputs may overshoot to Vcc + 2.0 V for periods of up to 20ns.
3. Minimum DC input voltage on A9 pin is -0.5V. During voltage transitions, A9 may overshoot Vss to -2V for periods of up to 20ns. Maximum DC input voltage on A9 is +13.5V which may overshoot to 14.0 V for periods up to 20ns.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C
A_9 Voltage for Sector Protect	V_{ID}	11.5	12.5	V

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}_{1-4}$ capacitance HIP (PGA)	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
CQFP G2U/G1U/G1T			15	
$\overline{CS}_{1-4}$ capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS - CMOS COMPATIBLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C TO +125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LOx32}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
V_{CC} Active Current for Read (1)	I_{CC1}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}		140	mA
V_{CC} Active Current for Program or Erase (2)	I_{CC2}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}		200	mA
V_{CC} Standby Current	I_{CC3}	V_{CC} = 5.5, $\overline{CS}$ = V_{IH}, f = 5MHz		6.5	mA
V_{CC} Static Current	I_{CC4}	V_{CC} = 5.5, $\overline{CS}$ = V_{IH}		0.6	mA
Output Low Voltage	V_{OL}	I_{OL} = 8.0 mA, V_{CC} = 4.5		0.45	V
Output High Voltage	V_{OH1}	I_{OH} = -2.5 mA, V_{CC} = 4.5	0.85 x V_{CC}		V
Output High Voltage	V_{OH2}	I_{OH} = -100 µA, V_{CC} = 4.5	V_{CC} -0.4		V
Low V_{CC} Lock Out Voltage	V_{LKO}		3.2		V

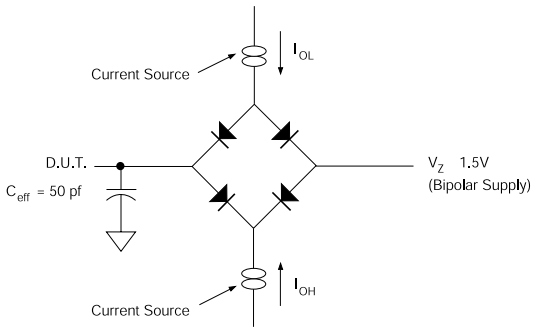
NOTES:
1. The ICC current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at VIH.
2. ICC active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions: VIL = 0.3V, VIH = VCC - 0.3V

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{CS}$ CONTROLLED

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C TO +125°C)

Parameter	Symbol		-50		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	50		60		70		90		120		150		ns
$\overline{WE}$ Setup Time	t_{WLEL}	t_{WS}	0		0		0		0		0		0		ns
$\overline{CS}$ Pulse Width	t_{ELEH}	t_{CP}	25		30		35		45		50		50		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		0		0		0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	25		30		30		45		50		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	40		45		45		45		50		50		ns
$\overline{WE}$ Hold from $\overline{WE}$ High	t_{EHWH}	t_{WH}	0		0		0		0		0		0		ns
$\overline{CS}$ Pulse Width High	t_{EHEL}	t_{CPH}	20		20		20		20		20		20		ns
Duration of Programming Operation	t_{WHWH1}		14		14		14		14		14		14		µs
Duration of Erase Operation	t_{WHWH2}		2.2	60	2.2	60	2.2	60	2.2	60	2.2	60	2.2	60	sec
Read Recovery before Write	t_{GHEL}		0		0		0		0		0		0		ns
Chip Programming Time				12.5		12.5		12.5		12.5		12.5		12.5	sec

FIG. 4 AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:
VZ is programmable from -2V to +7V.
IOL & IOH programmable from 0 to 16mA.
Tester Impedance Z0 = 75 ý.
VZ is typically the midpoint of VOH and VOL.
IOL & IOH are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{WE}$ CONTROLLED

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C TO +125°C)

Parameter	Symbol		-50		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	50		60		70		90		120		150		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		0		0		0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	25		30		35		45		50		50		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		0		0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	25		30		30		45		50		50		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		0		0		0		ns
Address Hold Time	t_{WLAX}	t_{AH}	40		45		45		45		50		50		ns
Chip Select Hold Time	t_{WHEH}	t_{CH}	0		0		0		0		0		0		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	20		20		20		20		20		20		ns
Duration of Byte Programming Operation (min)	t_{WHWH1}		14		14		14		14		14		14		µs
Sector Erase Time	t_{WHWH2}		2.2	60	2.2	60	2.2	60	2.2	60	2.2	60	2.2	60	sec
Read Recovery Time Before Write	t_{GHWL}		0		0		0		0		0		0		ns
V_{CC} Setup Time		t_{VCS}	50		50		50		50		50		50		µs
Chip Programming Time				12.5		12.5		12.5		12.5		12.5		12.5	sec
Output Enable Setup Time		t_{OES}	0		0		0		0		0		0		ns
Output Enable Hold Time (1)		t_{OEH}	10		10		10		10		10		10		ns

1. For Toggle and $\overline{Data}$ Polling.

AC CHARACTERISTICS – READ ONLY OPERATIONS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C TO +125°C)

Parameter	Symbol		-50		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	50		60		70		90		120		150		ns
Address Access Time	t_{AVQV}	t_{ACC}		50		60		70		90		120		150	ns
Chip Select Access Time	t_{ELQV}	t_{CE}		50		60		70		90		120		150	ns
$\overline{OE}$ to Output Valid	t_{GLQV}	t_{OE}		25		30		35		40		50		55	ns
Chip Select to Output High Z (1)	t_{EHQZ}	t_{DF}		20		20		20		25		30		35	ns
$\overline{OE}$ High to Output High Z (1)	t_{GHQZ}	t_{DF}		20		20		20		25		30		35	ns
Output Hold from Address, $\overline{CS}$ or $\overline{OE}$ Change, whichever is first	t_{AXQX}	t_{OH}	0		0		0		0		0		0		ns

1. Guaranteed by design, not tested.

FIG. 5 AC WAVEFORMS FOR READ OPERATIONS

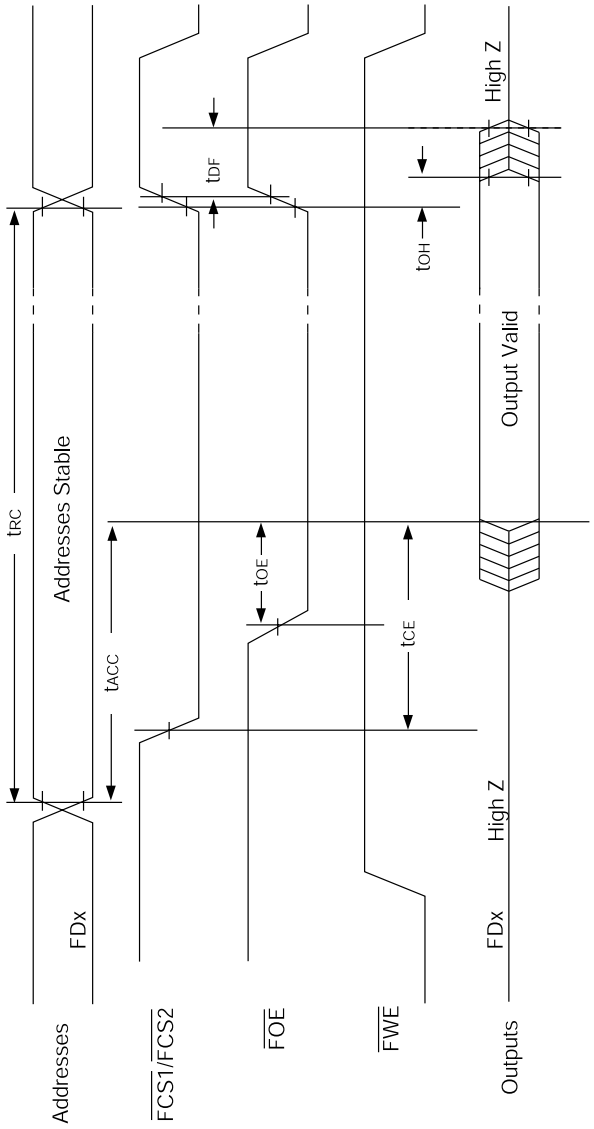
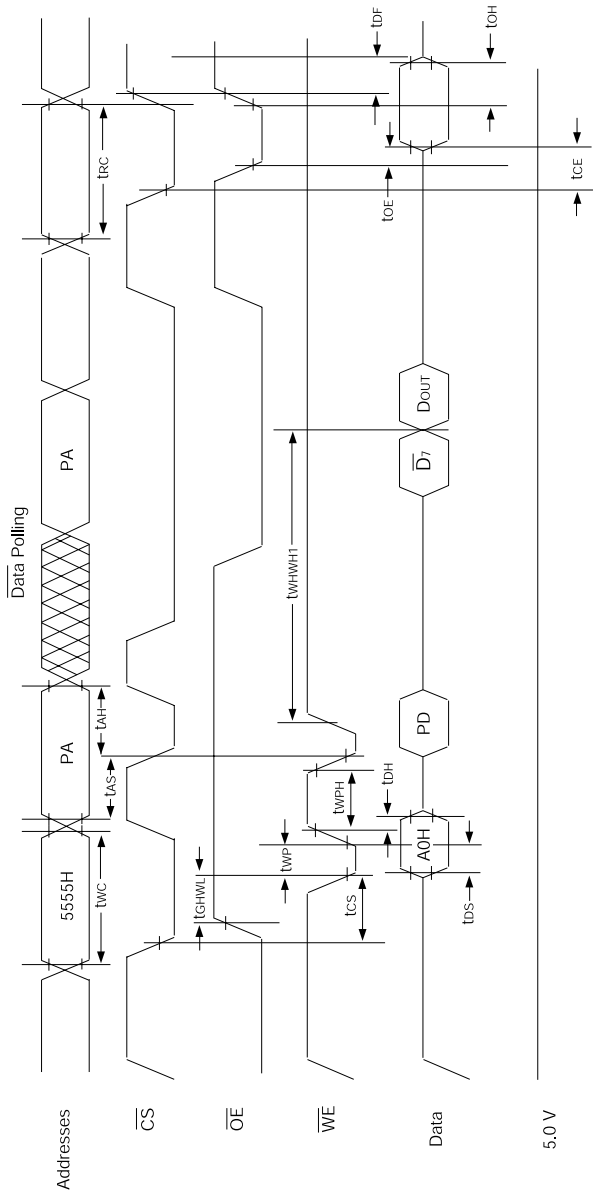


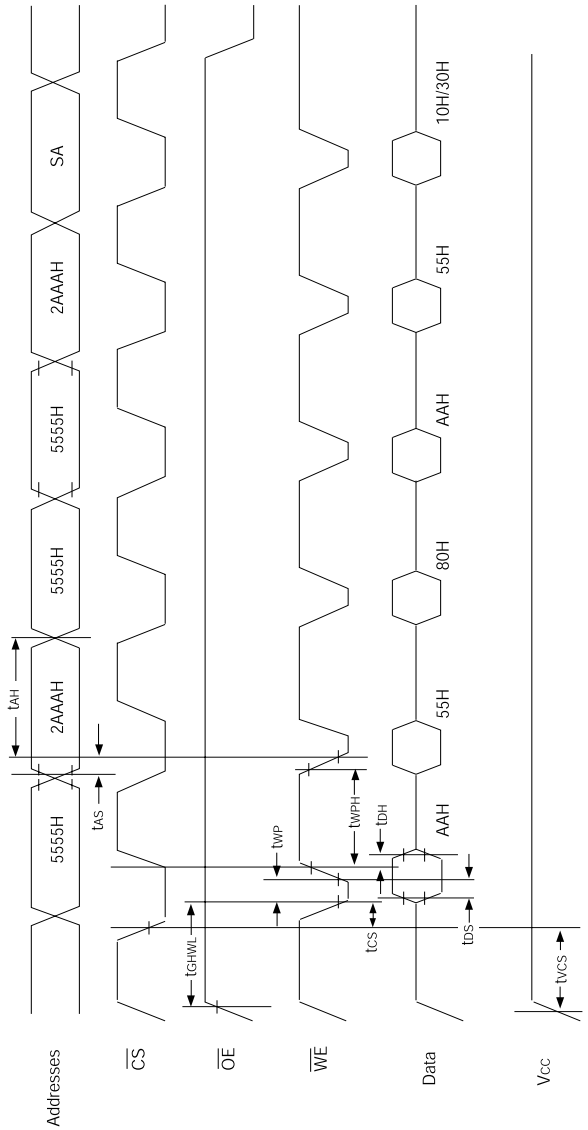
FIG. 6 WRITE/ERASE/PROGRAM OPERATION, $\overline{WE}$ CONTROLLED



NOTES:

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. $\overline{D7}$ is the output of the complement of the data written to the device (for each chip).
4. DOUT is the output of the data written to the device.
5.Figure indicates last two bus cycles of four bus cycle sequence.

FIG. 7 AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS



Notes:
1. SA is the sector address for Sector Erase.

FIG. 8 AC WAVEFORMS FOR $\overline{\text{DATA}}$ POLLING DURING EMBEDDED ALGORITHM OPERATIONS

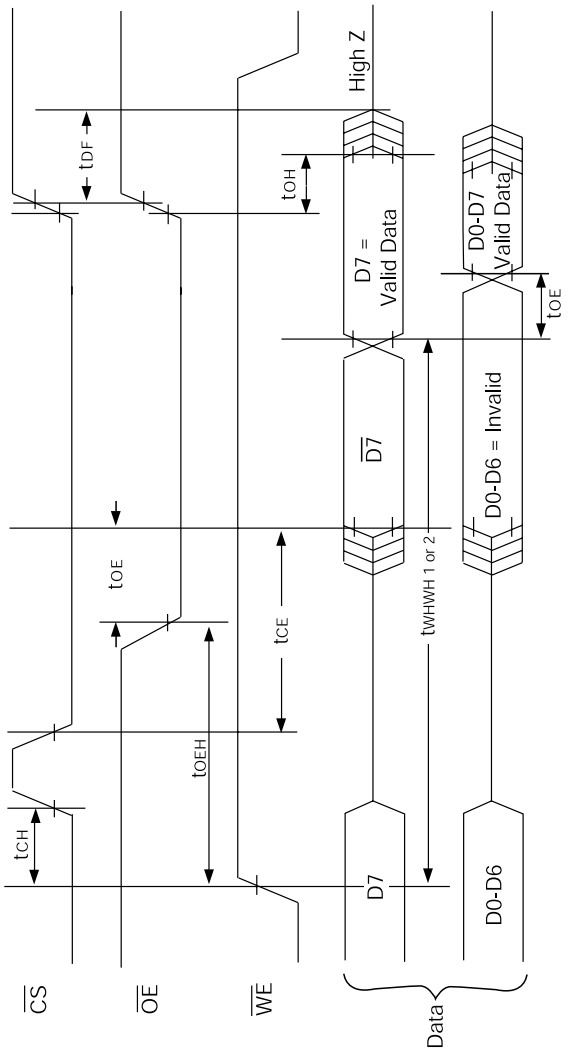
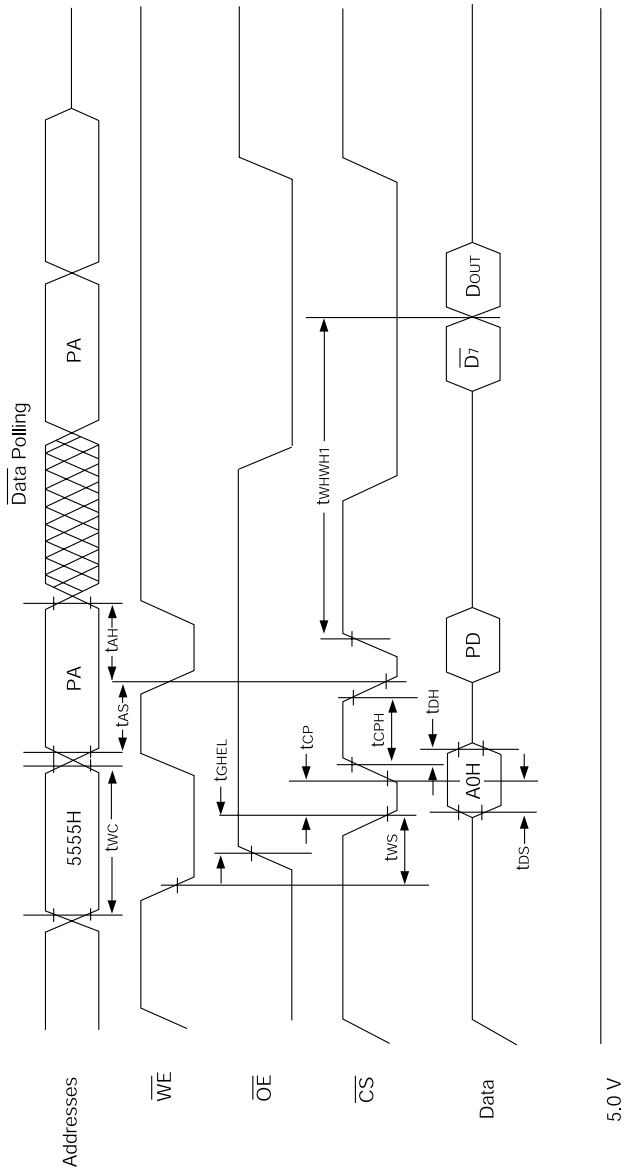


FIG. 9 WRITE/ERASE/PROGRAM OPERATION, $\overline{CS}$ CONTROLLED



NOTES:

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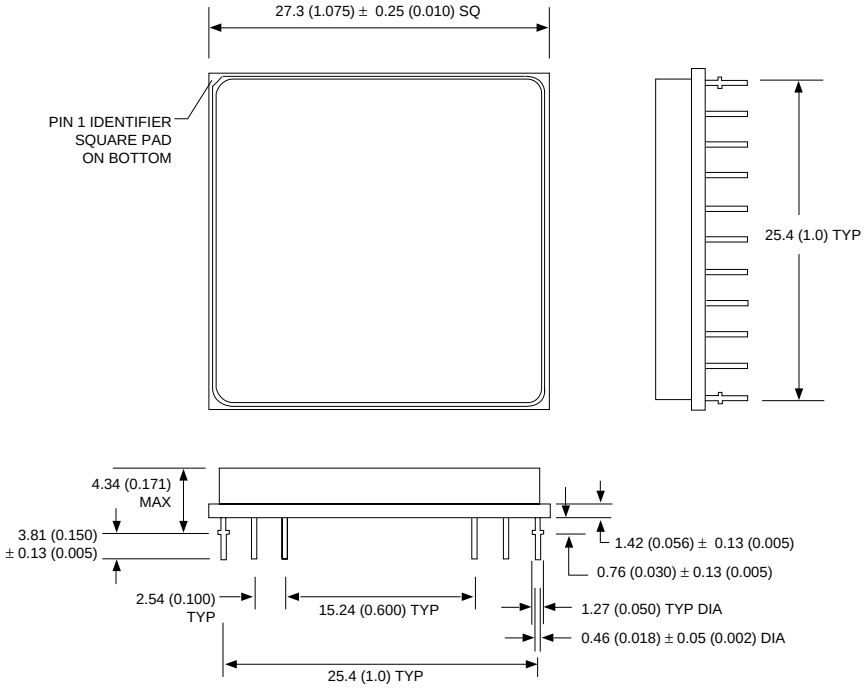
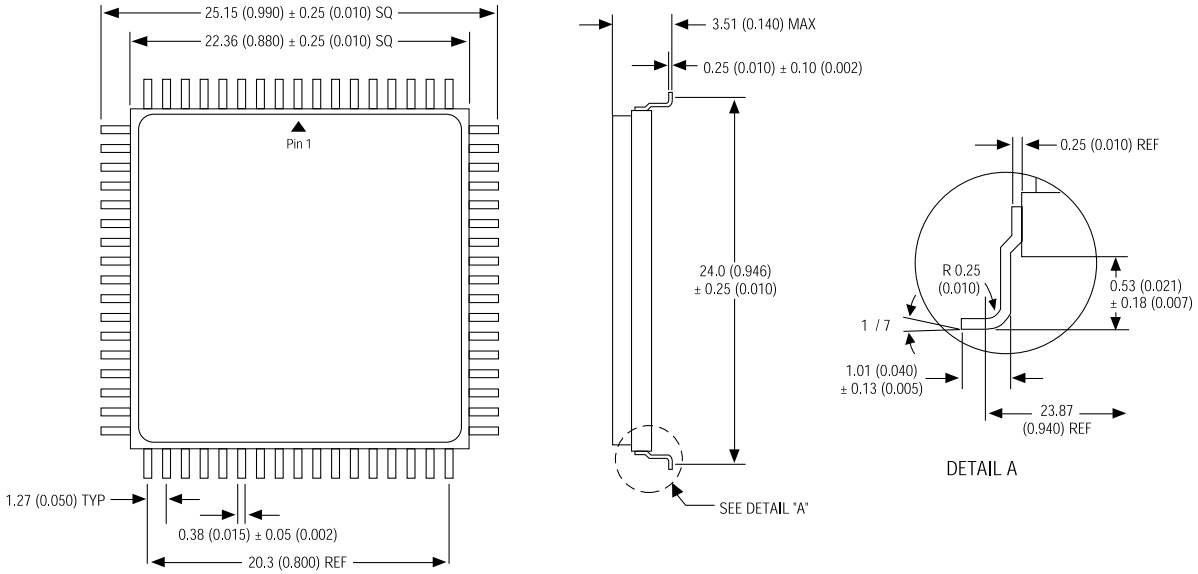
2. PD represents the data to be programmed at byte address.
3. $\overline{D7}$ is the output of the complement of the data written to the device (for each chip).
4. DOUT is the output of the data written to the device.
5. Figure indicates the last two bus cycles of a four bus cycle sequence.

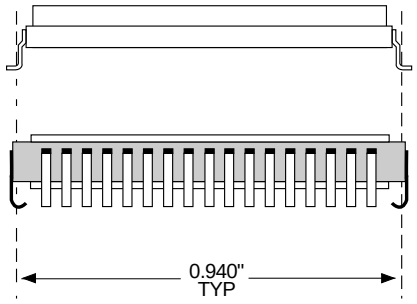
PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 510: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2U)[1]



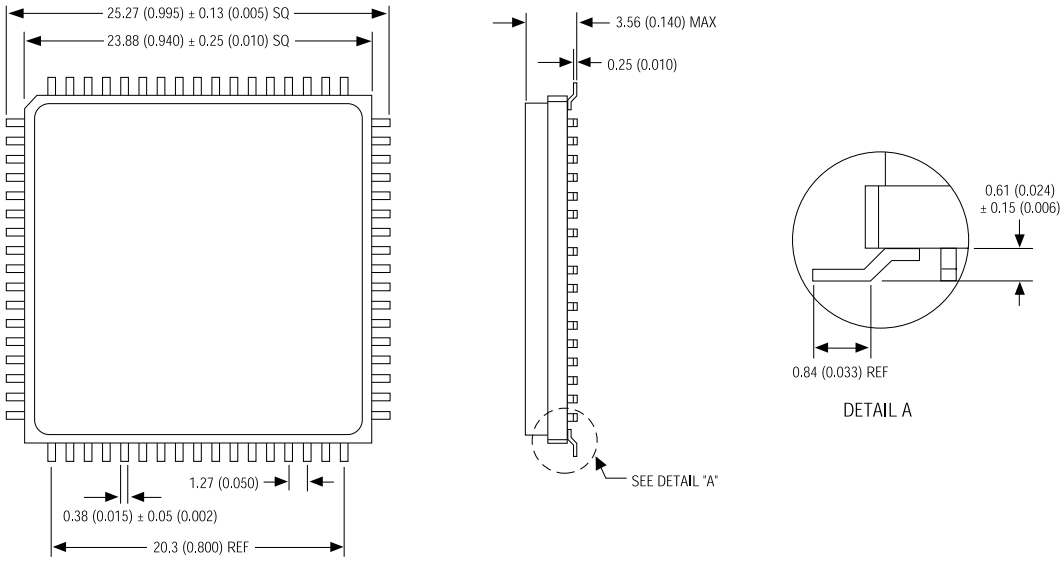


The White 68 lead G2U CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2U has the TCE and lead inspection advantage of the CQFP form.

Note 1: Package Not Recommended For New Design

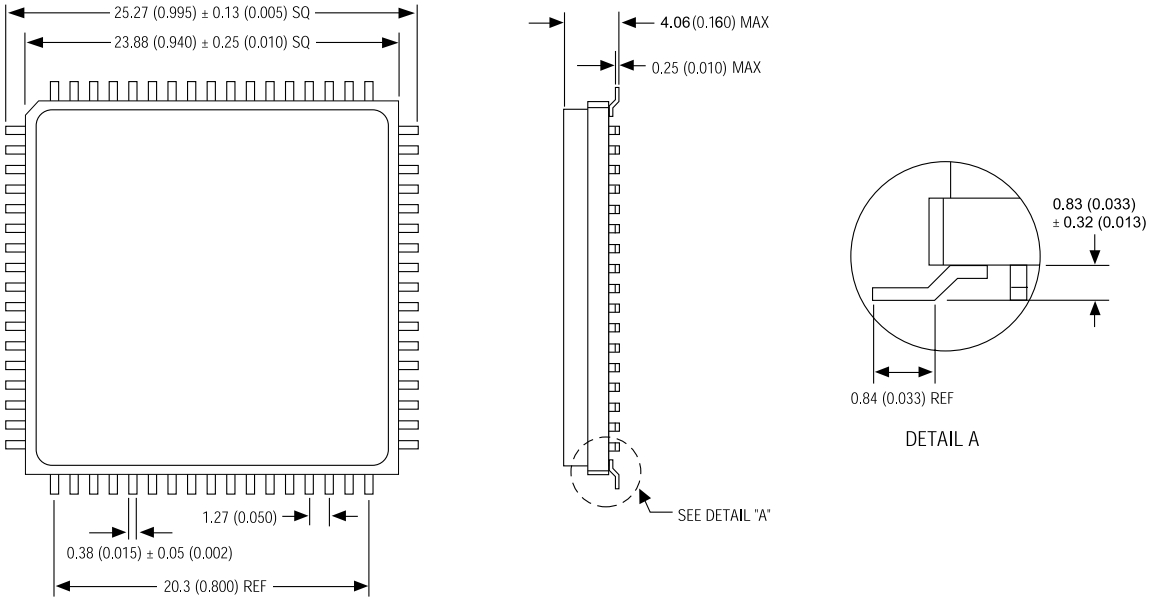
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 519: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G1U)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 524: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G1T)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W F 128K32 X - XXX X X 5 X

LEAD FINISH:
Blank = Gold plated leads
A = Solder dip leads

V_{PP} PROGRAMMING VOLTAGE
5 = 5V

DEVICE GRADE:
Q = MIL - STD 833 Compliant
M = Military Screened -55°C to +125°C
I = Industrial -40°C to +85°C
C = Commercial 0°C to + 70°C

PACKAGE TYPE:
H1 = 1.075" sq. Ceramic Hex In-line Package, HIP (Package 400)
G2U[1] = 22.4mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 510)
G1U = 23.9mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 519)
G1T = 23.9mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 524)

ACCESS TIME (ns)

IMPROVEMENT MARK
N = No Connect at pin 8, 21, 28 and 39 in HIP for Upgrade

ORGANIZATION, 128K x 32
User configurable as 256K x 16 or 512K x 8

Flash

WHITE ELECTRONIC DESIGNS CORP.

Note 1: Package Not Recommended For New Design

DEVICE TYPE	SPEED	PACKAGE	SMD NO.
128K x 32 Flash	150ns	66 pin HIP (H1)	5962-94716 01H8X
128K x 32 Flash	120ns	66 pin HIP (H1)	5962-94716 02H8X
128K x 32 Flash	90ns	66 pin HIP (H1)	5962-94716 03H8X
128K x 32 Flash	70ns	66 pin HIP (H1)	5962-94716 04H8X
128K x 32 Flash	60ns	66 pin HIP (H1)	5962-94716 05H8X
128K x 32 Flash	150ns	68 lead CQFP (G1U)	5962-94716 01H9X
128K x 32 Flash	120ns	68 lead CQFP (G1U)	5962-94716 02H9X
128K x 32 Flash	90ns	68 lead CQFP (G1U)	5962-94716 03H9X
128K x 32 Flash	70ns	68 lead CQFP (G1U)	5962-94716 04H9X
128K x 32 Flash	60ns	68 lead CQFP (G1U)	5962-94716 05H9X
128K x 32 Flash	150ns	68 lead CQFP (G2U)[1]	5962-94716 01HNX[1]
128K x 32 Flash	120ns	68 lead CQFP (G2U)[1]	5962-94716 02HNX[1]
128K x 32 Flash	90ns	68 lead CQFP (G2U)[1]	5962-94716 03HNX[1]
128K x 32 Flash	70ns	68 lead CQFP (G2U)[1]	5962-94716 04HNX[1]
128K x 32 Flash	60ns	68 lead CQFP (G2U)[1]	5962-94716 05HNX[1]

Note 1: Package Not Recommended For New Design