



# 128Kx16 SRAM/512Kx16 FLASH MODULE

## FEATURES

- Access Times of 35ns (SRAM) and 90ns (FLASH)
- Packaging
  - 66 pin, PGA Type, 1.075" square HIP, Hermetic Ceramic HIP (Package 400)
  - 68 lead, Hermetic CQFP (G2U), 22.4mm (0.880") square (Package 510) 3.56mm (0.140") height. Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 2)
- 128Kx16 SRAM
- 512Kx16 5V FLASH
- Organized as 128Kx16 of SRAM and 512Kx16 of Flash Memory with separate Data Buses
- Both blocks of memory are User Configurable as 256Kx8
- Low Power CMOS
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs

- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight:
  - WSF2816-39G2UX - 8 grams typical
  - WSF2816-39H1X - 13 grams typical

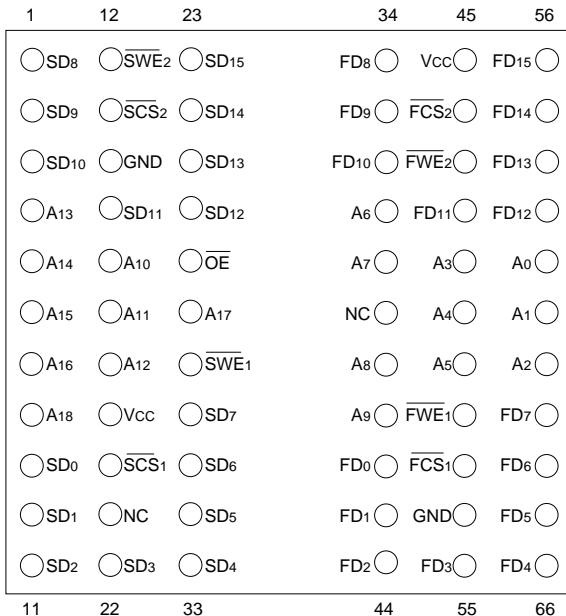
## FLASH MEMORY FEATURES

- 100,000 Erase/Program Cycles
- Sector Architecture
  - 8 equal size sectors of 64K bytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- 5 Volt Programming; 5V ± 10% Supply
- Embedded Erase and Program Algorithms
- Hardware Write Protection

Note: For programming information refer to Flash Programming 4M5 Application Note.

FIG. 1 PIN CONFIGURATION FOR WSF2816-39H1X

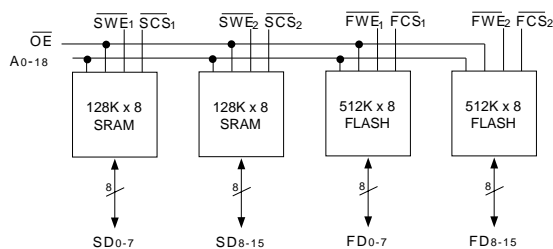
### TOP VIEW



### PIN DESCRIPTION

FD <sub>0-15</sub>	Flash Data Inputs/Outputs
SD <sub>0-15</sub>	SRAM Data Inputs/Outputs
A <sub>0-18</sub>	Address Inputs
SWE <sub>1-2</sub>	SRAM Write Enable
SCS <sub>1-2</sub>	SRAM Chip Selects
OE	Output Enable
V <sub>cc</sub>	Power Supply
GND	Ground
NC	Not Connected
FWE <sub>1-2</sub>	Flash Write Enable
FCS <sub>1-2</sub>	Flash Chip Select

### BLOCK DIAGRAM



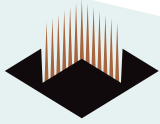
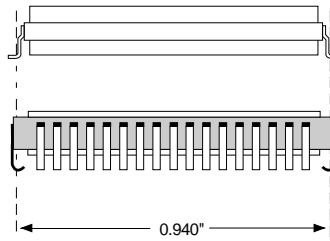
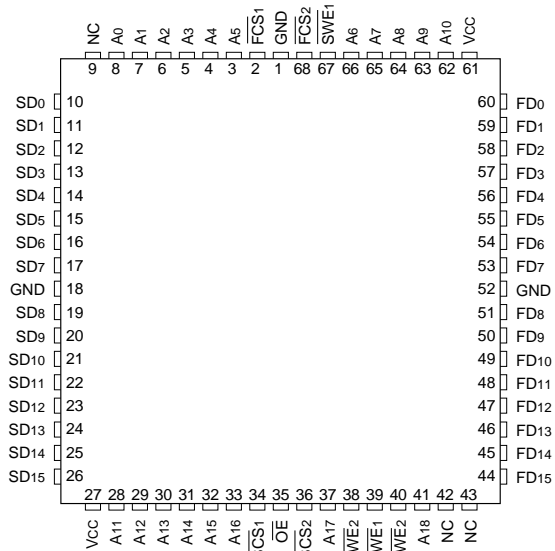


FIG. 2 PIN CONFIGURATION FOR WSF2816-39G2UX

TOP VIEW

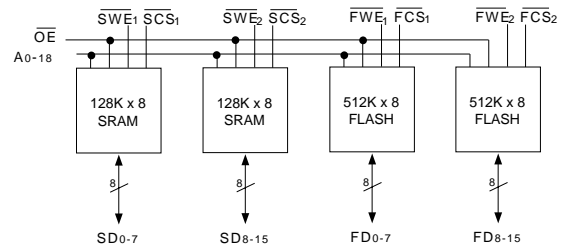


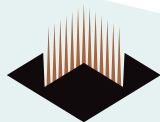
The White 68 lead G2U CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2U has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

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SWE <sub>1-2</sub>	SRAM Write Enable
SCS <sub>1-2</sub>	SRAM Chip Selects
OE	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected
EWE <sub>1-2</sub>	Flash Write Enable
FCS <sub>1-2</sub>	Flash Chip Select

BLOCK DIAGRAM





## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T <sub>A</sub>	-55	+125	°C
Storage Temperature	T <sub>STG</sub>	-65	+150	°C
Signal Voltage Relative to GND	V <sub>G</sub>	-0.5	7.0	V
Junction Temperature	T <sub>J</sub>		150	°C
Supply Voltage	V <sub>CC</sub>	-0.5	7.0	V

Parameter	Value
Flash Data Retention	20 years
Flash Endurance (write/erase cycles)	100,000

### NOTES:

- Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.5	V
Input High Voltage	V <sub>IH</sub>	2.2	V <sub>CC</sub> + 0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.5	+0.8	V

## SRAM TRUTH TABLE

$\overline{SCS}$	$\overline{OE}$	$\overline{SWE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Read	High Z	Active
L	X	L	Write	Data In	Active

## CAPACITANCE

(T<sub>A</sub> = +25°C)

Test	Symbol	Condition	Max	Unit
$\overline{OE}$ Capacitance	C <sub>OE</sub>	V <sub>IN</sub> = 0V, f = 1.0MHz	50	pF
$\overline{WE}$ Capacitance	C <sub>WE</sub>	V <sub>IN</sub> = 0V, f = 1.0MHz	20	pF
$\overline{CS}$ Capacitance	C <sub>CS</sub>	V <sub>IN</sub> = 0V, f = 1.0MHz	20	pF
Data I/O Capacitance	C <sub>I/O</sub>	V <sub>IN</sub> = 0V, f = 1.0MHz	20	pF
Address Line Capacitance	C <sub>AD</sub>	V <sub>IN</sub> = 0V, f = 1.0MHz	50	pF

This parameter is guaranteed by design but not tested.

## DC CHARACTERISTICS

(V<sub>CC</sub> = 5.0V, V<sub>SS</sub> = 0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I <sub>LI</sub>	V <sub>CC</sub> = 5.5, V <sub>IN</sub> = GND to V <sub>CC</sub>		10	μA
Output Leakage Current	I <sub>LO</sub>	$\overline{SCS} = V_{IH}$ , $\overline{OE} = V_{IH}$ , V <sub>OUT</sub> = GND to V <sub>CC</sub>		10	μA
SRAM Operating Supply Current x 16 Mode	I <sub>CCx16</sub>	$\overline{SCS} = V_{IL}$ , $\overline{OE} = \overline{FCS} = V_{IH}$ , f = 5MHz, V <sub>CC</sub> = 5.5		325	mA
Standby Current	I <sub>SB</sub>	$\overline{FCS} = \overline{SCS} = V_{IH}$ , $\overline{OE} = V_{IH}$ , f = 5MHz, V <sub>CC</sub> = 5.5		20	mA
SRAM Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8.0mA, V <sub>CC</sub> = 4.5		0.4	V
SRAM Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -4.0mA, V <sub>CC</sub> = 4.5	2.4		V
Flash V <sub>CC</sub> Active Current for Read (1)	I <sub>CC1</sub>	$\overline{FCS} = V_{IL}$ , $\overline{OE} = \overline{SCS} = V_{IH}$		120	mA
Flash V <sub>CC</sub> Active Current for Program or Erase (2)	I <sub>CC2</sub>	$\overline{FCS} = V_{IL}$ , $\overline{OE} = \overline{SCS} = V_{IH}$		140	mA
Flash Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 12.0mA, V <sub>CC</sub> = 4.5		0.45	V
Flash Output High Voltage	V <sub>OH1</sub>	I <sub>OH</sub> = -2.5 mA, V <sub>CC</sub> = 4.5	0.85 x V <sub>CC</sub>		V
Flash Output High Voltage	V <sub>OH2</sub>	I <sub>OH</sub> = -100 μA, V <sub>CC</sub> = 4.5	V <sub>CC</sub> - 0.4		V
Flash Low V <sub>CC</sub> Lock Out Voltage	V <sub>LKO</sub>		3.2		V

### NOTES:

- The I<sub>CC</sub> current listed includes both the DC operating current and the frequency dependent component (@ 5 MHz). The frequency component typically is less than 2 mA/MHz, with  $\overline{OE}$  at V<sub>IH</sub>.
- I<sub>CC</sub> active while Embedded Algorithm (program or erase) is in progress.
- DC test conditions: V<sub>IL</sub> = 0.3V, V<sub>IH</sub> = V<sub>CC</sub> - 0.3V



**SRAM AC CHARACTERISTICS**  
(VCC = 5.0V, TA = -55°C to +125°C)

Parameter	Symbol	-35		Unit
		Min	Max	
Read Cycle Time	t <sub>RC</sub>	35		ns
Address Access Time	t <sub>AA</sub>		35	ns
Output Hold from Address Change	t <sub>OH</sub>	0		ns
Chip Select Access Time	t <sub>ACS</sub>		35	ns
Output Enable to Output Valid	t <sub>OE</sub>		20	ns
Chip Select to Output in Low Z	t <sub>CLZ</sub> <sup>1</sup>	3		ns
Output Enable to Output in Low Z	t <sub>OLZ</sub> <sup>1</sup>	0		ns
Chip Disable to Output in High Z	t <sub>CHZ</sub> <sup>1</sup>		20	ns
Output Disable to Output in High Z	t <sub>OHZ</sub> <sup>1</sup>		20	ns

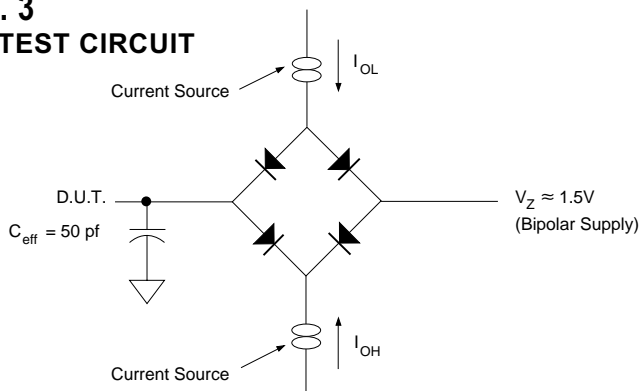
1. This parameter is guaranteed by design but not tested.

**SRAM AC CHARACTERISTICS**  
(VCC = 5.0V, TA = -55°C to +125°C)

Parameter	Symbol	-35		Unit
		Min	Max	
Write Cycle Time	t <sub>WC</sub>	35		ns
Chip Select to End of Write	t <sub>CW</sub>	25		ns
Address Valid to End of Write	t <sub>AW</sub>	25		ns
Data Valid to End of Write	t <sub>DW</sub>	20		ns
Write Pulse Width	t <sub>WP</sub>	25		ns
Address Setup Time	t <sub>AS</sub>	0		ns
Address Hold Time	t <sub>AH</sub>	0		ns
Output Active from End of Write	t <sub>OW</sub> <sup>1</sup>	4		ns
Write Enable to Output in High Z	t <sub>WHZ</sub> <sup>1</sup>		20	ns
Data Hold from Write Time	t <sub>DH</sub>	0		ns

1. This parameter is guaranteed by design but not tested.

**FIG. 3**  
**AC TEST CIRCUIT**



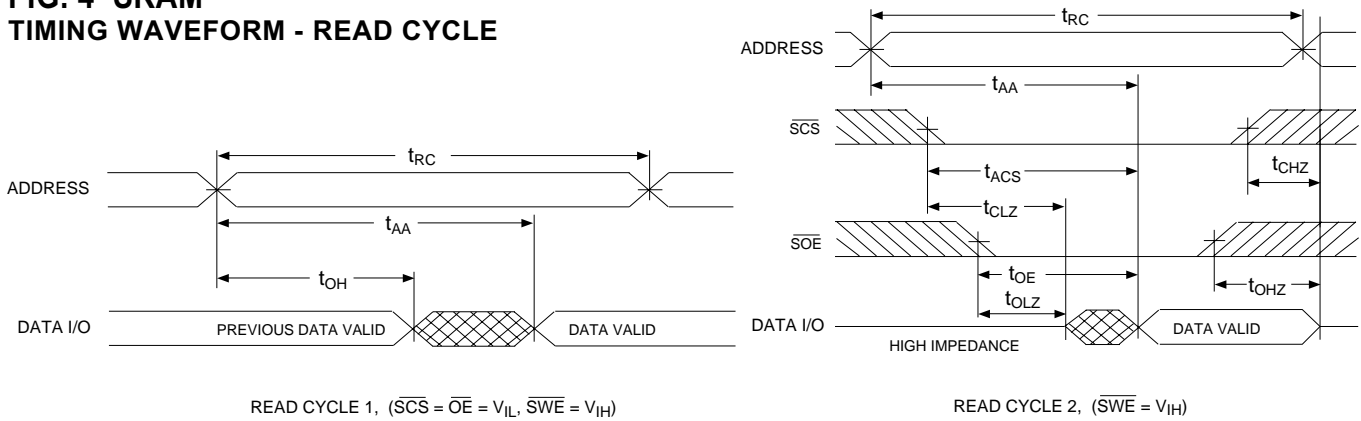
**AC TEST CONDITIONS**

PARAMETER	TYP	UNIT
Input Pulse Levels	V <sub>IL</sub> = 0, V <sub>IH</sub> = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

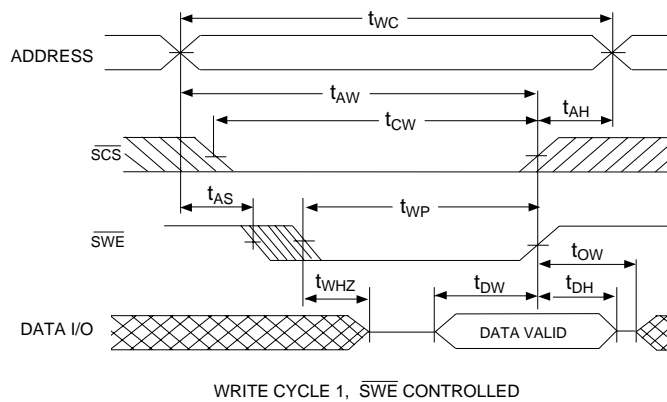
NOTES:  
 Vz is programmable from -2V to +7V.  
 I<sub>OL</sub> & I<sub>OH</sub> programmable from 0 to 16mA.  
 Tester Impedance Z<sub>0</sub> = 75 Ω.  
 Vz is typically the midpoint of V<sub>OH</sub> and V<sub>OL</sub>.  
 I<sub>OL</sub> & I<sub>OH</sub> are adjusted to simulate a typical resistive load circuit.  
 ATE tester includes jig capacitance.



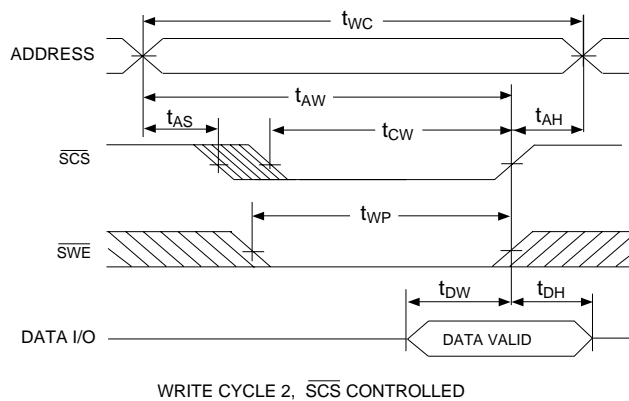
**FIG. 4 SRAM  
TIMING WAVEFORM - READ CYCLE**



**FIG. 5 SRAM  
WRITE CYCLE -  $\overline{SWE}$  CONTROLLED**



**FIG. 6 SRAM  
WRITE CYCLE -  $\overline{SCS}$  CONTROLLED**





**FLASH AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS,  $\overline{\text{FWE}}$  CONTROLLED**  
(V<sub>CC</sub> = 5.0V, T<sub>A</sub> = -55°C to +125°C)

Parameter	Symbol		-90		Unit
			Min	Max	
Write Cycle Time	t <sub>AVAV</sub>	t <sub>WC</sub>	90		ns
Chip Select Setup Time	t <sub>ELWL</sub>	t <sub>CS</sub>	0		ns
Write Enable Pulse Width	t <sub>WLWH</sub>	t <sub>WP</sub>	45		ns
Address Setup Time	t <sub>AVWL</sub>	t <sub>AS</sub>	0		ns
Data Setup Time	t <sub>DVWH</sub>	t <sub>DS</sub>	45		ns
Data Hold Time	t <sub>WHDX</sub>	t <sub>DH</sub>	0		ns
Address Hold Time	t <sub>WLAX</sub>	t <sub>AH</sub>	45		ns
Chip Select Hold Time	t <sub>WHEH</sub>	t <sub>CH</sub>	0		ns
Write Enable Pulse Width High	t <sub>WHWL</sub>	t <sub>WPH</sub>	20		ns
Duration of Byte Programming Operation (1)	t <sub>WHWH1</sub>			300	μs
Sector Erase Time (2)	t <sub>WHWH2</sub>			15	sec
Read Recovery Time Before Write	t <sub>GHWL</sub>		0		μs
V <sub>CC</sub> Set-up Time		t <sub>VCS</sub>	50		μs
Chip Programming Time				11	sec
Output Enable Setup Time		t <sub>OES</sub>	0		ns
Output Enable Hold Time (4)		t <sub>OEH</sub>	10		ns
Chip Erase Time				64	sec

**NOTES:**

1. Typical value for t<sub>WHWH1</sub> is 7μs.
2. Typical value for t<sub>WHWH1</sub> is 1sec.
3. Typical value for Chip Erase Time is 8sec.
4. For Toggle and Data Polling.

**FLASH AC CHARACTERISTICS – READ ONLY OPERATIONS**  
(V<sub>CC</sub> = 5.0V, T<sub>A</sub> = -55°C TO +125°C)

Parameter	Symbol		-90		Unit
			Min	Max	
Read Cycle Time	t <sub>AVAV</sub>	t <sub>RC</sub>	90		ns
Address Access Time	t <sub>AVQV</sub>	t <sub>ACC</sub>		90	ns
Chip Select Access Time	t <sub>ELQV</sub>	t <sub>CE</sub>		90	ns
$\overline{\text{OE}}$ to Output Valid	t <sub>GLQV</sub>	t <sub>OE</sub>		35	ns
Chip Select to Output High Z (1)	t <sub>EHQZ</sub>	t <sub>DF</sub>		20	ns
$\overline{\text{OE}}$ High to Output High Z (1)	t <sub>GHQZ</sub>	t <sub>DF</sub>		20	ns
Output Hold from Address, $\overline{\text{CS}}$ or $\overline{\text{OE}}$ Change, whichever is first	t <sub>AXQX</sub>	t <sub>OH</sub>	0		ns

1. Guaranteed by design, not tested.



**FLASH AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS,  $\overline{\text{FCS}}$  CONTROLLED**  
**( $V_{CC} = 5.0V$ ,  $T_A = -55^{\circ}C$  TO  $+125^{\circ}C$ )**

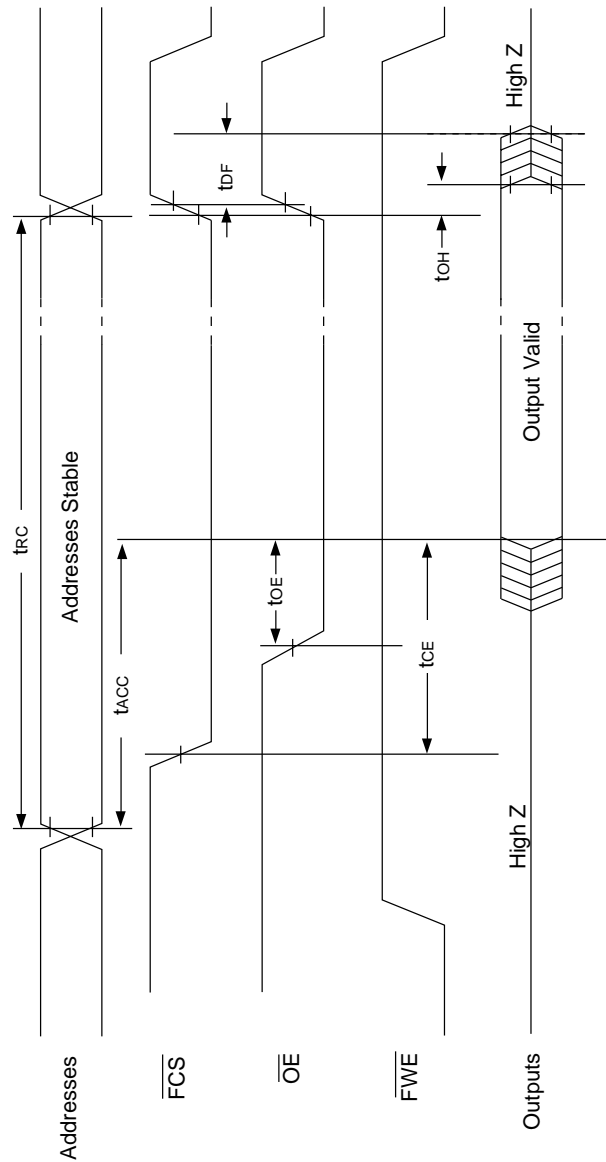
Parameter	Symbol		-90		Unit
			Min	Max	
Write Cycle Time	tAVAV	tWC	90		ns
$\overline{\text{FWE}}$ Setup Time	tWLEL	tWS	0		ns
$\overline{\text{FCS}}$ Pulse Width	tELEH	tCP	45		ns
Address Setup Time	tAVEL	tAS	0		ns
Data Setup Time	tDVEH	tDS	45		ns
Data Hold Time	tEHDX	tDH	0		ns
Address Hold Time	tELAX	tAH	45		ns
$\overline{\text{FWE}}$ Hold from $\overline{\text{FWE}}$ High	tEHHW	tWH	0		ns
$\overline{\text{FCS}}$ Pulse Width High	tEHEL	tCPH	20		ns
Duration of Byte Programming Operation (1)	tWHWH1			300	ms
Duration of Erase Operation (2)	tWHWH2			15	sec
Read Recovery before Write	tGHXL		0		ns
Chip Programming Time				11	sec
Chip Erase Time (3)				64	sec

**NOTES:**

1. Typical value for tWHWH1 is 7 $\mu$ s.
2. Typical value for tWHWH1 is 1sec.
3. Typical value for Chip Erase Time is 8sec.



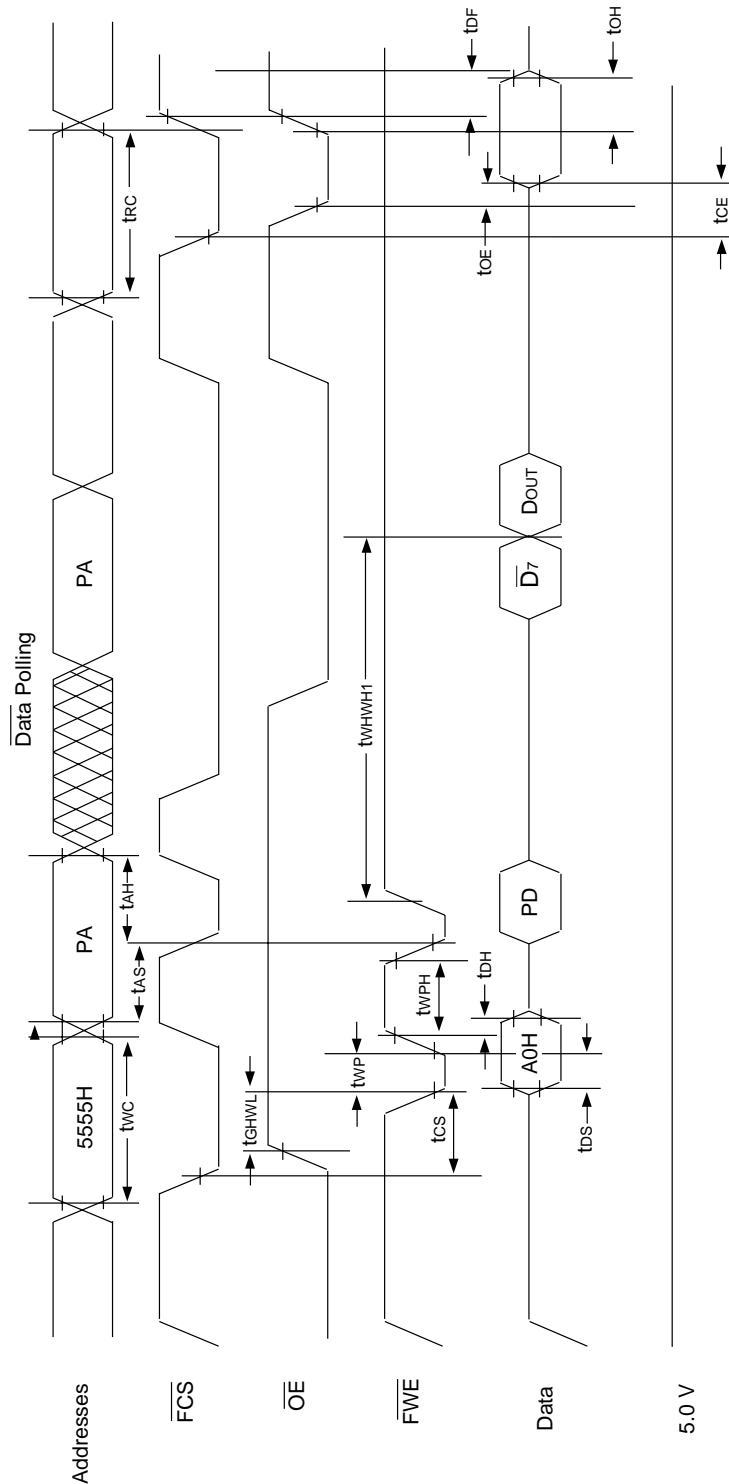
**FIG. 7**  
**AC WAVEFORMS FOR FLASH MEMORY READ OPERATIONS**







**FIG. 8**  
**WRITE/ERASE/PROGRAM OPERATION, FLASH MEMORY  $\overline{FWE}$  CONTROLLED**

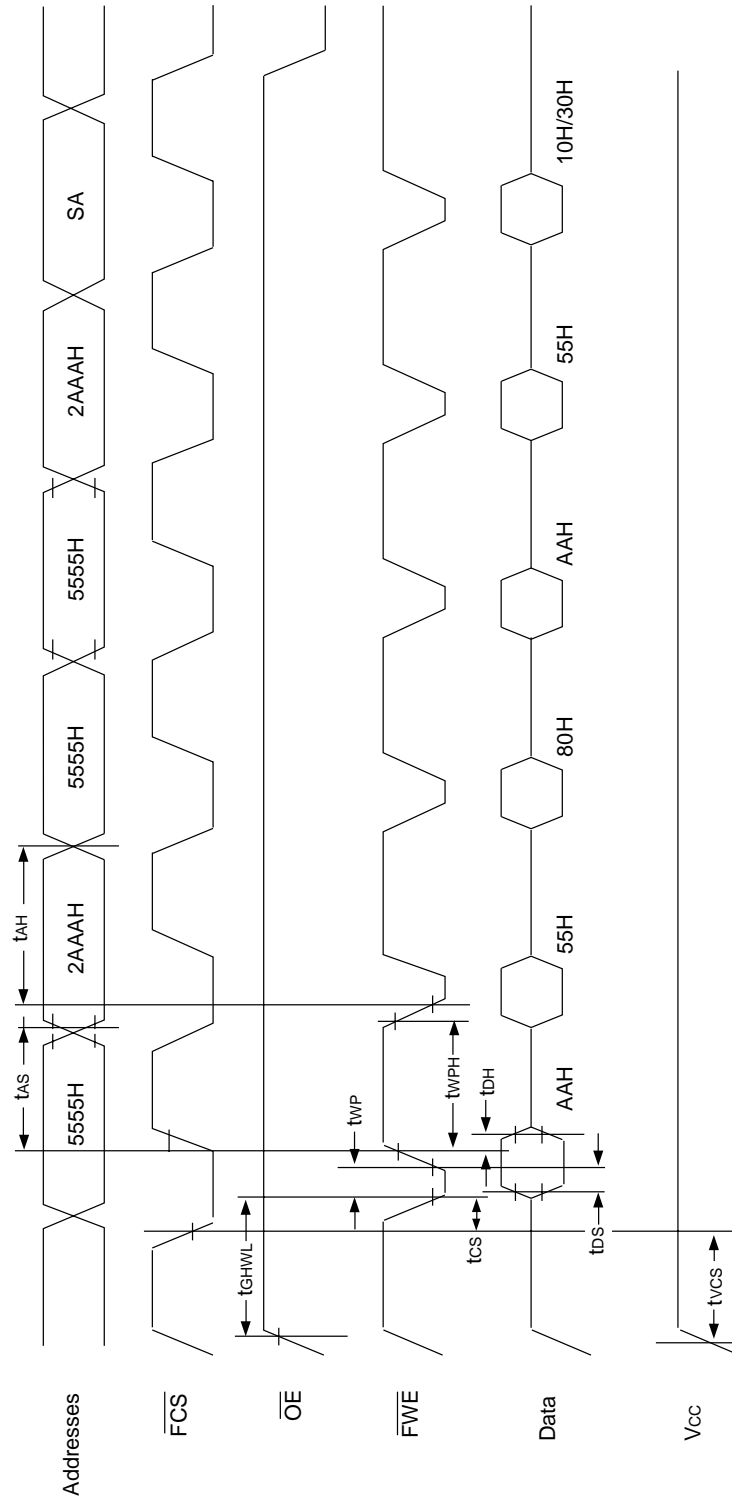


**NOTES:**

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3.  $\overline{D7}$  is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.



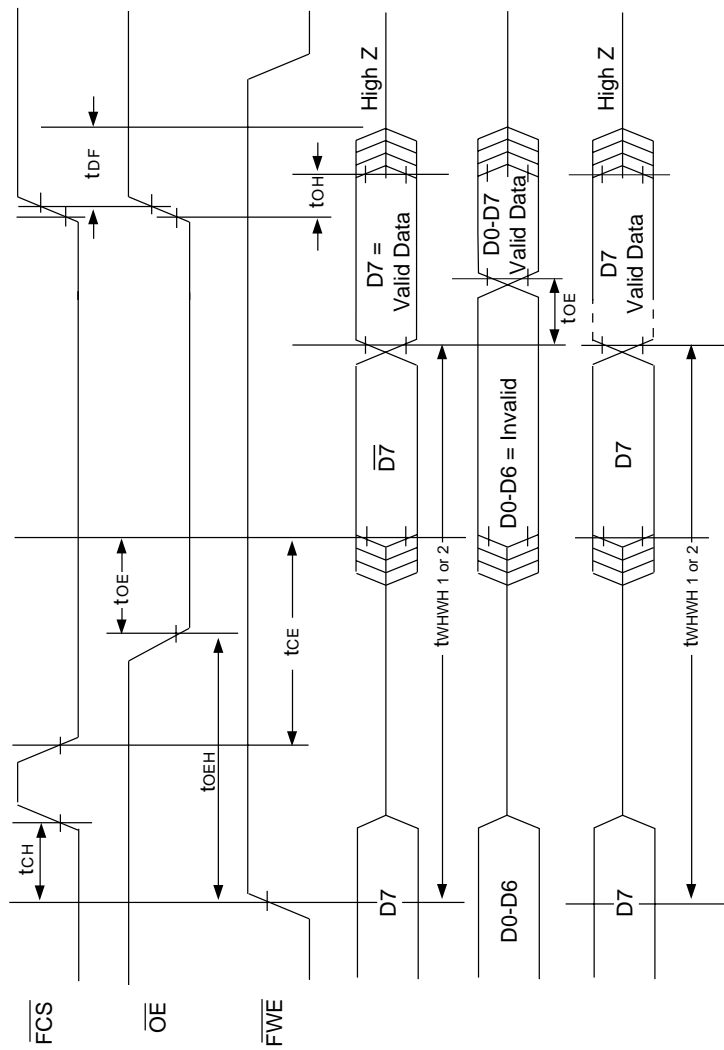
**FIG. 9**  
**AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS FOR FLASH MEMORY**



**NOTES:**  
 1. SA is the sector address for Sector Erase.

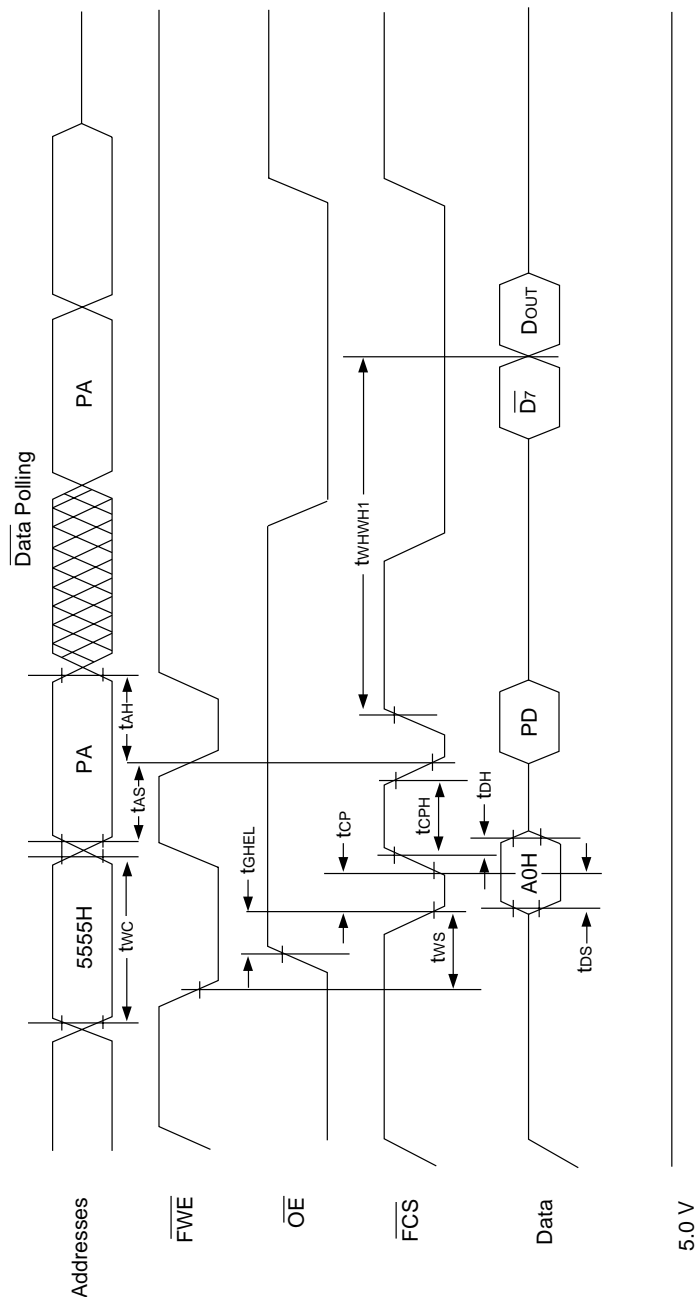


**FIG. 10**  
**AC WAVEFORMS FOR DATA POLLING DURING EMBEDDED ALGORITHM OPERATIONS**  
**FOR FLASH MEMORY**





**FIG. 11**  
**WRITE/ERASE/PROGRAM OPERATION FOR FLASH MEMORY,  $\overline{CS}$  CONTROLLED**

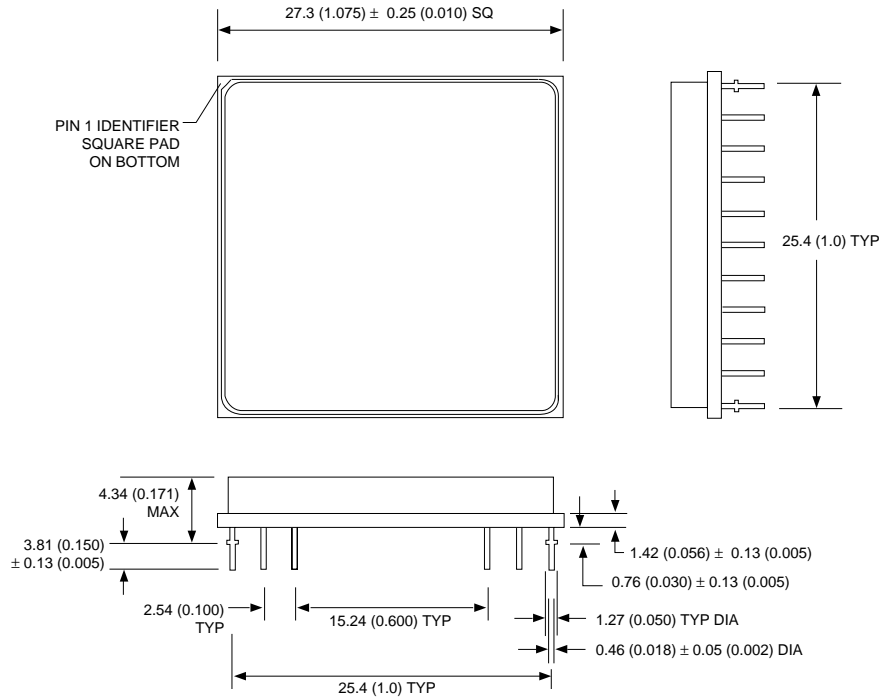


**NOTES:**

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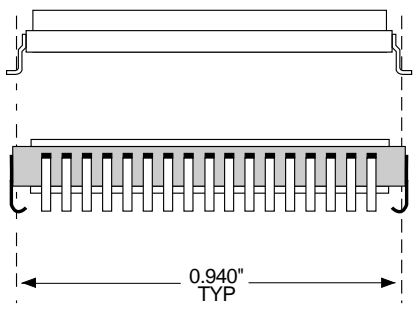
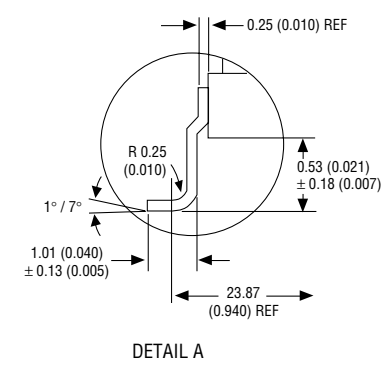
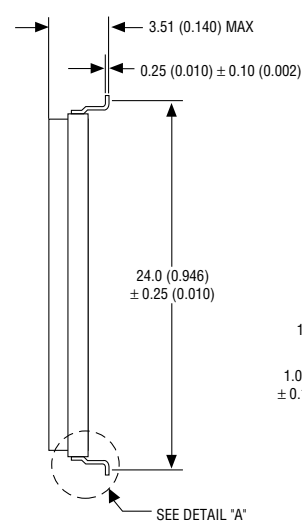
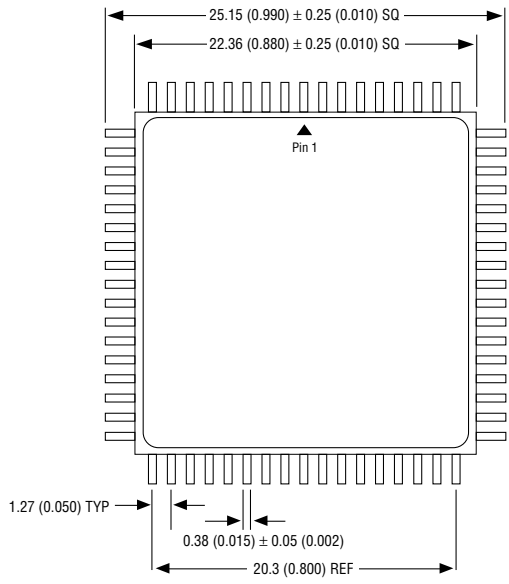
**PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)**



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



PACKAGE 510: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2U)



The White 68 lead G2U CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2U has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



### ORDERING INFORMATION

**W S F 2816 - 39 X X X**

**LEAD FINISH:**

Blank = Gold plated leads

A = Solder dip leads

**DEVICE GRADE:**

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C

**PACKAGE TYPE:**

H1= 1.075" sq. Ceramic Hex In-line Package, HIP (Package 400)

G2U = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 510)

**ACCESS TIME (ns)**

39 = 35ns SRAM and 90ns FLASH

**2Mbit of SRAM and 8Mbit of Flash**

**ORGANIZATION: 128K x 16 SRAM and  
512K x 16 Flash**

**Flash**

**SRAM**

**WHITE ELECTRONIC DESIGNS CORP.**