512Kx32 SRAM MODULE, 3.3V

FEATURES

- DSP Memory Solution
  - ADSP-21060L (SHARC)
  - ADSP-21062L (SHARC)
  - Texas Instruments TMS320LC31
- RISC Memory Solution
  - MPC860 (Power Quic)
- Random Access Memory Array
  - Fast Access Times: 12, 15, 17, and 20ns
  - Individual Byte Enables
  - User configurable organization with Minimal Additional Logic
  - Master Output Enable and Write Control
  - TTL Compatible Inputs and Outputs
  - Fully Static, No Clocks
- Surface Mount Package
  - 68 Lead PLCC, No. 99 JEDEC M0-47AE
  - Small Footprint, 0.990 Sq. In.
  - Multiple Ground Pins for Maximum Noise Immunity
- Single +3.3V (±5%) Supply Operation

The EDI8L32512V is a high speed, 3.3V, 16 megabit SRAM. The device is available with access times of 12, 15, 17 and 20ns allowing the creation of a no wait state DSP and RISC microprocessor memory solutions.

The device can be configured as a 512K x 32 and used to create a single chip external data memory solution for TI's TMS320LC31 (figure 5), or Analog's SHARC™ DSP (figure 6).

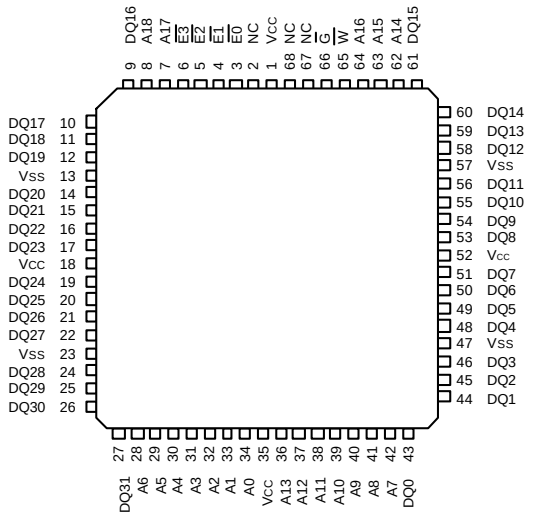
The device provides a 56% space savings when compared to four 512K x 8, 36 pin SOJs. In addition the EDI8L32512C has only a 10pF load on the data lines vs. 32pf for four plastic SOJs.

The device provides a memory upgrade of the EDI8L32256V (256K x 32) or the EDI8L32128V (128K x 32) (figure 8). Alternatively, the device's chip enables can configure it as a 1M x 16. A 1Mx 48 program memory array for Analog's SHARC DSP is created using three devices (figure 7). If this memory is too deep, two 512K x 24s (EDI8L24512V) can be used to create a 512K x 48 array or two 128K x 24s (EDI8L24128V) can be used to create a 128K x 48 array.

Note: *Solder Reflow Temperature should not exceed 260°C for 10 seconds.*

FIG. 1 PIN CONFIGURATION

TOP VIEW

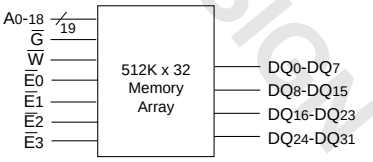


NOTE: *For memory upgrade information, refer to Page 7, Figure 8 "EDI MCM-L upgrade path.*

PIN DESCRIPTION

A0-18	Address Inputs
$\overline{E}$0-3	Chip Enables (One per Byte)
$\overline{W}$	Master Write Enable
$\overline{G}$	Master Output Enable
DQ0-31	Common Data Input/Output
VCC	Power (+3.3V±5%)
VSS	Ground
NC	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS}	-0.5V to 7.0V
Operating Temperature T_A (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature, Plastic	-55°C to +125°C
Power Dissipation	2.5 Watts
Output Current	20 mA
Junction Temperature, T_J	+175°C

* Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

$\overline{E}$	$\overline{W}$	$\overline{G}$	Mode	Output	Power
H	X	X	Standby	High Z	I_{CC2}, I_{CC3}
L	H	H	Output Deselect	High Z	I_{CC1}
L	H	L	Read	Data Out	I_{CC1}
L	L	X	Write	Data In	I_{CC1}

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Supply Voltage	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	Vcc +0.3	V
Input Low Voltage	V_{IL}	-0.3	—	+0.8	V

CAPACITANCE

(f = 1.0MHz, V_{IN} = V_{CC} or V_{SS})

Parameter	Sym	Max	Unit
Address Lines	C_I	30	pF
Data Lines	$C_{D/Q}$	10	pF
Write & Output Enable Line	$\overline{W}$, $\overline{G}$	30	pF
Chip Enable Line	E_{0-3}	8	pF

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V, T_A = 25°C)

Parameter	Symbol	Conditions	12 & 15 Min	12 & 15 Typ	12 & 15 Max	17 & 20 Min	17 & 20 Typ	17 & 20 Max	Units
Operating Power Supply Current	I_{CC1}	$\overline{W}$ = V_{IL}, $I_{I/O}$ = 0mA, Min Cycle	—	440	720	—	440	640	mA
Standby (TTL) Power Supply Current	I_{CC2}	$\overline{E} \geq V_{IH}$, $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$	—	100	200	—	100	200	mA
Full Standby Power CMOS Supply Current	I_{CC3}	$\overline{E} \geq V_{CC}$ -0.2V $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V	—	60	100	—	60	100	mA
Input Leakage Current	I_{LI}	V_{IN} = 0V to V_{CC}	—	—	±10	—	—	±10	µA
Output Leakage Current	I_{LO}	$V_{I/O}$ = 0V to V_{CC}	—	—	±10	—	—	±10	µA
Output High Voltage	V_{OH}	I_{OH} = -4.0mA	2.4	—	—	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 4.0mA	—	—	0.4	—	—	0.4	V

AC TEST CONDITIONS

Figure 1

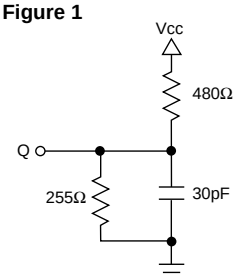
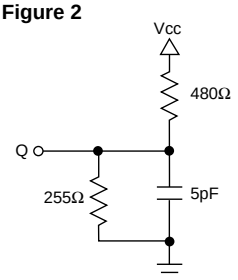


Figure 2



Input Pulse Levels	V_{SS} to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

(**NOTE:** For t_{EHQZ}, t_{GHQZ} and t_{WLQZ}, CL = 5pF, Figure 2)

AC CHARACTERISTICS – READ CYCLE

(V_{CC} = 3.3V, V_{SS} = 0V, T_A = 0°C to + 70°C)

Parameter	Symbol JEDEC	Symbol Alt.	12ns Min	12ns Max	15ns Min	15ns Max	17ns Min	17ns Max	20ns Min	20ns Max	Units
Read Cycle Time	tAVAV	tRC	12		15		17		20		ns
Address Access Time	tAVQV	tAA		12		15		17		20	ns
Chip Enable Access Time	tELQV	tACS		10		12		15		20	ns
Chip Enable to Output in Low Z (1)	tELQX	tCLZ	3		3		3		3		ns
Chip Disable to Output in High Z (1)	tEHQZ	tCHZ		6		7		8		9	ns
Output Hold from Address Change	tAVQX	tOH	3		3		3		3		ns
Output Enable to Output Valid	tGLQV	tOE		6		7		8		9	ns
Output Enable to Output in Low Z (1)	tGLQX	tOLZ	3		3		3		3		ns
Output Disable to Output in High Z (1)	tGHQZ	tOHZ		6		7		8		9	ns

1. This parameter is guaranteed by design but not tested.

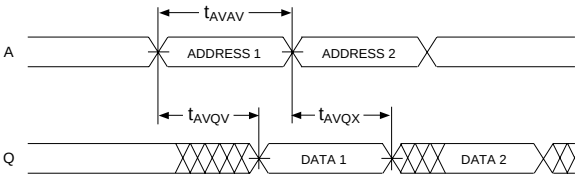
AC CHARACTERISTICS – WRITE CYCLE

(V_{CC} = 3.3V, V_{SS} = 0V, T_A = 0°C to + 70°C)

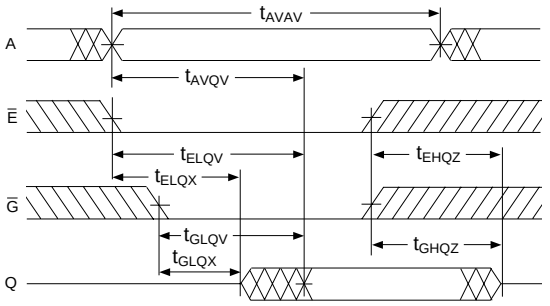
Parameter	Symbol JEDEC	Symbol Alt.	12ns Min	12ns Max	15ns Min	15ns Max	17ns Min	17ns Max	20ns Min	20ns Max	Units
Write Cycle Time	tAVAV	tWC	12		15		17		20		ns
Chip Enable to End of Write	tELWH tELEH	tCW tCW	8 8		10 10		11 11		12 12		ns ns
Address Setup Time	tAVWL tAVEL	tAS tAS	0 0		0 0		0 0		0 0		ns ns
Address Valid to End of Write	tAVWH tAVEH	tAW tAW	8 8		10 10		11 11		12 12		ns ns
Write Pulse Width	tWLWH tELEH	tWP tWP	8 8		10 10		11 11		12 12		ns ns
Write Recovery Time	tWHAX tEHAX	tWR tWR	0 0		0 0		0 0		0 0		ns ns
Data Hold Time	tWHDX tEHDX	tDH tDH	0 0		0 0		0 0		0 0		ns ns
Write to Output in High Z (1)	tWLQZ	tWHZ	0	6	0	7	0	8	0	9	ns
Data to Write Time	tDVWH tDVEH	tDW tDW	6 6		7 7		8 8		9 9		ns ns
Output Active from End of Write (1)	tWHQX	tWLZ	3		3		3		3		ns

1. This parameter is guaranteed by design but not tested.

FIG. 2
TIMING WAVEFORM - READ CYCLE

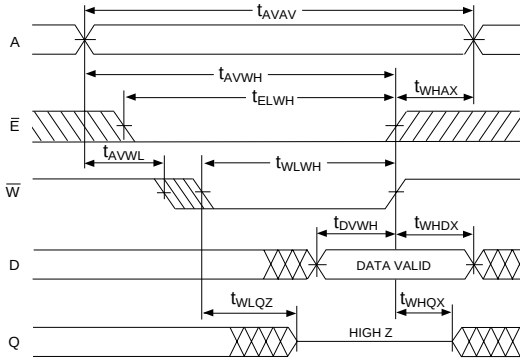


READ CYCLE 1 ($\overline{W}$ HIGH; $\overline{G}$, $\overline{E}$ LOW)



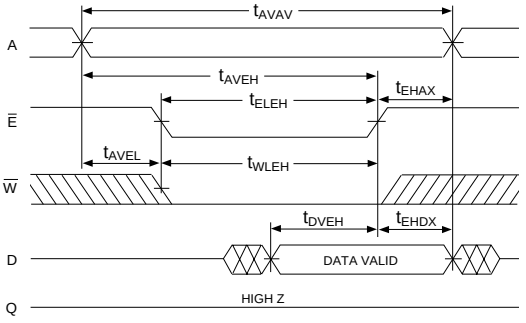
READ CYCLE 2 ($\overline{W}$ HIGH)

FIG. 3
WRITE CYCLE - $\overline{W}$ CONTROLLED



WRITE CYCLE 1, $\overline{W}$ CONTROLLED

FIG. 4
WRITE CYCLE - $\overline{E}$ CONTROLLED



WRITE CYCLE 2, $\overline{E}$ CONTROLLED

ORDERING INFORMATION

Commercial Temperature Range (0°C to +70°C)

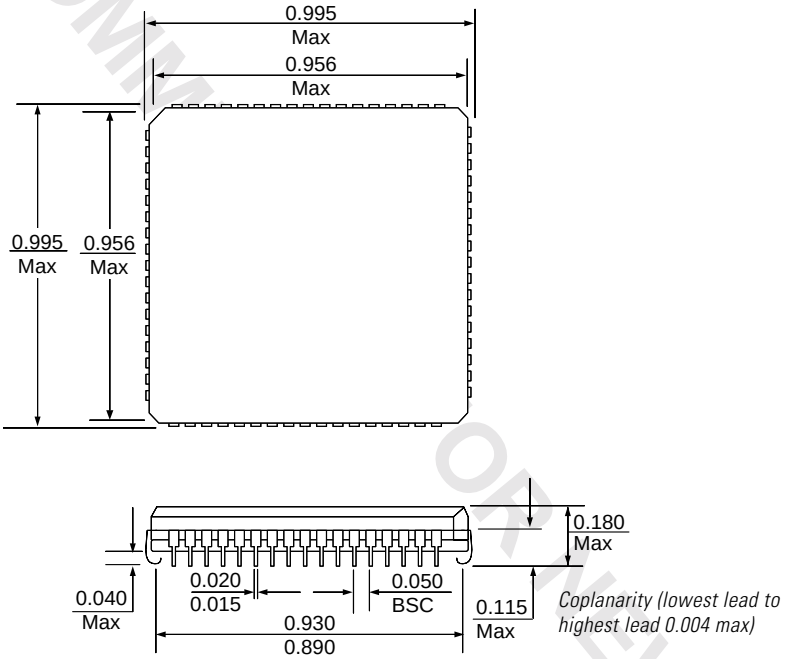
Part Number	Speed (ns)	Package No.
EDI8L32512V12AC	12	99
EDI8L32512V15AC	15	99
EDI8L32512V17AC	17	99
EDI8L32512V20AC	20	99

Industrial Temperature Range (-40°C to +85°C)

Part Number	Speed (ns)	Package No.
EDI8L32512V15AI	15	99
EDI8L32512V17AI	17	99
EDI8L32512V20AI	20	99

PACKAGE 99: 68 LEAD PLCC

JEDEC MO-47AE



ALL DIMENSIONS ARE IN INCHES

FIG. 5
INTERFACING THE TEXAS INSTRUMENTS TMS320LC31 WITH THE EDI8L32512V (512Kx32)

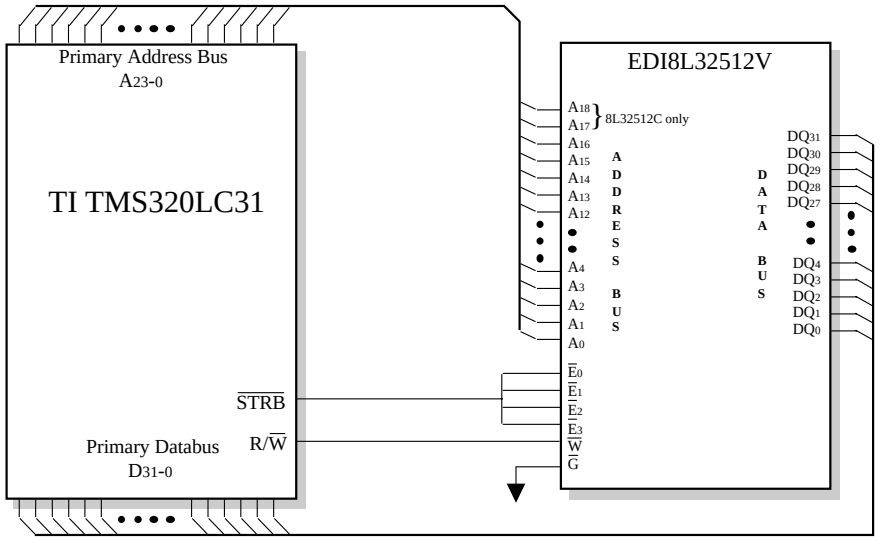


FIG. 6
INTERFACING THE ANALOG SHARC DSP WITH THE EDI8L32512V (512Kx32 ARRAY).

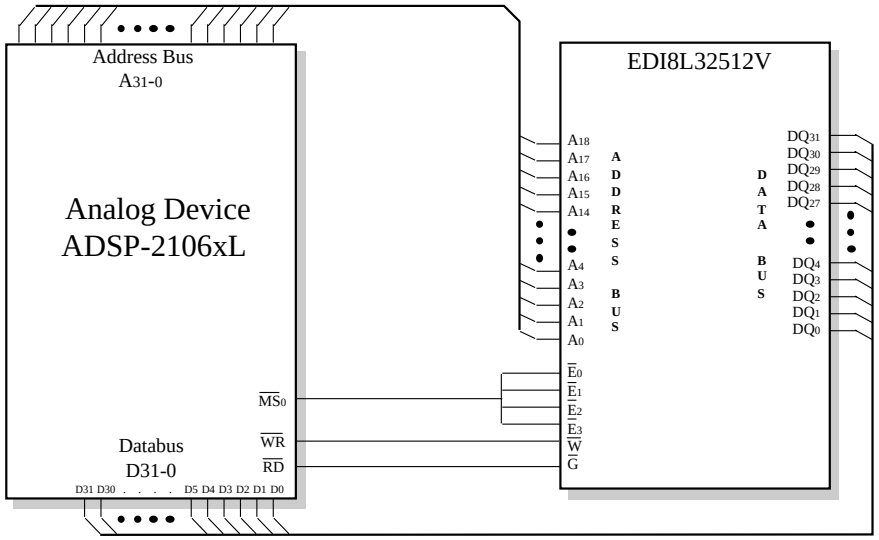


FIG. 7
INTERFACING THE ANALOG SHARC DSP WITH THE EDI8L32512V (1Mx48 ARRAY)

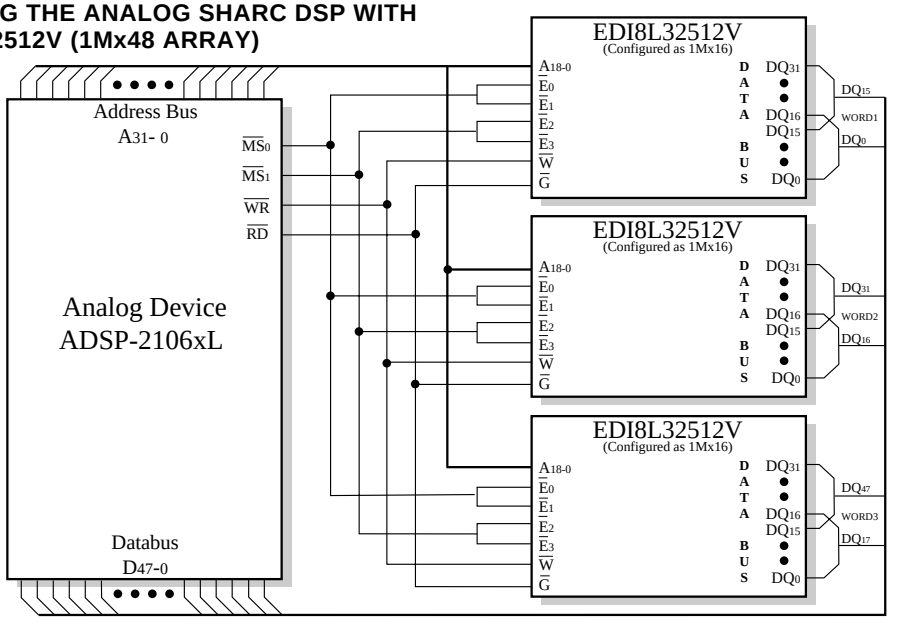


FIG. 8
MCM-L UPGRADE PATH