





## Absolute Maximum Ratings\*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to + 70°C
Industrial	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Power Dissipation	3.0 Watts
Output Current	20 mA
Junction Temperature, TJ	175°C

\*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.75	5.0	5.25	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	VCC+0.5	V
Input Low Voltage	VIL	-0.3	--	0.8	V

## AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	Figure 1

(note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

Figure 1

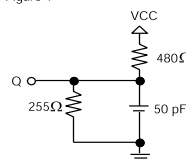
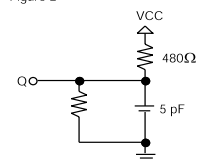


Figure 2



## DC Electrical Characteristics

Parameter	Sym	Conditions	Min	Max	Unit
Operating Power	ICC1	$\bar{W} = V_{IL}$ , I/O = 0mA, Min Cycle		12ns* 500	mA
Supply Current				15ns 460	
Standby (TTL)	ICC2	$\bar{E} \geq V_{IH}$ , $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$ , f=0MHz	60	60	60
Supply Current				20/25ns	mA
Full Standby	ICC3	$\bar{E} \geq V_{CC}-0.2V$	20	20	20
Supply Current CMOS		$V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$			
Input Leakage Current	ILI	$V_{IN} = 0V$ to VCC	±10	±10	±10
Output Leakage Current	ILO	$V_{I/O} = 0V$ to VCC		±10	±10
Output High Voltage	VOH	I/OH = -4.0mA	2.4		
Output Low Voltage	VOL	I/OH = 8.0mA	0.4	0.4	0.4
					V

\*Typical: TA = 25°C, VCC = 5.0V

\*Advanced Information

## Truth Table

$\bar{E}$	W	$\bar{G}$	BS0-3	Mode	Output	Power
H	X	X	X	Standby	High Z	ICC2, ICC3
L	H	H	X	Output Disable	High Z	ICC1
L	X	X	H	Output Disable	High Z	ICC1
L	H	L	L	Read	Dout	ICC1
L	L	X	L	Write	Din	ICC1

X Means Don't Care

## Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CA	20	pF
Data Lines	CD/Q	10	pF
Write & Output Enable Lines	W, $\bar{G}$	16	pF
Chip Enable Lines	$\bar{E}$ , $\bar{BS}$	9	pF

These parameters are sampled, not 100% tested.



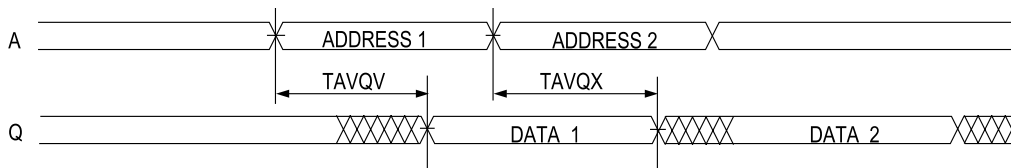
## AC Characteristics Read Cycle

Parameter	Symbol		12ns*		15ns		20ns		25ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	TAVAV	TRC	12		15		20		25		ns
Address Access Time	TAVQV	TAA		12		15		20		25	ns
Chip Enable Access Time	TELQV	TACS		12		15		20		25	ns
Byte Select Access Time	TBLQV	TBA		12		15		20		25	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		3		ns
Byte Select to Output in Low Z	TBLQX	TBLZ	3		3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		7		8		10		10	ns
Byte Select to Output in High Z	TBHQZ	TBHZ		7		8		10		10	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		5		6		8		10	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	2		2		2		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		4		5		8		10	ns

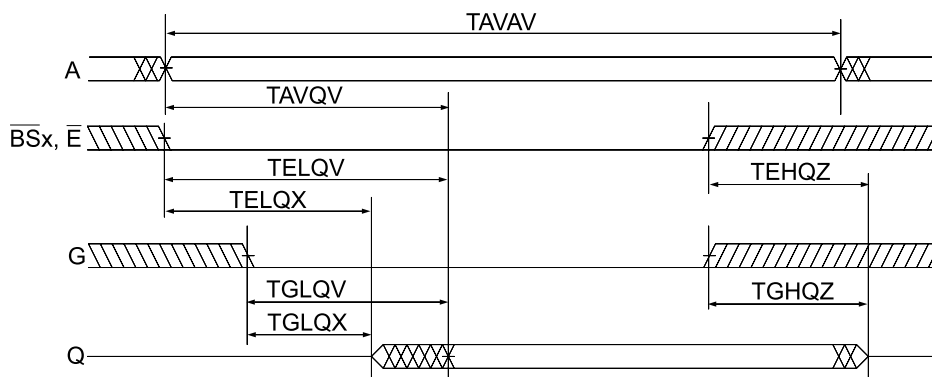
Note 1: Parameter guaranteed, but not tested.

\*Advanced Information

### Read Cycle 1 - $\overline{W}$ High, $\overline{G}$ , $\overline{E}$ Low



### Read Cycle 2 - $\overline{W}$ High





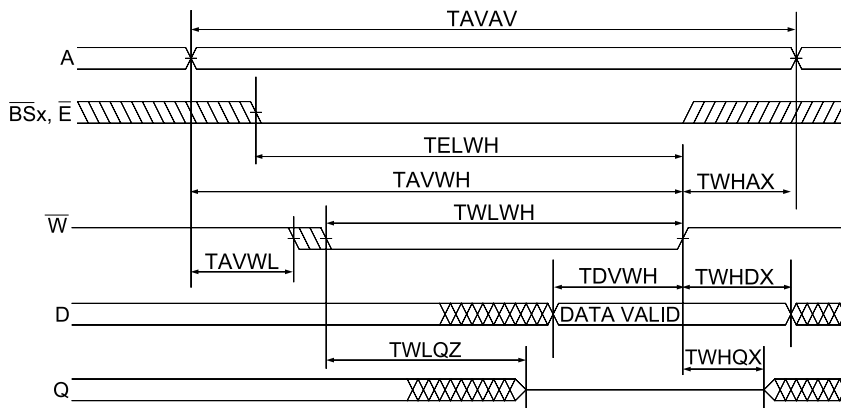
## AC Characteristics Write Cycle

Parameter	Symbol		12ns*		15ns		20ns		25ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV	TWC	12		15		20		25		ns
Chip Enable to End of Write	TELWH	TCW	8		9		15		20		ns
	TELEH	TCW	8		9		15		20		ns
Byte Select to end of Write	TBLWH	TBW	8		9		15		20		ns
Address Setup Time	TAVWL	TAS	0		0		0		0		ns
	TAVEL	TAS	0		0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	9		10		15		15		ns
	TAVEH	TAW	9		10		15		15		ns
Write Pulse Width	TWLWH	TWP	9		10		15		15		ns
	TWLEH	TWP	9		10		15		15		ns
Write Recovery Time	TWHAX	TWR	0		0		0		0		ns
	TEHAX	TWR	0		0		0		0		ns
Data Hold Time	TWHDX	TDH	0		0		0		0		ns
	TEHDX	TDH	0		0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	5	0	6	0	7	0	10	ns
Data to Write Time	TDVWH	TDW	5		6		8		12		ns
	TDVEH	TDW	5		6		8		12		ns
Output Active from End of Write (1)	TWHQX	TWLZ	2		2		2		2		ns

Note 1: Parameter guaranteed, but not tested.

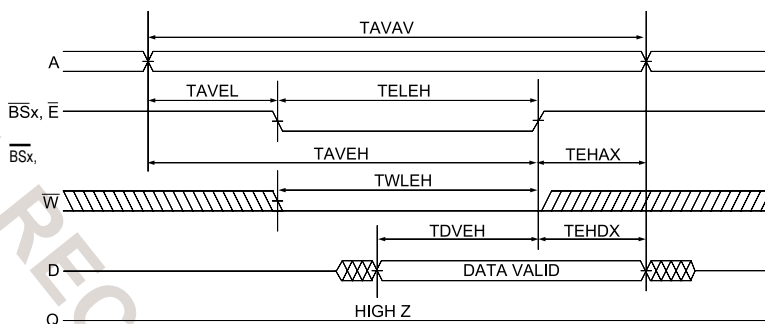
\*Advanced Information

## Write Cycle 1 - $\overline{W}$ Controlled





## Write Cycle 2 - $\bar{E}$ Controlled



## Ordering Information

Commercial (0°C to 70°C)

Part Number	Speed (ns)	Package No.
ED18L3265C12AC*	12	99
ED18L3265C15AC	15	99
ED18L3265C20AC	20	99
ED18L3265C25AC	25	99

\*Advanced Information

Industrial (-40°C to +85°C)

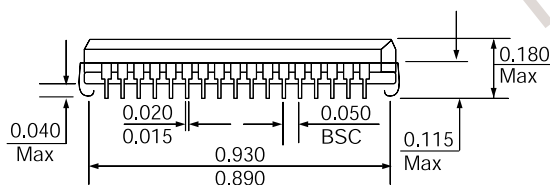
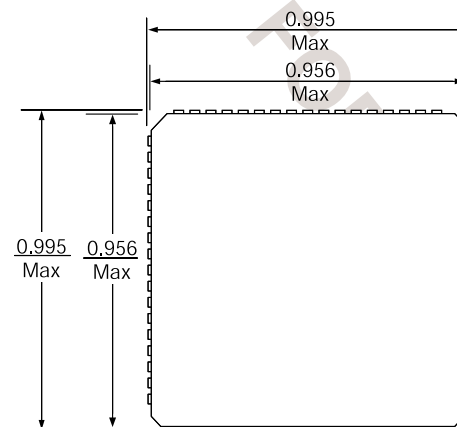
Part Number	Speed (ns)	Package No.
ED18L3265C15AI	15	99
ED18L3265C20AI	20	99
ED18L3265C25AI	25	99

## Package Description

Package No. 99

68 Lead PLCC

JEDEC M0-47AE



**EDI MCM-L Upgrade Path**