4x128Kx16 Static RAM CMOS, Module

FEATURES

- 4x128Kx16 bit CMOS Static
- Random Access Memory
  - Access Times 70 thru 100ns
  - Data Retention Function (EDI9F416128LP)
  - TTL Compatible Inputs and Outputs
  - Fully Static, No Clocks
- High Density Packaging
  - 80 Pin SIMM, No. 318
- Single +5V (±10%) Supply Operation

DESCRIPTION

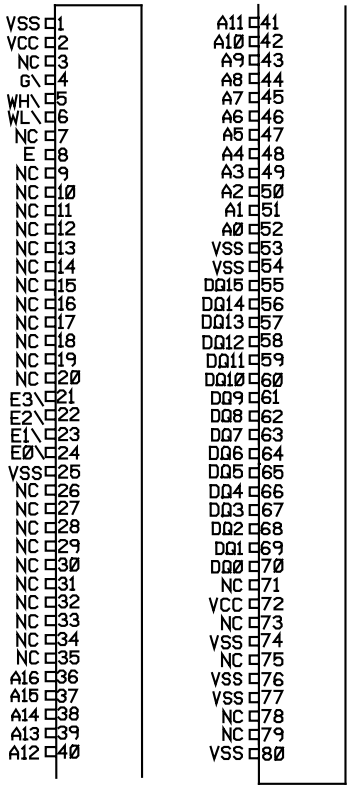
The EDI9F416128C is a 8192K bit CMOS Static RAM based on eight 128Kx8 Static RAMs mounted on a multi-layered epoxy laminate (FR-4) substrate.

A low power version with data retention (EDI9F416128LP) is also available.

All inputs and outputs are TTL compatible and operate from a single +5V supply. Fully asynchronous, the EDI9F416128C requires no clocks or refreshing for operation.

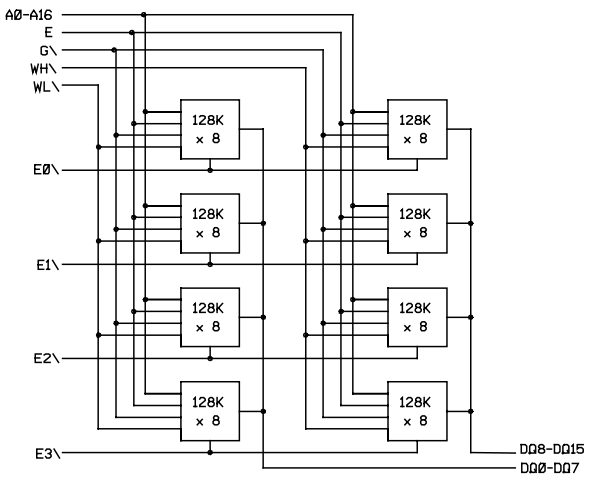
FIG. 1

PIN CONFIGURATIONS AND BLOCK DIAGRAM



PIN NAMES

AØ-A16	Address Inputs
$\overline{E}$Ø-$\overline{E}$3	Chip Enable
$\overline{G}$	Output Enables
$\overline{WH}$-$\overline{WL}$	Write Enables
E	Chip Select
DQØ-DQ15	Data Input/Output
VCC	Supply 5 Volts
VSS	Ground
NC	No Connect



ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature	
Plastic	-55°C to +125°C
Power Dissipation	1 Watt
Output Current.	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC TEST CONDITIONS

Input Pulse Levels		VSS to 3.0V
Input Rise and Fall Times		5ns
Input and Output Timing Levels		1.5V
Output Load	70ns	1TTL = 30pF
	85-120ns	1TTL, CL =100pF

(note: For TEHQZ,TGHQZ and TWLQZ, CL = 5pF)

DC ELECTRICAL CHARACTERISTICS

Parameter	Sym	Conditions		Min	Typ	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle		–	94	158	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E} \geq$ VIH, VIN $\leq$ VIL VIN $\geq$ VIH		–	56	120	mA
Full Standby Power Supply Current CMOS	ICC3	$\overline{E} \geq$ VCC-0.2V VIN $\geq$ VCC-0.2V or VIN $\leq$ 0.2V	C	–		24	mA
			LP	–		80	µA
Input Leakage Current	ILI	VIN = 0V to VCC		–	–	±10	µA
Output Leakage Current	ILO	V I/O = 0V to VCC		–	–	±10	µA
Output High Voltage	VOH	IOH = -1.0mA		2.4	–	–	V
Output Low Voltage	VOL	IOL = 2.1mA		–	–	0.4	V

TRUTH TABLE

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

CAPACITANCE

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	60	pF
Data Lines	CD/Q	80	pF
Chip Enable Line	CC	15	pF
Write and Output Enable Lines	CW	60	pF

AC CHARACTERISTICS READ CYCLE

Parameter	Symbol JEDEC	Alt.	70ns Min	70ns Max	85ns Min	85ns Max	100ns Min	100ns Max	Units
Read Cycle Time	TAVAV	TRC	70		85		100		ns
Address Access Time	TAVQV	TAA		70		85		100	ns
Chip Enable Access Time	TELQV	TACS		70		85		100	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	5		5		5		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ		30		35		40	ns
Output Hold from Address Change	TAVQX	TOH	3		3		3		ns
Output Enable to Output Valid	TGLQV	TOE		40		45		50	ns
Output Enable to Output in Low Z (1)	TGLQX	TOLZ	0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ		30		35		40	ns

FIG. 2

READ CYCLE 1 - $\overline{W}$ HIGH, $\overline{G}$, $\overline{E}$ LOW

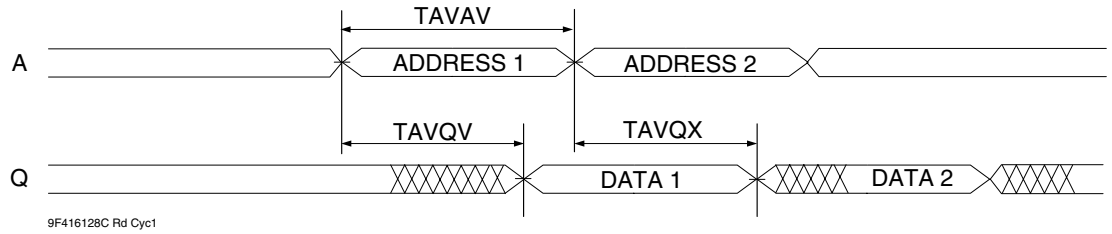
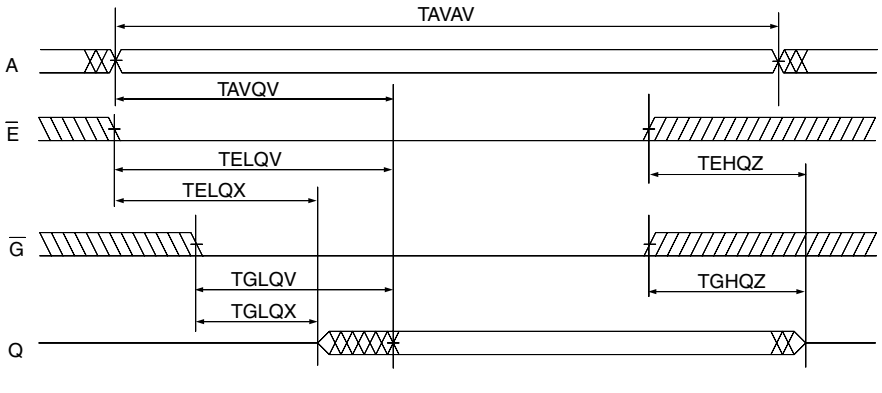


FIG. 3

READ CYCLE 2 - $\overline{W}$ HIGH



AC CHARACTERISTICS WRITE CYCLE

Parameter	Symbol JEDEC	Alt.	70ns Min	70ns Max	85ns Min	85ns Max	100ns Min	100ns Max	Units
Write Cycle Time	TAVAV	TWC	70		85		100		ns
Chip Enable to End of Write	TELWH	TCW	65		70		80		ns
	TELEH	TCW	65		70		80		ns
Address Setup Time	TAVWL	TAS	0		0		0		ns
	TAVEL	TAS	0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	65		70		80		ns
	TAVEH	TAW	65		70		80		ns
Write Pulse Width	TWLWH	TWP	65		70		80		ns
	TWLEH	TWP	65		70		80		ns
Write Recovery Time	TWHAX	TWR	0		0		0		ns
	TEHAX	TWR	0		0		0		ns
Data Hold Time	TWHDX	TDH	0		0		0		ns
	TEHDX	TDH	0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	30	0	35	0	40	ns
Data to Write Time	TDVWH	TDW	30		35		40		ns
	TDVEH	TDW	30		35		40		ns
Output Active from End of Write (1)	TWHQX	TWLZ	5		5		5		ns

Note 1: Parameter guaranteed, but not tested. *Advance Information

FIG. 4

WRITE CYCLE 1 - $\overline{W}$ CONTROLLED

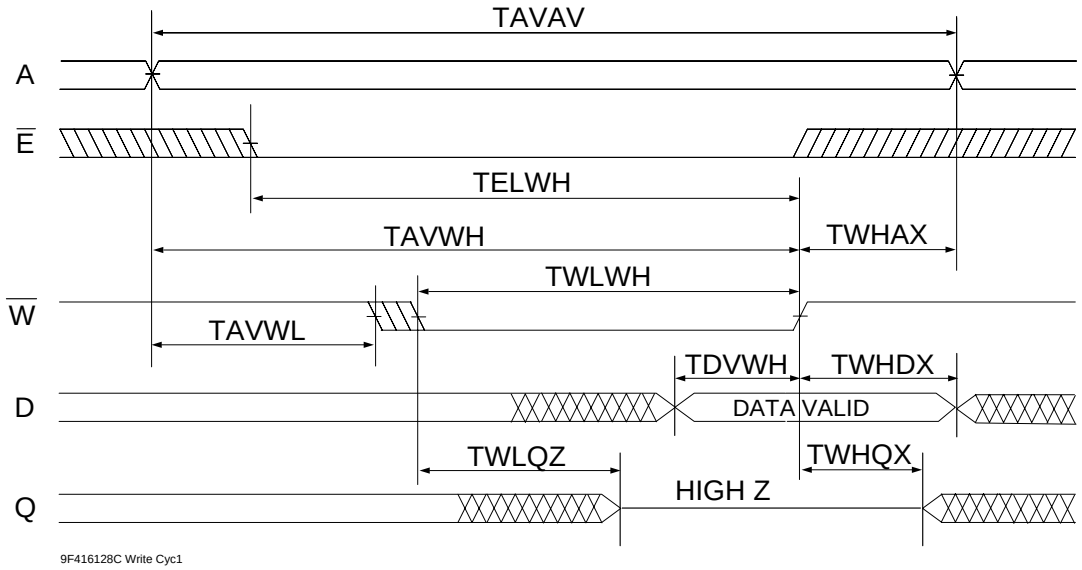
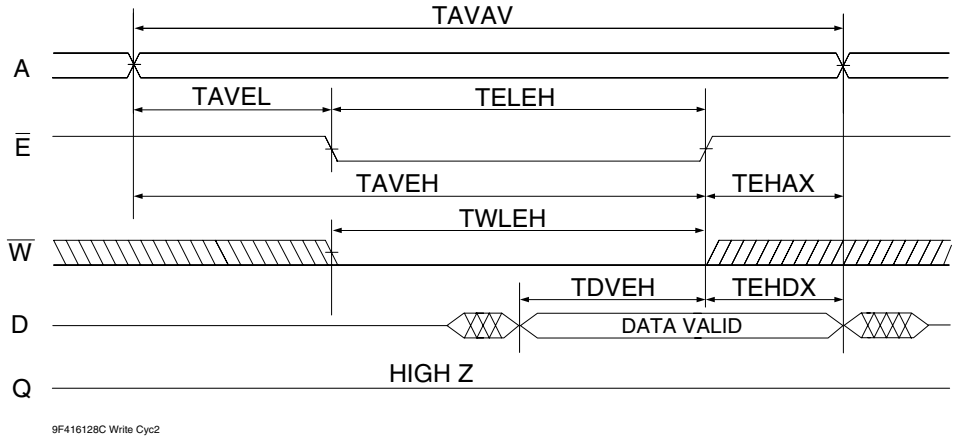


FIG. 5

WRITE CYCLE 2 - $\overline{E}$ CONTROLLED

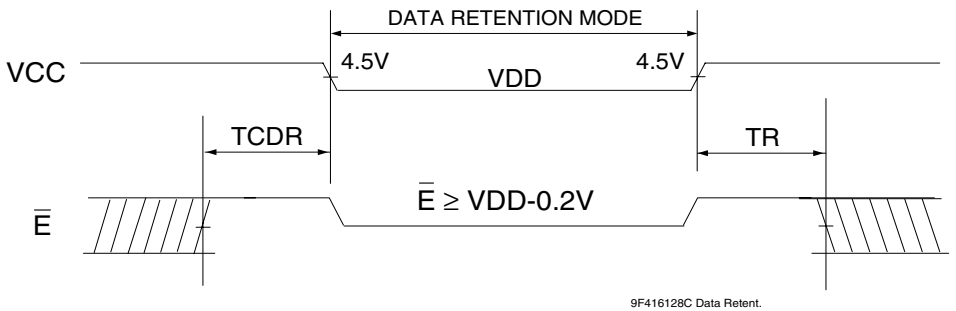


DATA RETENTION CHARACTERISTICS

Characteristic	Sym	Test Conditions	VDD	Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 0.2V		2	–		V
Data Retention Quiescent Current	ICCDR	$\overline{E}$ ž VDD -0.2V	2V	–	1	6	µA
		VIN ž VDD -0.2V	3V	–	1	8	µA
Chip Disable to Data Retention Time(1)	TCDR	or VIN - 0.2V		0	--	–	ns
Operation Recovery Time (1)	TR			5	--	–	ms

FIG. 6

DATA RETENTION - $\overline{E}$ CONTROLLED



ORDERING INFORMATION

Part Number	Speed (ns)	Package No.
Standard Power		
EDI9F416128C70BNC	70	318
EDI9F416128C85BNC	85	318
EDI9F416128C100BNC	100	318
Low Power		
EDI9F416128LP70BNC	70	318
EDI9F416128LP85BNC	85	318
EDI9F416128LP100BNC	100	318

Note: To order an Industrial grade product substitute the letter C in the Suffix with the letter I, eg. EDI9F416128C70BNC becomes EDI9F416128C70BNI.

PACKAGE DESCRIPTION

PACKAGE NO. 318: 80 LEAD SIMM ANGLED